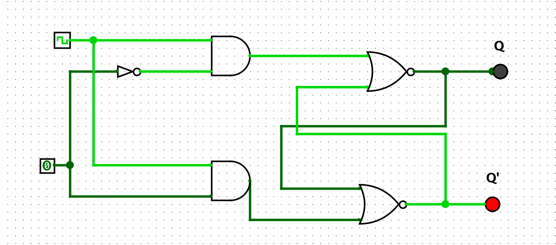


1. When the inputs are 1, the states of the outputs remain unchanged.

2. This input condition is forbidden as it forces outputs of both NOR Gates to become 0, which is a violation of complementary outputs. Even if this input condition is applied, if the next inputs become R = 0 and S = 0 (hold condition), then it causes a ‘race condition’ between the NOR Gates, which causes an unstable or unpredictable state at the output.

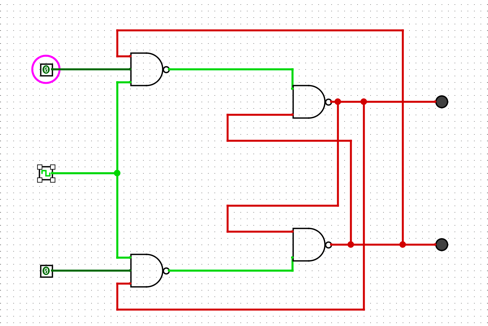
|  |  |  |  |
| --- | --- | --- | --- |
| Set | Reset | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | INVALID | INVALID |



1. D flip – flops are also called as “Delay flip – flop” or “Data flip – flop”. They are used to store 1 – bit binary data. They are one of the widely used flip – flops in digital electronics. Apart from being the basic memory element  in  digital systems, D flip – flops are also considered as Delay line elements  and  Zero – Order Hold elements. D flip – flop has two inputs , a clock (CLK) input and a data (D) input and two outputs; one is main output represented by Q and the other is complement of Q represented by Q’.

2. When we don’t apply any clock input to the D flip flop or during the falling edge of the clock signal, there will be no change in the output. It will retain its previous value at the output Q. If the clock signal is high (rising edge to be more precise) and if D input is high, then the output is also high and if  D input is low, then the output will become low. Hence the output Q follows the input D in the presence of clock signal.

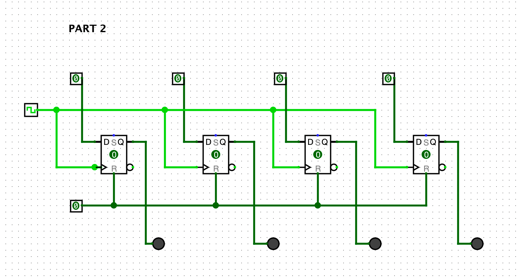
|  |  |  |  |
| --- | --- | --- | --- |
| Clock | Pin | Q | Q’ |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |



1. The given JK flip-flop can be converted into a D-type flip-flop by driving its J and K input pins with the D input and its negation, respectively. Thus the additional hardware component required would be a NOT gate, resulting in the digital system

2. If both the J and K inputs are HIGH at logic “1” (J = K = 1), when the clock input goes HIGH, the circuit will “toggle” as its outputs switch and change state complementing each other. This results in the JK flip-flop acting more like a T-type toggle flip-flop when both terminals are “HIGH”.

|  |  |  |  |
| --- | --- | --- | --- |
| J | K | Q | Q’ |
| 0 | 0 | Q | Q’ |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | toggle | toggle |



|  |  |  |
| --- | --- | --- |
| Ox | Input Binary | Output Binary |
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0010 |
| 3 | 0011 | 0011 |
| 4 | 0100 | 0100 |
| 5 | 0101 | 0101 |
| A | 1010 | 1010 |
| B | 1011 | 1011 |
| C | 1100 | 1100 |
| D | 1101 | 1101 |
| E | 1110 | 1110 |
| F | 1111 | 1111 |