

EEE3096S-2023

Tutorial 2



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1 I2C Communication

1.1 Message Structure for I2C protocol when master communicates with slave

- **Start condition:** Signifies the beginning of the communication.
- **Address byte:** 7 bits of the 8-bit address byte are the slave device address and the last bit determines if the operation is a read (1) or write (0).
- **Acknowledge bit (ACK):** After every byte, the receiver sends an acknowledge bit.
- **Data byte(s):** 8-bit long data chunks.
- **Stop condition:** Signifies the end of the communication.

1.2 Advantages of I2C over SPI

- **Fewer pins/wires required:** I2C only requires 2 bus lines (SDA and SCL) regardless of the number of devices, while SPI needs 4 lines (MOSI, MISO, SCK, CS) for each device.
- **In-built addressing scheme:** Every I2C device has a unique address, allowing communication without additional select lines, unlike SPI which requires separate chip select lines for each device.

1.3 Start and Stop Conditions for I2C

- **Start Condition:** When the SDA line transitions from high to low while the SCL is high.
- **Stop Condition:** When the SDA line transitions from low to high while the SCL is high.

1.4 Timing Diagram

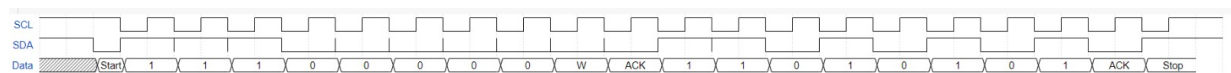


Figure 1: Timing Diagram

2 Binary Coded Decimal (BCD)

2.1 What Binary Coded Decimal is

BCD is a method of decimal digits storage and representation using a four-bit binary code for each digit. For example, the BCD representation of 582 is 0101 1000 0010.

2.2 Advantages and Disadvantages of BCD

Advantage	Disadvantage
Simplifies arithmetic of decimals	BCD requires more bits to represent a given range of values compared to pure binary representation.

3 Unix Epoch

3.1 What Unix Epoch Time is

Epoch Time is a system for tracking time that defines the time as the number of seconds that have elapsed since 00:00:00 Coordinated Universal Time (UTC) on Thursday, 1 January 1970, minus leap seconds.

3.1.1 Why it is used

- **Standardization:** It offers a standard reference point, ensuring consistency across systems.
- **Simplicity:** Representing time as a single ever-increasing number simplifies time calculations and comparisons.

3.2 Epoch Time for 01 January 2023 at 12:00:00 AM (timezone GMT+02:00):

The Unix Epoch Time for January 1, 2023, at 12:00:00 AM (timezone GMT+02:00) is 1672567200000 milliseconds

4 RTS and RISC/CISC

4.1 Dynamic Synchronous Hard Real-time System

A Dynamic Synchronous Hard Real-time System is a system where tasks are scheduled at run-time (dynamic) based on some priority or scheduling algorithm, operate in synchronization with a clock, and have strict timing constraints (hard real-time) that must be met. Failure to meet these constraints can result in catastrophic failures.

4.2 RISC vs. CISC

Characteristic	RISC	CISC
Instruction Set Size	Uses a small set of simple and general instructions.	Uses a large set of complex and specialized instructions.
Memory Access For Operands	Memory access typically performed through explicit load and store instructions	May have instructions that directly operate on memory locations, allowing operations to be performed directly between memory and registers