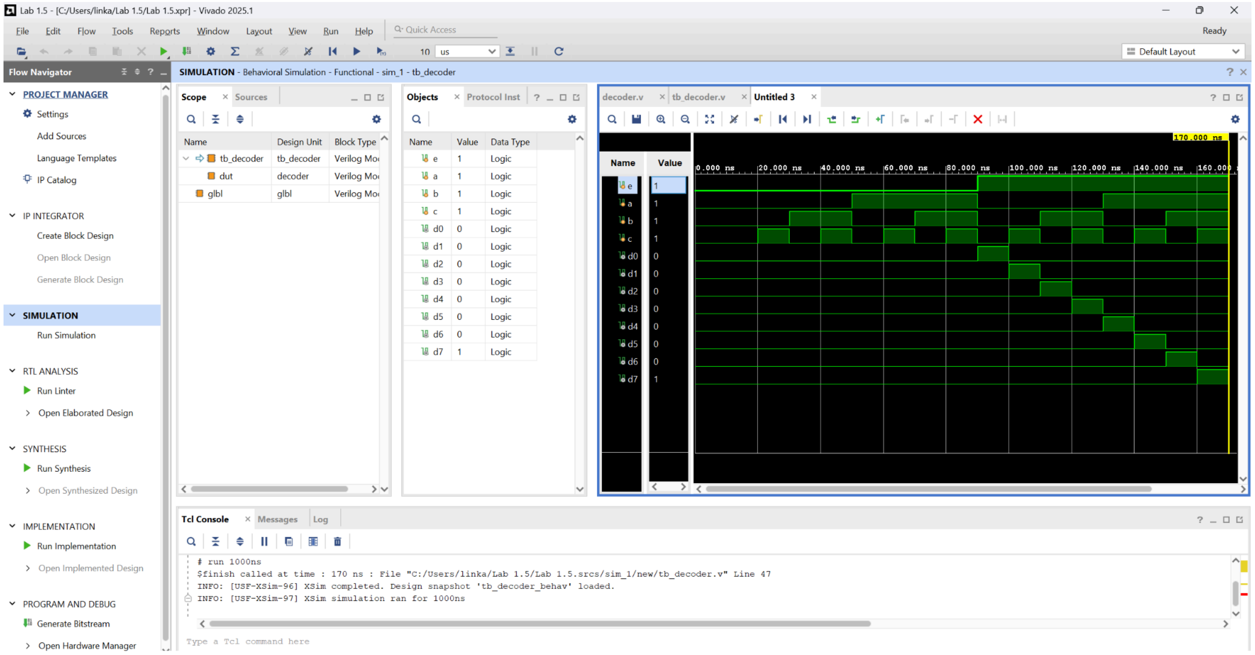
Part 1

i)

Simulation (Structural):



Lab 1.5 - [C:/Users/linka/Lab 1.5/Lab 1.5.xpr] - Vivado 2025.1

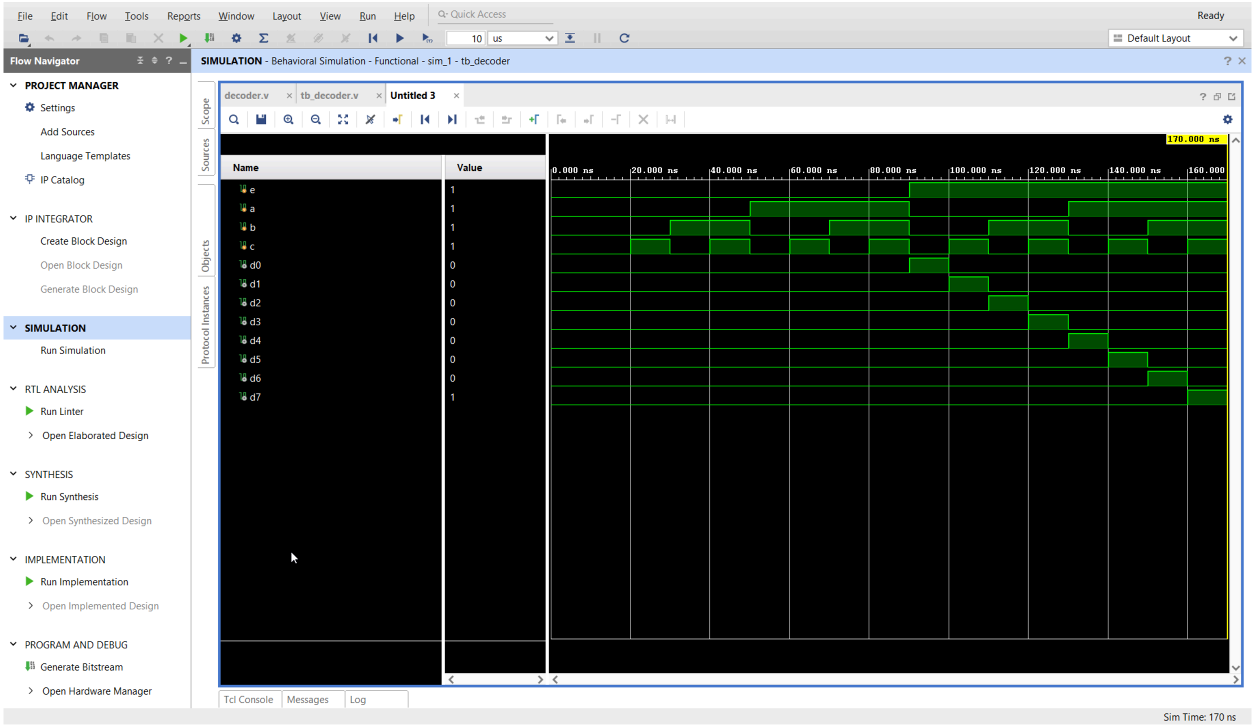
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_decoder

Name	Design Unit	Block Type
tb_decoder	tb_decoder	Verilog Mo
dut	decoder	Verilog Mo
glbl	glbl	Verilog Mo

Name	Value	Data Type
e	1	Logic
a	1	Logic
b	1	Logic
c	1	Logic
d0	0	Logic
d1	0	Logic
d2	0	Logic
d3	0	Logic
d4	0	Logic
d5	0	Logic
d6	0	Logic
d7	1	Logic

```
# run 1000ns
$finish called at time : 170 ns : File "C:/Users/linka/Lab 1.5/Lab 1.5.srcs/sim_1/new/tb_decoder.v" Line 47
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_decoder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Simulation (Behavioral):



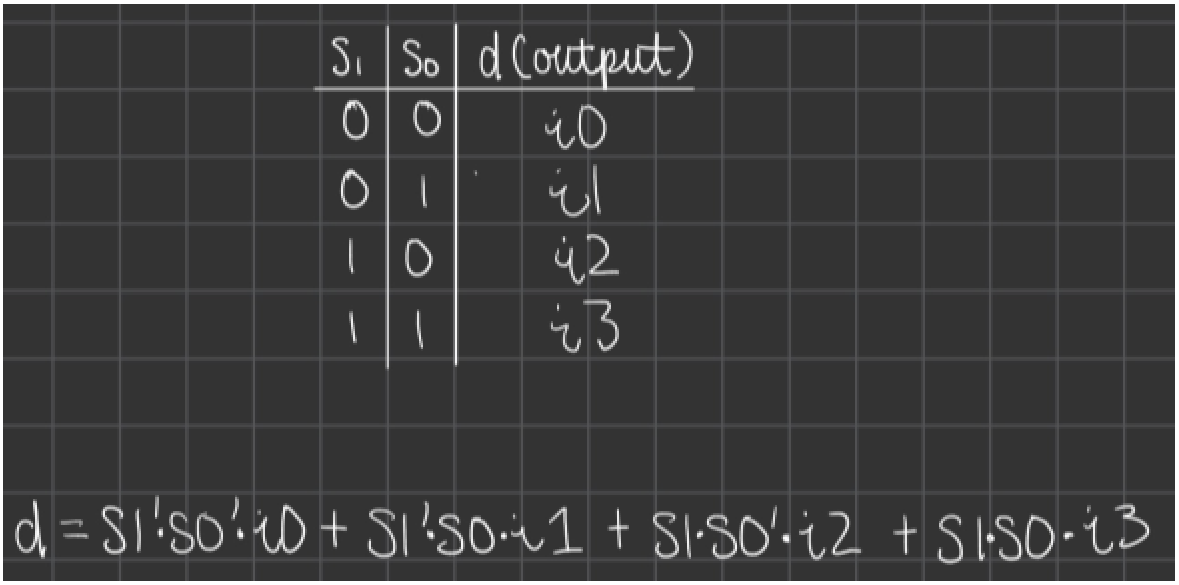
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_decoder

Name	Value
e	1
a	1
b	1
c	1
d0	0
d1	0
d2	0
d3	0
d4	0
d5	0
d6	0
d7	1

Sim Time: 170 ns

Part 2

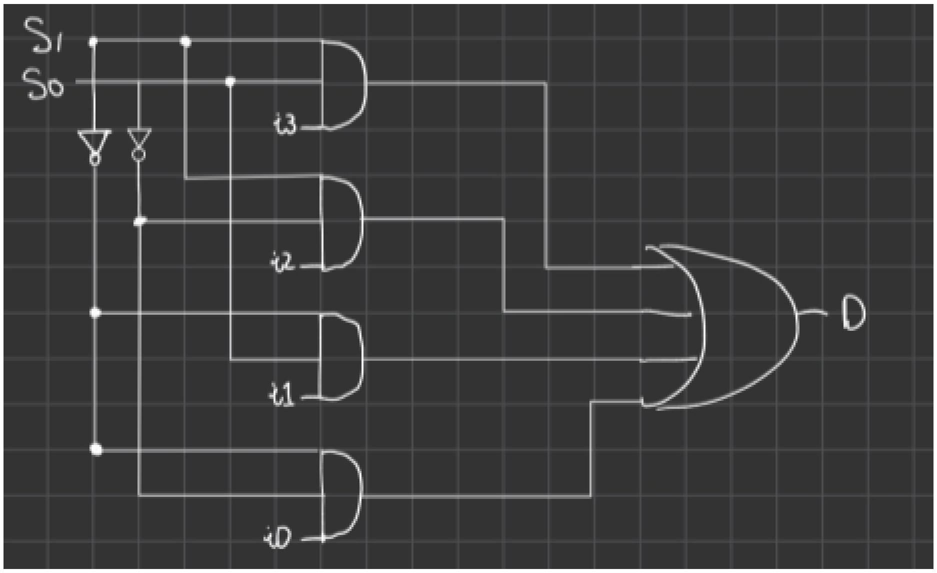
ii. Truth table of the function iii. Algebraic expression of the logic function



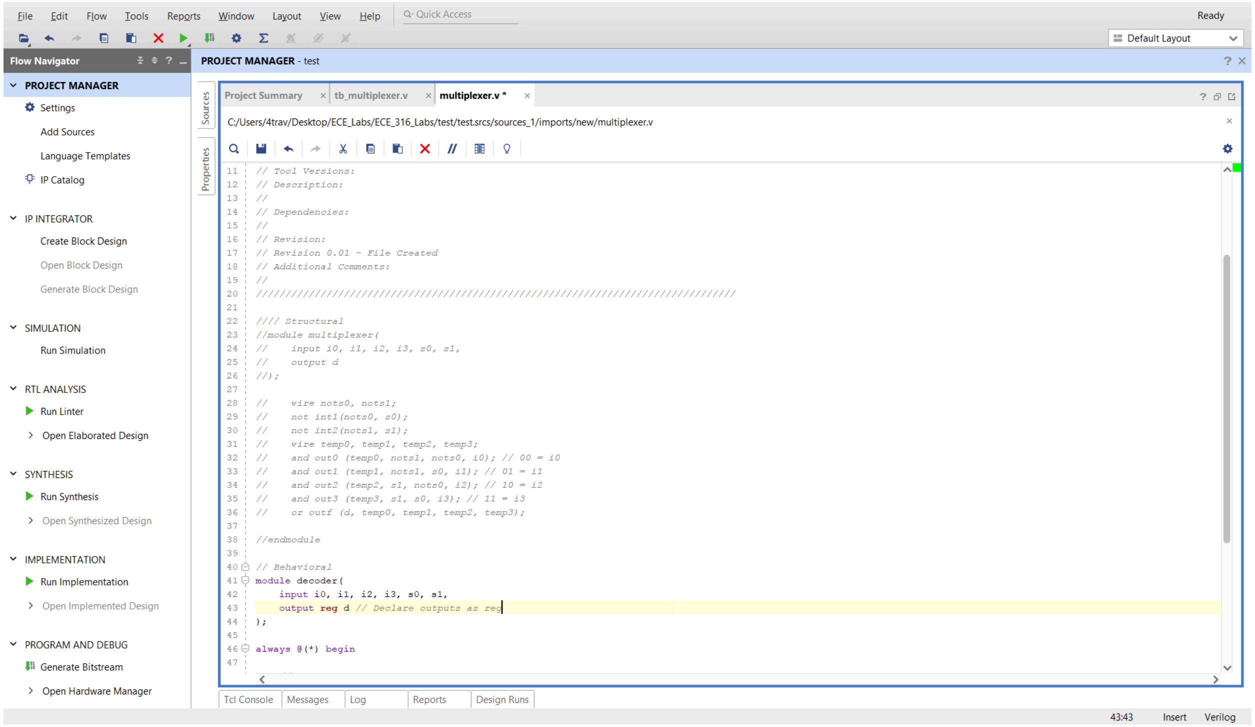
S_1	S_0	d (output)
0	0	i0
0	1	i1
1	0	i2
1	1	i3

$$d = S1' \cdot S0' \cdot i0 + S1' \cdot S0 \cdot i1 + S1 \cdot S0' \cdot i2 + S1 \cdot S0 \cdot i3$$

iv. Logic circuit schematic for structural modelling

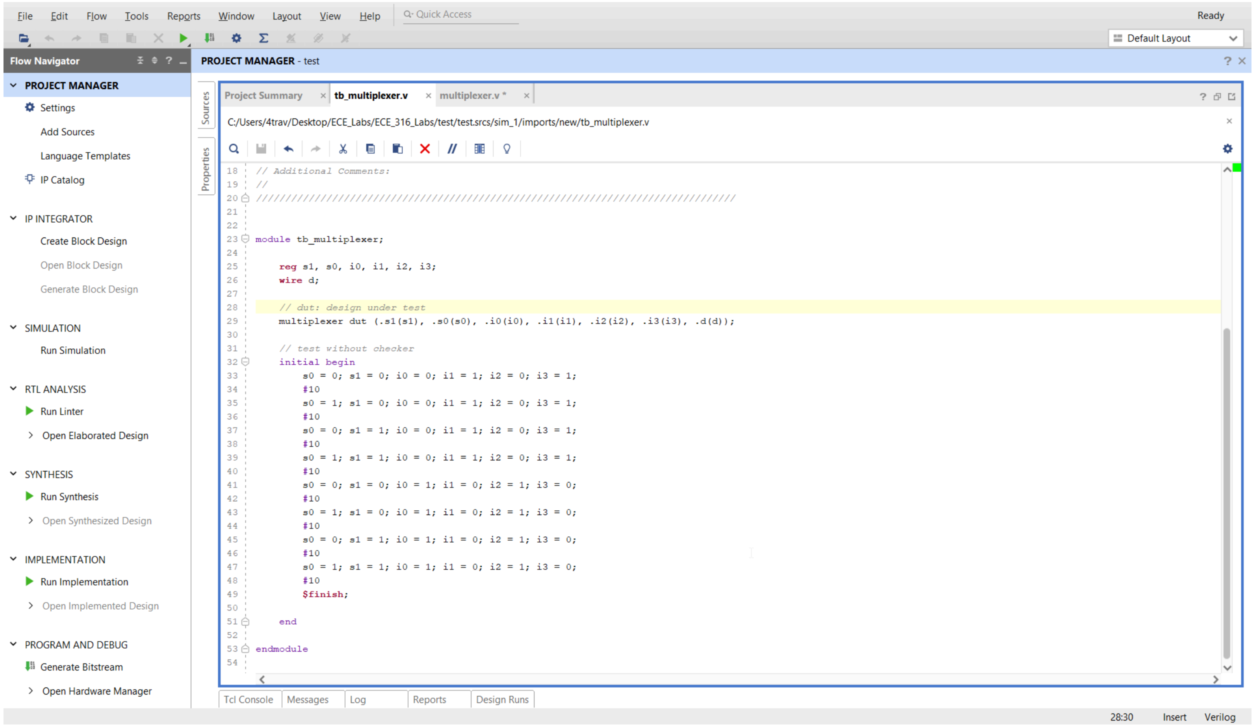


v. Verilog codes for module and testbench for structural modelling



C:/Users/4trav/Desktop/ECE_Labs/ECE_316_Labs/test/test.srcs/sources_1/imports/new/multiplexer.v

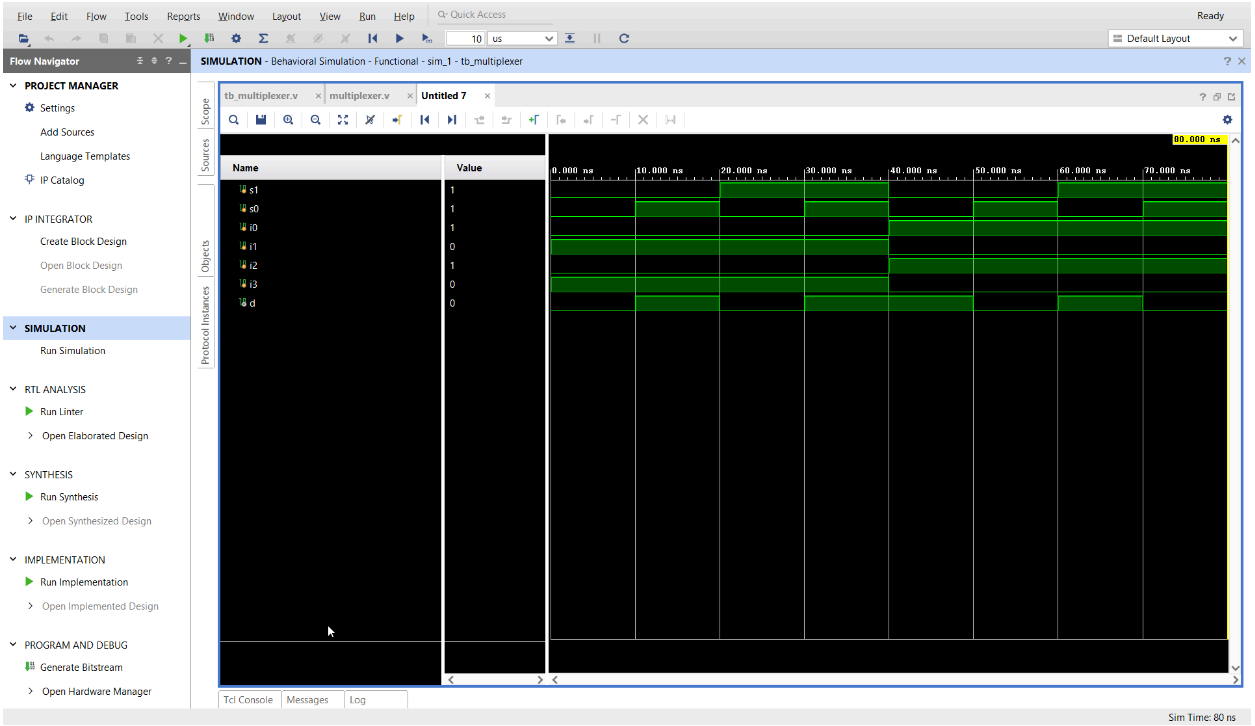
```
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

//// Structural
//module multiplexer(
//    input i0, i1, i2, i3, s0, s1,
//    output d
//);

//    wire nots0, nots1;
//    not int1(nots0, s0);
//    not int2(nots1, s1);
//    wire temp0, temp1, temp2, temp3;
//    and out0 (temp0, nots1, nots0, i0); // 00 = i0
//    and out1 (temp1, nots1, s0, i1); // 01 = i1
//    and out2 (temp2, s1, nots0, i2); // 10 = i2
//    and out3 (temp3, s1, s0, i3); // 11 = i3
//    or outf (d, temp0, temp1, temp2, temp3);

//endmodule

// Behavioral
module decoder(
    input i0, i1, i2, i3, s0, s1,
    output reg d // Declare outputs as reg
);

always @(*) begin

```



C:/Users/4trav/Desktop/ECE_Labs/ECE_316_Labs/test/test.srcs/sim_1/imports/new/tb_multiplexer.v

```verilog
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_multiplexer;

    reg s1, s0, i0, i1, i2, i3;
    wire d;

    // dut: design under test
    multiplexer dut (.s1(s1), .s0(s0), .i0(i0), .i1(i1), .i2(i2), .i3(i3), .d(d));

    // test without checker
    initial begin
        s0 = 0; s1 = 0; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 1; s1 = 0; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 0; s1 = 1; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 1; s1 = 1; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 0; s1 = 0; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 1; s1 = 0; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 0; s1 = 1; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 1; s1 = 1; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        $finish;

    end

endmodule
```

vi. Simulation waveform for structural modelling (Screenshot)

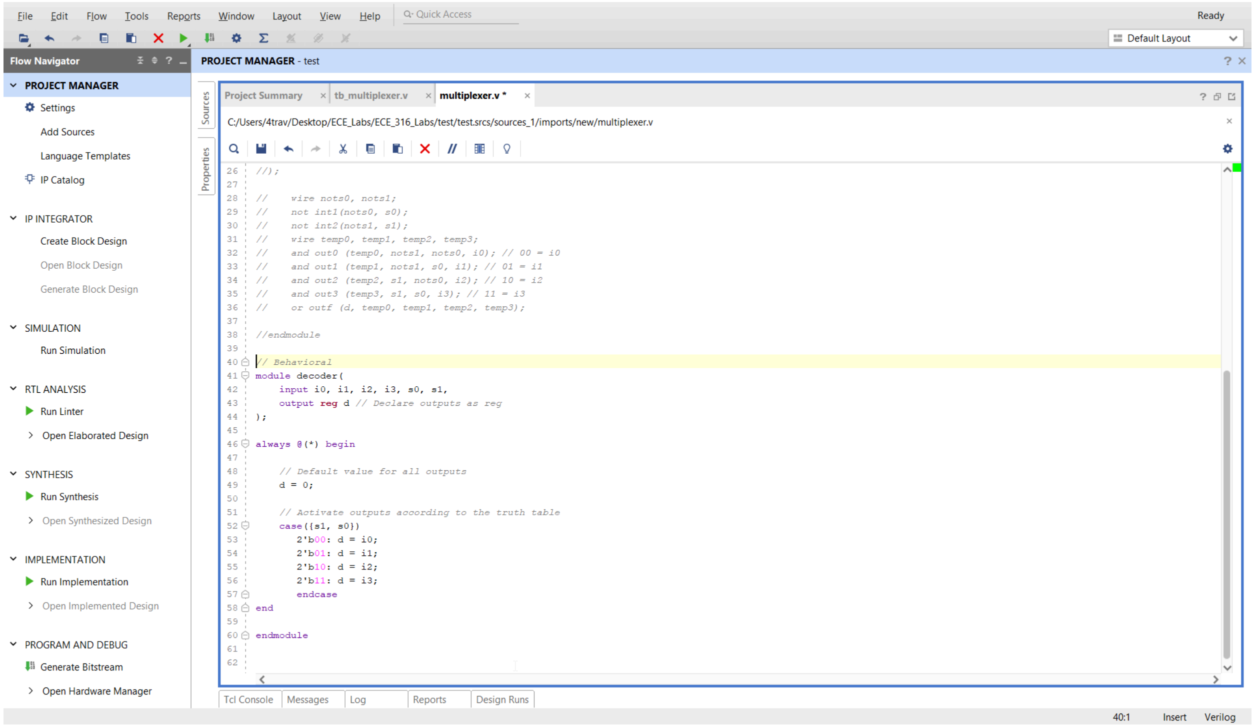


SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_multiplexer

Name	Value
s1	1
s0	1
i0	1
i1	0
i2	1
i3	0
d	0

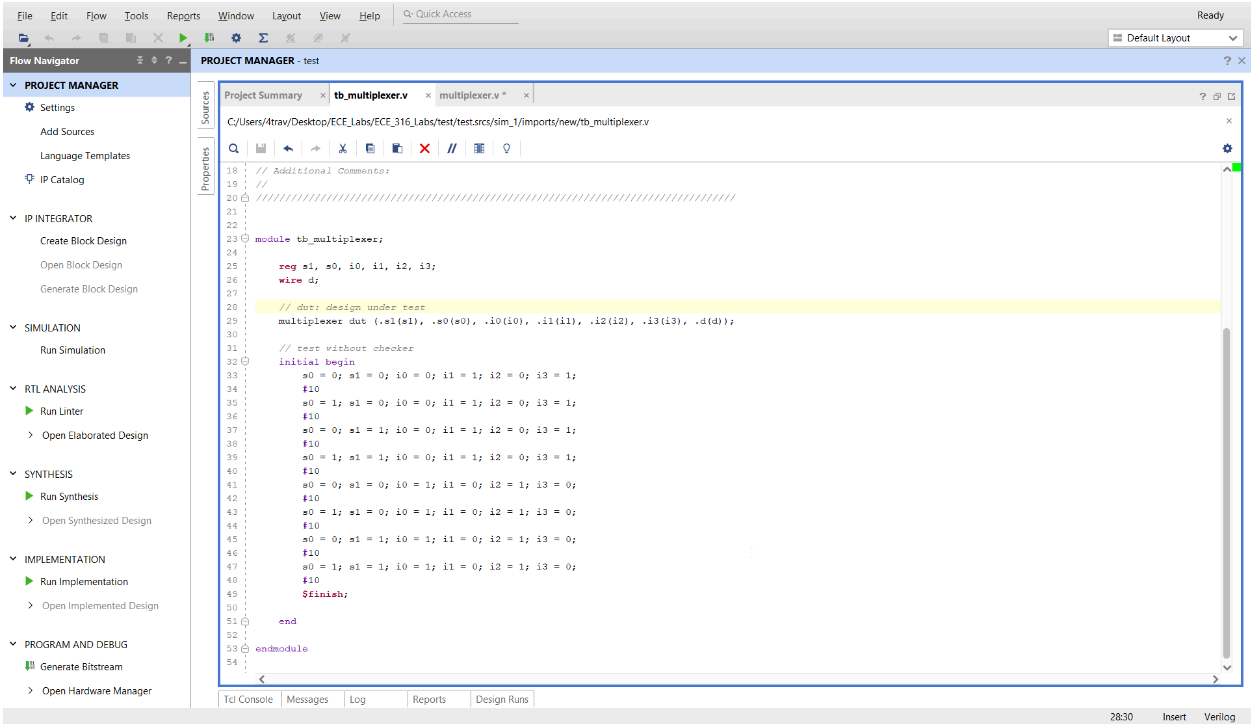
vii. Verilog codes for module and testbench for behavioral modelling

//// Behavioral



C:/Users/4trav/Desktop/ECE_Labs/ECE_316_Labs/test/test.srcs/sources_1/imports/new/multiplexer.v

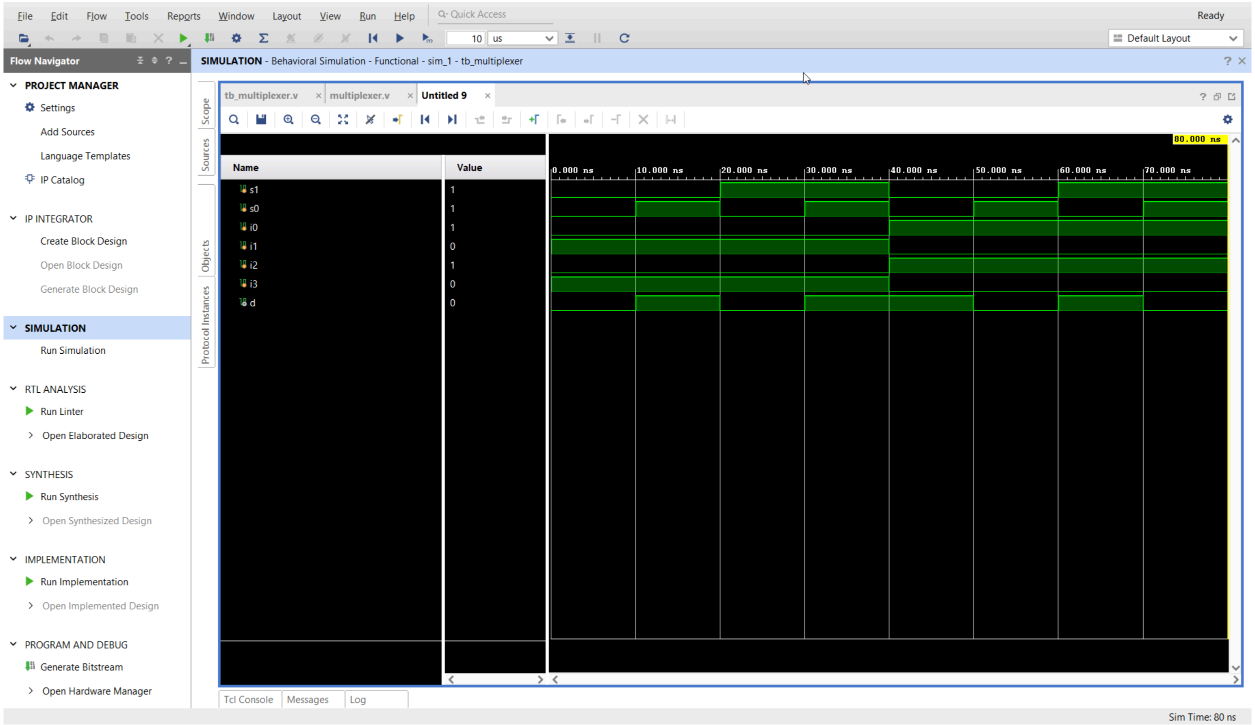
```verilog
//);

//    wire nots0, nots1;
//    not int1(nots0, s0);
//    not int2(nots1, s1);
//    wire temp0, temp1, temp2, temp3;
//    and out0 (temp0, nots1, nots0, i0); // 00 = i0
//    and out1 (temp1, nots1, s0, i1); // 01 = i1
//    and out2 (temp2, s1, nots0, i2); // 10 = i2
//    and out3 (temp3, s1, s0, i3); // 11 = i3
//    or outf (d, temp0, temp1, temp2, temp3);

//endmodule

// Behavioral
module decoder(
    input i0, i1, i2, i3, s0, s1,
    output reg d // Declare outputs as reg
);

always @(*) begin

    // Default value for all outputs
    d = 0;

    // Activate outputs according to the truth table
    case({s1, s0})
       2'b00: d = i0;
       2'b01: d = i1;
       2'b10: d = i2;
       2'b11: d = i3;
       endcase
end

endmodule


```



C:/Users/4trav/Desktop/ECE_Labs/ECE_316_Labs/test/test.srcs/sim_1/imports/new/tb_multiplexer.v

```verilog
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb_multiplexer;

    reg s1, s0, i0, i1, i2, i3;
    wire d;

    // dut: design under test
    multiplexer dut (.s1(s1), .s0(s0), .i0(i0), .i1(i1), .i2(i2), .i3(i3), .d(d));

    // test without checker
    initial begin
        s0 = 0; s1 = 0; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 1; s1 = 0; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 0; s1 = 1; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 1; s1 = 1; i0 = 0; i1 = 1; i2 = 0; i3 = 1;
        #10
        s0 = 0; s1 = 0; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 1; s1 = 0; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 0; s1 = 1; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        s0 = 1; s1 = 1; i0 = 1; i1 = 0; i2 = 1; i3 = 0;
        #10
        $finish;

    end

endmodule

```

viii. Simulation waveform for behavioral modelling (Screenshot)



Name	Value
s1	1
s0	1
i0	1
i1	0
i2	1
i3	0
d	0