

LABORATORY # 1

Combinational Logic Design with Verilog

PART 1 (decoder) Design of Sprinkler Valve Controller

PART 2 (multiplexer) Design of Computer Data Bus

PART 1. Design of a Sprinkler Valve Controller¹

In this guided simulation experiment, we will design and test a 3 x 8 decoder (with “enable” switch) for a sprinkler valve controller system:

Specification

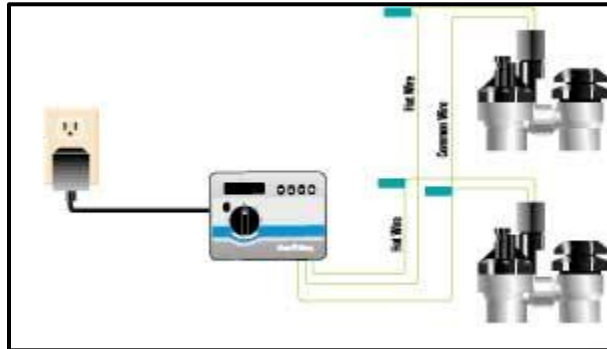


Figure 1. Sprinkler Digital Controller System

Automatic lawn sprinkler systems control the opening and closing of water valves. A sprinkler system must support several different zones, such as the backyard, left side yard, right side yard, etc. **Only one zone’s valve can be opened at a time** to maintain enough pressure in the sprinklers in that zone. In this design assignment, a sprinkler system must support up to 8 zones. Note that typically a sprinkler system is controlled by a small microcontroller unit (MCU) which executes a program that opens each valve only at specific times of the day and for specific durations. However, we will limit ourselves to a sub-project that is dealing only with opening and closing of the valves. The system must also provide a facility to disable the opening of any valve.

Analysis and Design

Assuming a microcontroller has only four output pins, a system based on a 3 x 8 decoder (with “enable” switch) will do the job.

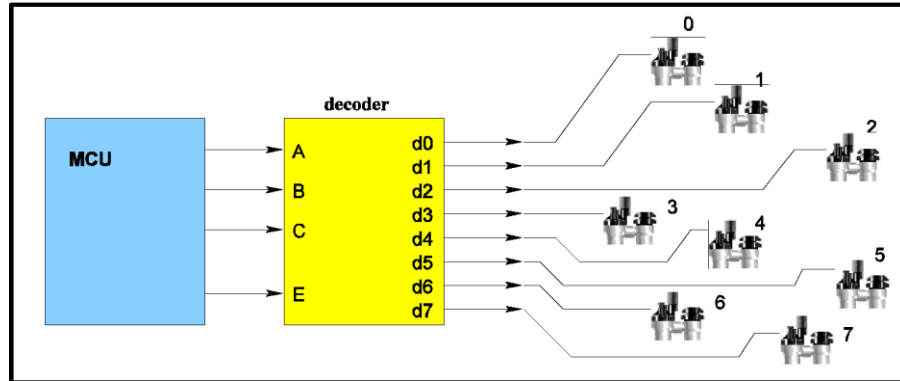


Figure 2. Internal Sprinkler System

MCU has one pin to indicate whether the system is active (enabled) and the other three pins indicate the binary number of the valve to be opened. The system is a combinational logic circuit that has 4 inputs: E (enabler) and A, B, C (the binary value of the active zone), and 8 outputs d7, ..., d0 (the valve controls). The truth table of the system is shown below.

E	A	B	C	d0	d1	d2	d3	d4	d5	d6	d7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Table 1. Truth Table of the Sprinkler System ('x' stands for "don't care")

Following the procedure outlined in zyBook section 1.13, constructing sum-of-products (SOP) minterm based logic expression for each of the data outputs d.

Step 1 – Capture the function.

$$\begin{aligned}
 d0 &= E \cdot A' \cdot B' \cdot C' \\
 d1 &= E \cdot A' \cdot B' \cdot C \\
 d2 &= E \cdot A' \cdot B \cdot C' \\
 d3 &= E \cdot A' \cdot B \cdot C \\
 d4 &= E \cdot A \cdot B' \cdot C' \\
 d5 &= E \cdot A \cdot B' \cdot C \\
 d6 &= E \cdot A \cdot B \cdot C' \\
 d7 &= E \cdot A \cdot B \cdot C
 \end{aligned}$$

Step 2 – Convert to equations and/or minimize.
Nothing to do here (already minimized).

Step 3 – Implement as a gate based logic circuit.
It is shown below using a non-standard² 4-input AND gates and inverters.

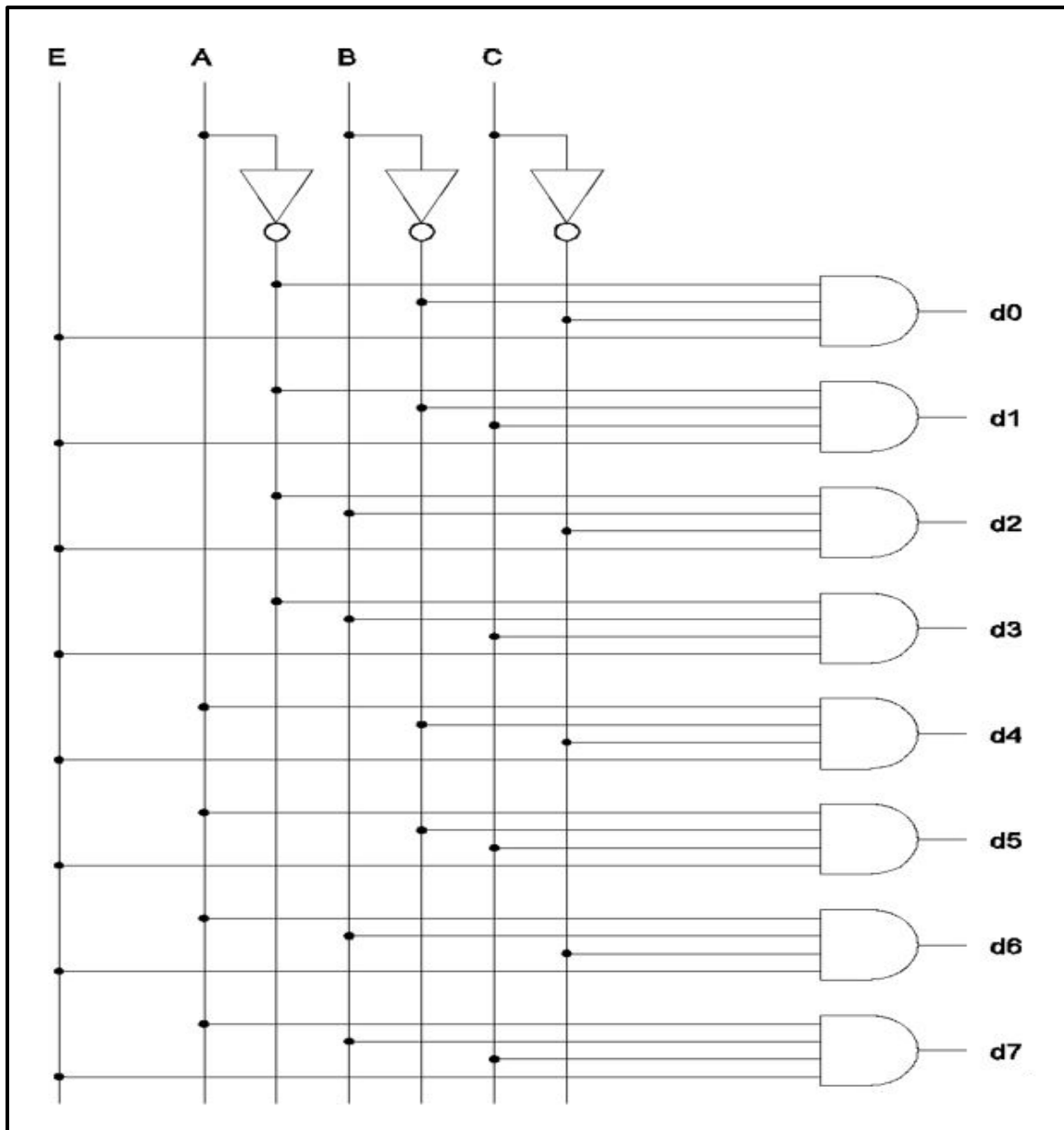


Figure 3. Logic Circuit Schematic of the Sprinkler System based on **Table 1**

² Usage of non-standard gates largely clarifies a circuit schematic, but in many cases requires a creation of a gate library manually within Logic Design Software Environments such as Xilinx Vivado.

Design Entry using Text-Based HDL

Our next task is to implement the design above in Verilog, which is a Hardware Description Language and is used for describing electronic circuits and systems in a text-based manner. There are three ways to model circuits in Verilog as discussed below.

- (i) **Structural Modeling** – This is the gate-level modeling of the circuit. (It most closely resembles the schematic entry and, in a way, replaces a gate symbol with its text-based description.)
- (ii) **Dataflow Modeling** – This is mainly used to describe combinational circuits using the continuous assignment statements. (More on this later).
- (iii) **Behavioral Modeling** – This is the most high-level modeling technique in Verilog and is used for complex circuits, both sequential and combinational. It allows capturing behavior and lets a synthesis tool to automatically translate it into gates (at a later point).

Note -> *The schematic entry has been popular for many years but is no longer practiced for digital gate-level design. HDL-based design entry has replaced it. However, schematics are required to be submitted as part of the lab report.*

In this lab, our task is to model the circuits using structural and behavioral modeling techniques. Since Part 1 is the guided example, all the Verilog codes will be provided for both tasks. For Part 2, you are required to work out the schematic and equations, and model the circuit structurally as well as behaviorally in Verilog.

Part A. Structural Modeling

Step 1 (Creating a new project) – The first step is to create a new project in Vivado. Go to File -> New Project, to open the wizard for new project creation. The wizard will prompt you to enter Project Name (can be named as Lab_2) and location. Project Type can be selected as RTL Project (and check the box stating Do not specify sources at this time). We will be using Basys3 board in this course, and its part number is **XC7A35TCPG236-1**. Hence, this board needs to be selected in the Project menu. Click on Finish to start the new project. The figures below demonstrate the creation of a new project in Xilinx Vivado.

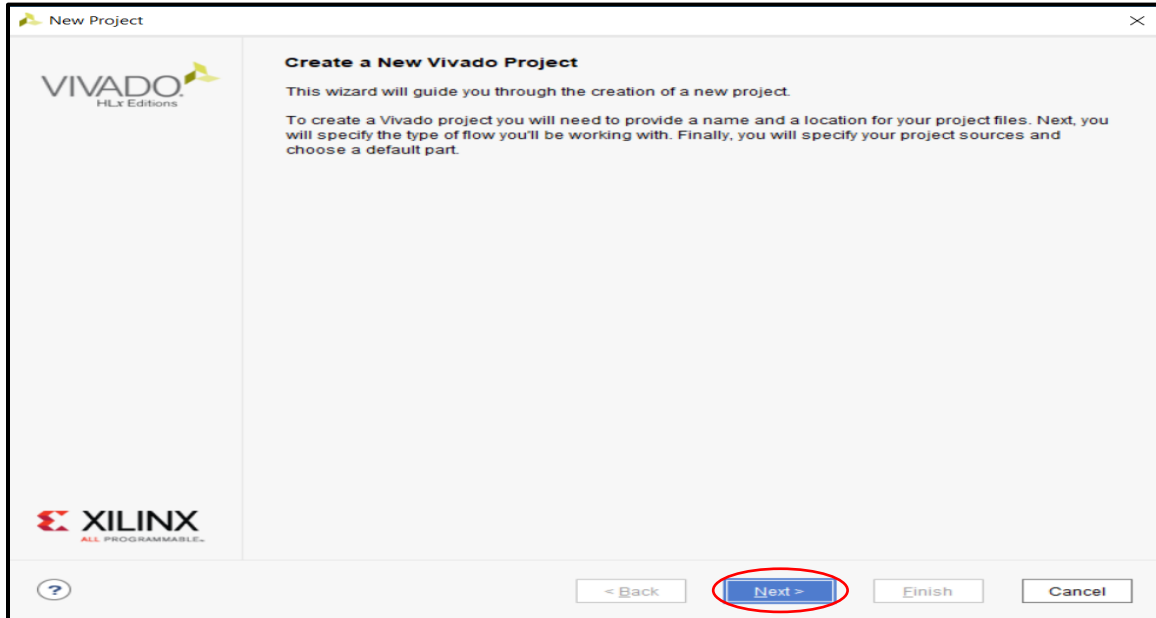


Figure 4. Creating a new project – Step 1

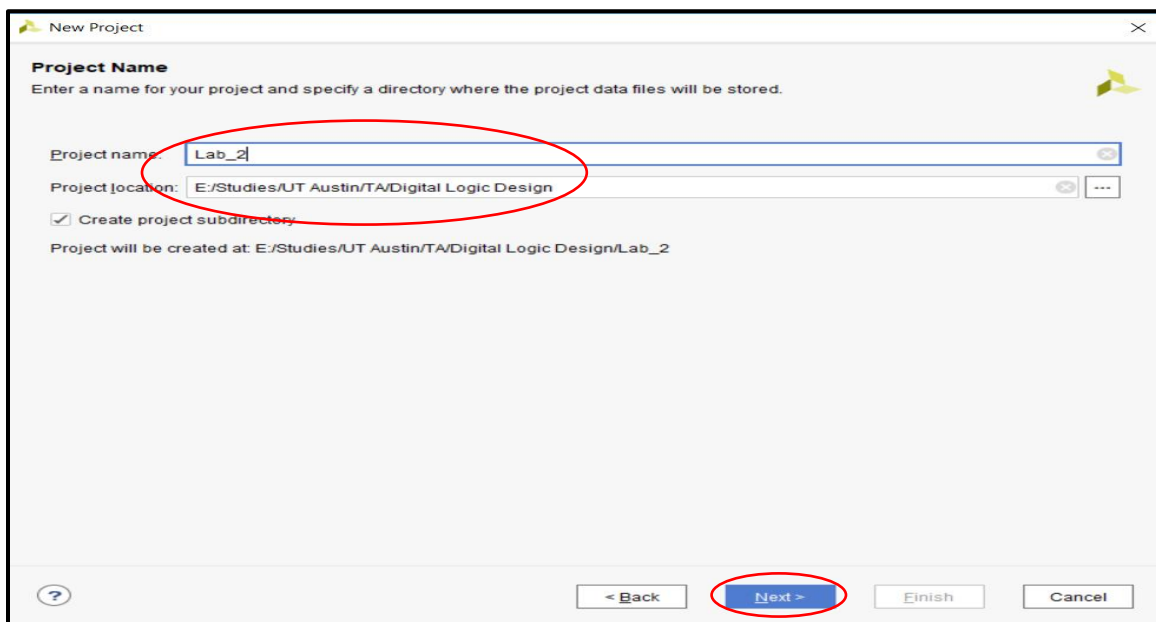


Figure 5. Creating a new project – Step 2

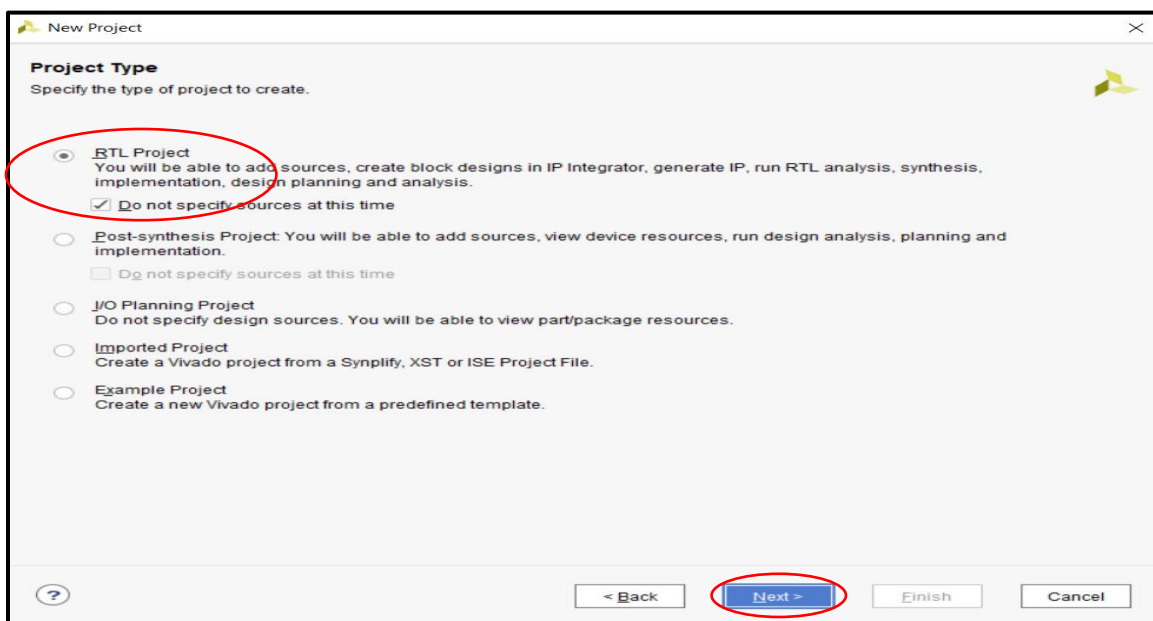


Figure 6. Creating a new project – Step 3

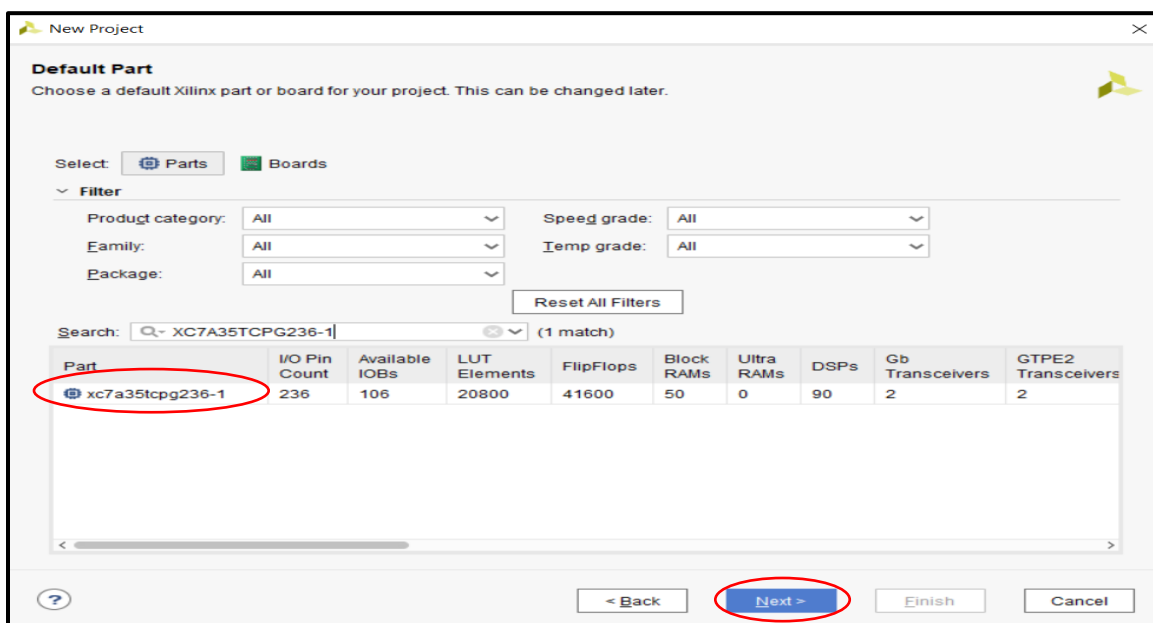


Figure 7. Creating a new project – Step 4

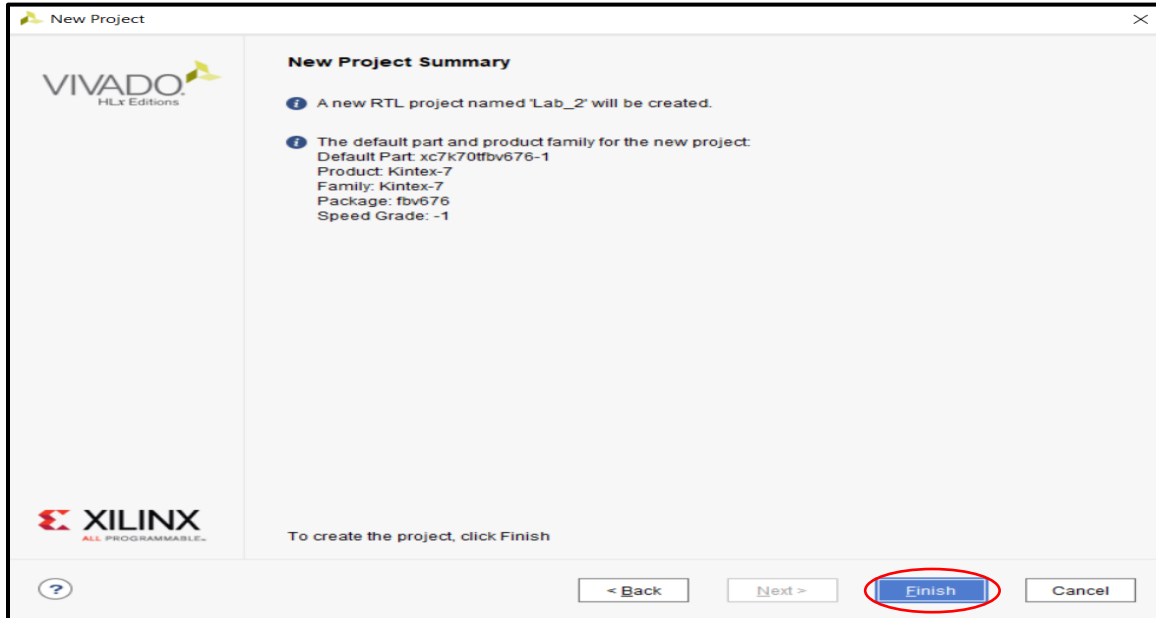


Figure 8. Creating a new project – Step 5

Step 2 (Creating a Verilog file) – The next step is to create the Verilog file for the Decoder module.

1. Click on File -> Add Sources to start creating the Verilog module definition.
2. In the Add Sources wizard, select Add or create design sources and click on Next.
3. Click on Create File option to create the new Verilog file. Select File type as Verilog, and File name can be of your choice, but it is a good practice to keep the File name similar to the name of the top module (for part a, decoder.v). File location should be kept as <Local to Project>. Click on Finish to open the Define Module wizard, where the port definitions of the module are defined.
4. Click on Ok. This will create a Verilog file under the Design Sources tab, which can be opened by double-clicking on it. The steps to create a new Verilog file in the Vivado project are demonstrated in the figures below.

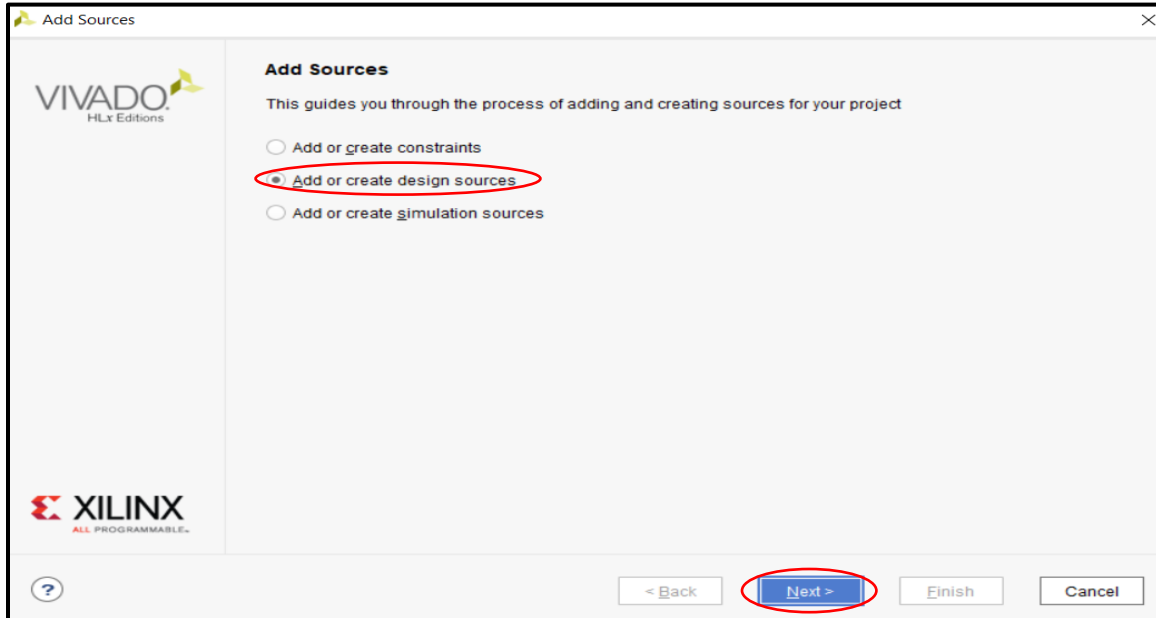


Figure 9. Creating a new Verilog file – Step 1

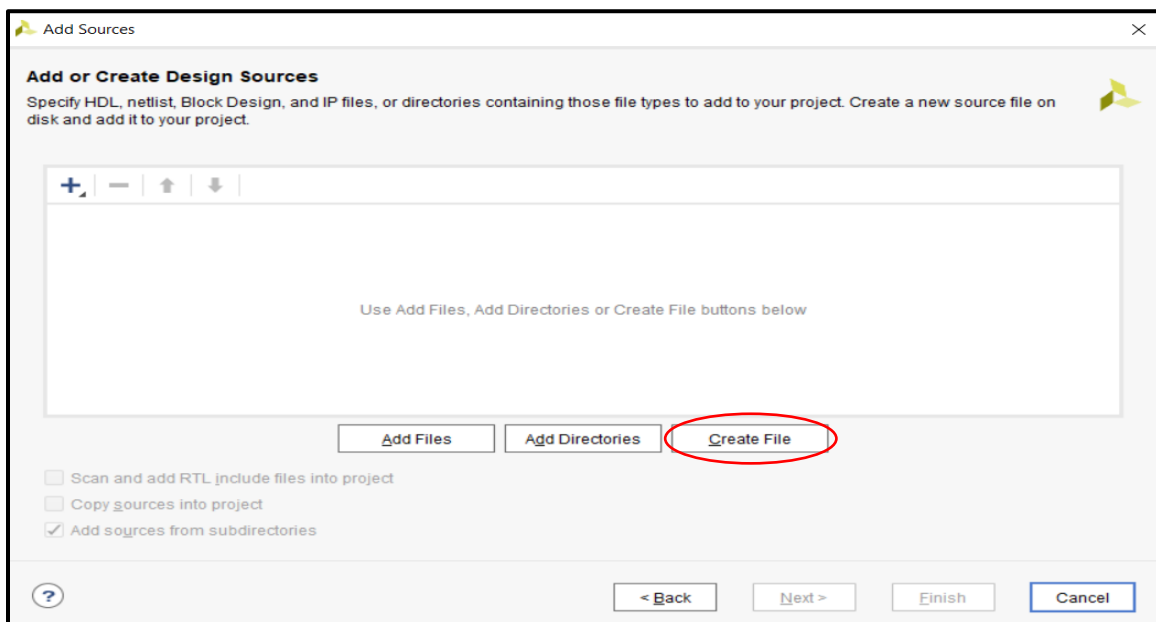


Figure 10. Creating a new Verilog file – Step 2

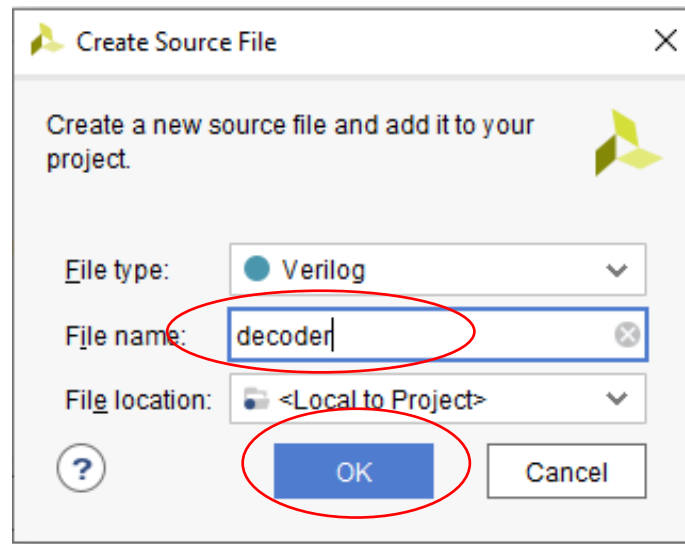


Figure 11. Creating a new Verilog file – Step 3.

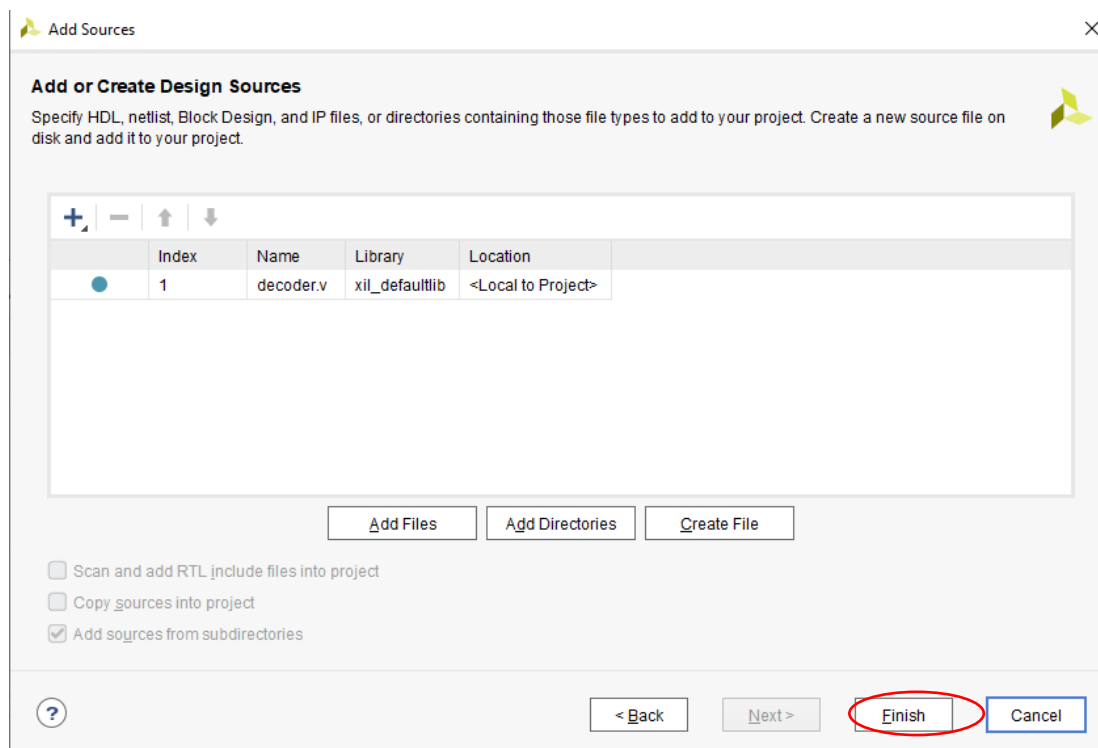


Figure 12. Creating a new Verilog file – Step 4

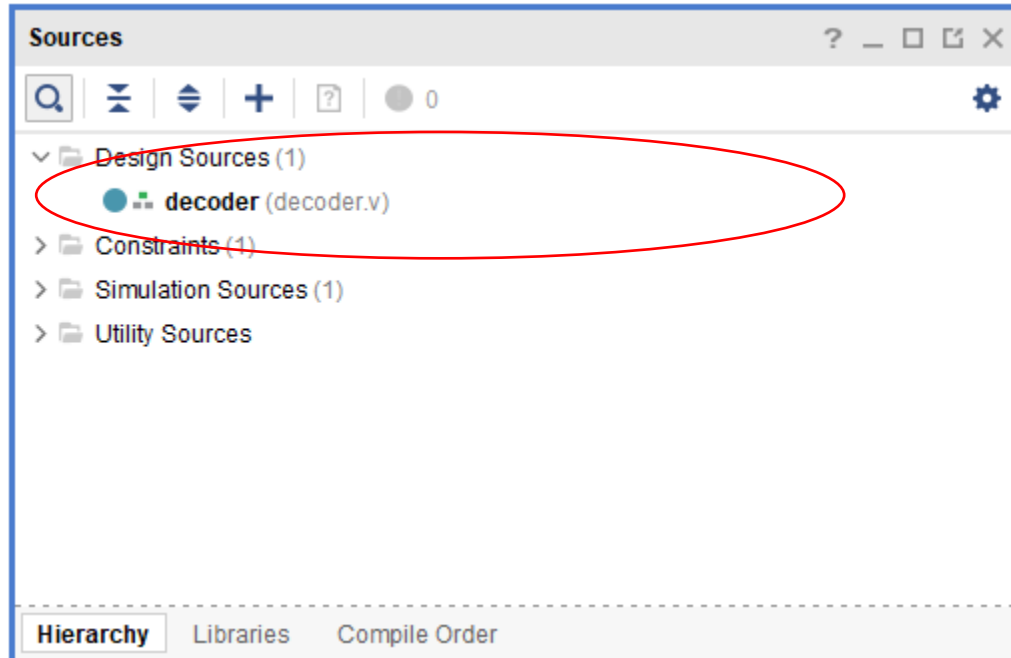


Figure 13. Newly created Verilog file – appearing in Design Sources

Step 3 (Writing Verilog Code) – Now, the Verilog code of the module needs to be written in the generated file. The code of the Decoder module is provided on Canvas and can be copied to the generated file.

Step 4 (Creating a Verilog Testbench) – A testbench is used to verify the correctness of the circuit by giving the stimulus (various input combinations) and checking for the output. For smaller circuits, it is good to perform “*exhaustive*” circuit testing, i.e., testing the circuit for all possible input combinations and this will be done for both circuits in this lab.

1. To open a Verilog testbench file, go to File -> Add Sources. In the wizard, select Add or create simulation sources option and click Next.
2. Now, click on the Create File button and give any File name. (A good practice is to name the testbench files as tb_<Module_name>).
3. Click on Finish to open the Define Module window
4. Double click on the file (which will be present under the Simulation Sources tab) to open it. The steps to create a new Verilog testbench file are demonstrated in the figures below.

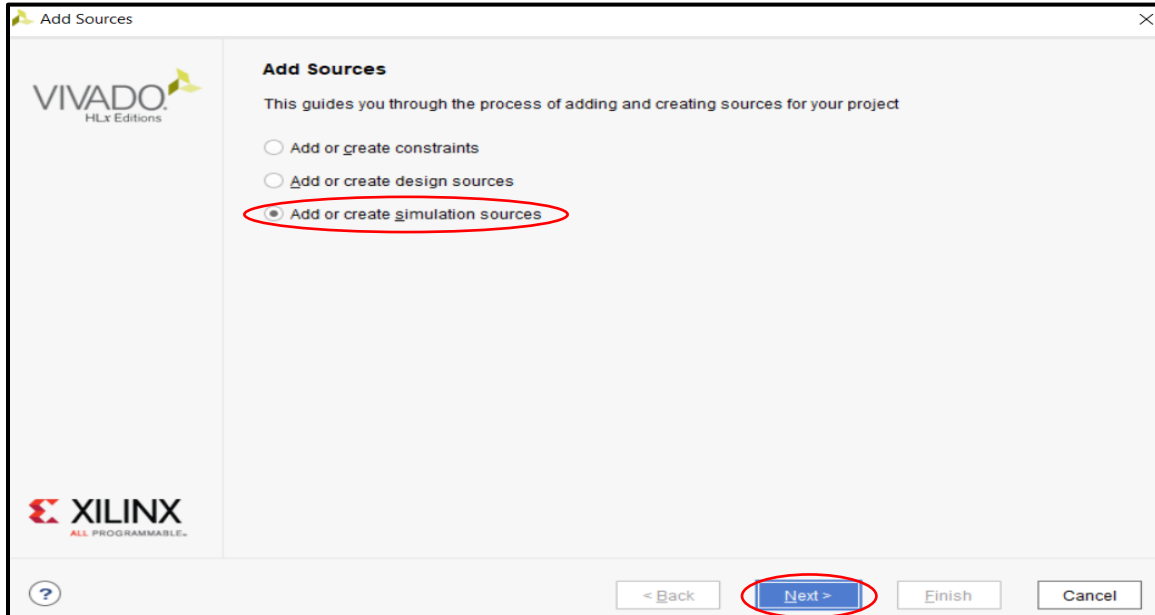


Figure 14. Creating a new Verilog testbench – Step 1

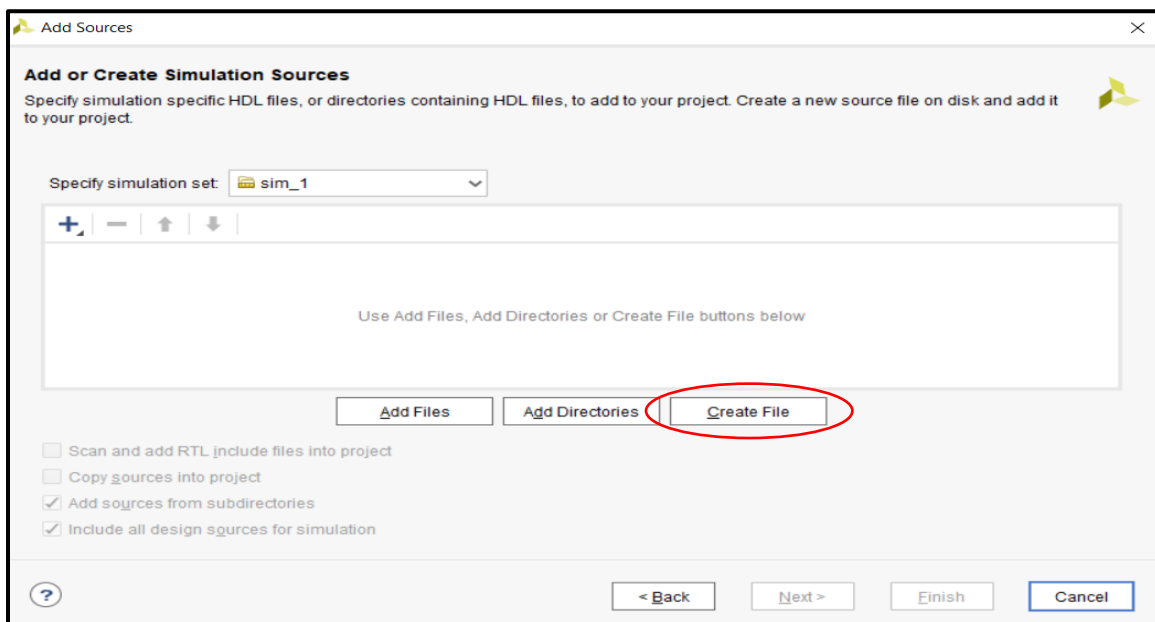


Figure 15. Creating a new Verilog testbench – Step 2

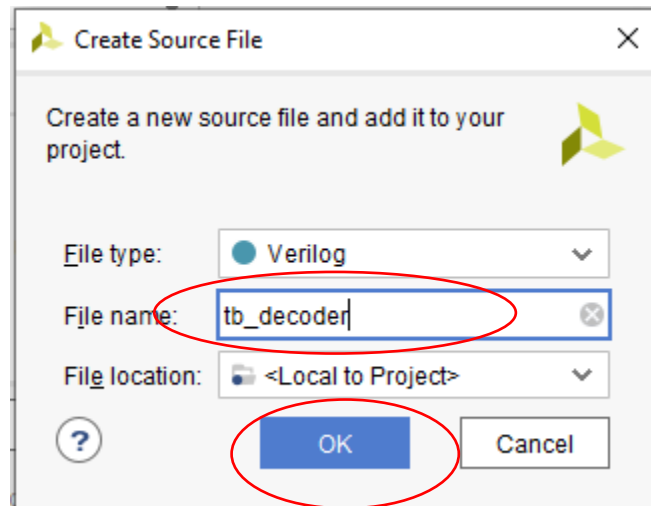


Figure 16. Creating a new Verilog testbench – Step 3

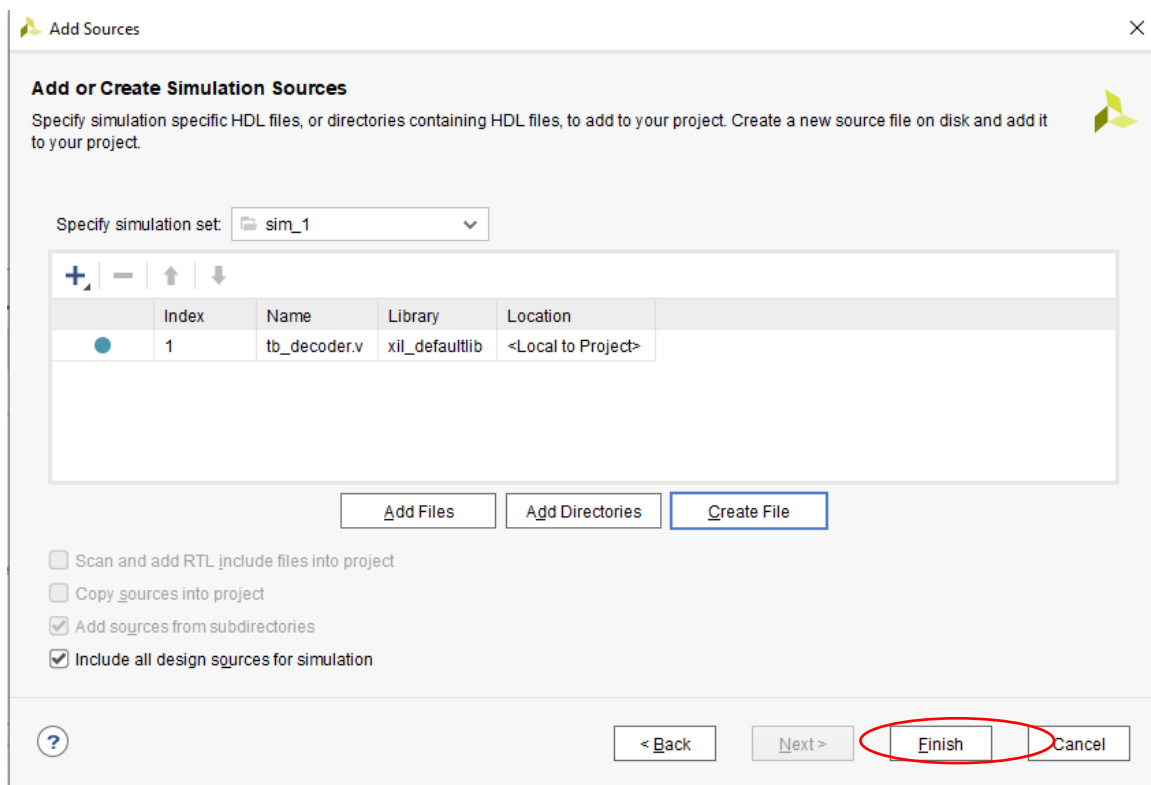


Figure 17. Creating a new Verilog testbench – Step 4

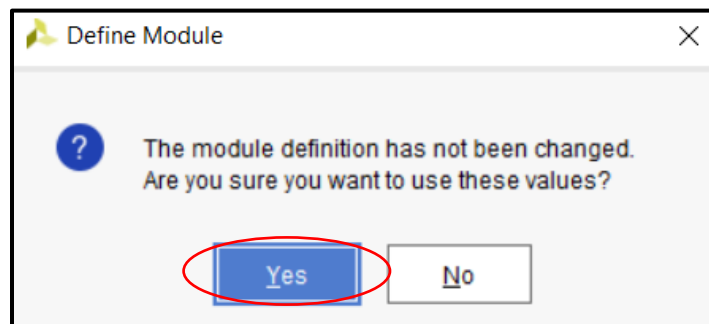


Figure 18. Creating a new Verilog testbench – Step 5

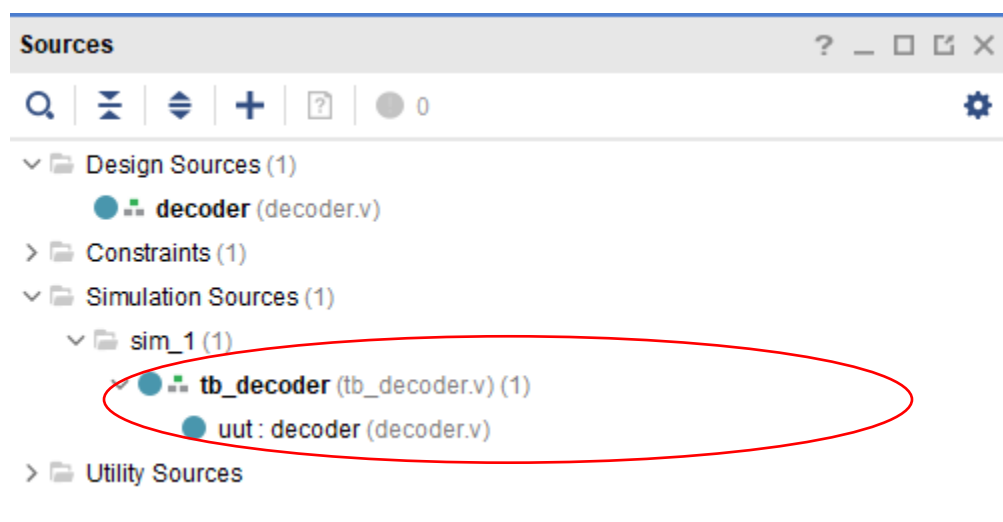


Figure 19. Newly created Verilog testbench – appearing in Simulation Sources

Step 5 (Writing Verilog Testbench) – Now, the Verilog testbench needs to be written for the design verification. The code of the testbench is provided on Canvas and can be copied into your *tb_decoder.v* file.

Step 6 (Circuit Simulation and Verification) – The next step is to simulate the testbench created in the previous step and verify the functionality of the circuit. Select the *Run Simulation* option in the left pane and select *Run Behavioral Simulation* from the drop-down menu. A simulation waveform window will come up, and the messages in \$display statements in the testbench will come on the Tcl console. On the simulation window, click on the Zoom fit icon to fit the simulation waveform on the screen. Other options in the menu can be explored as well. Also, different signals can be put on the waveform, by right clicking on the signal names in the Scope and Objects panes.

Note –> If your computer has an active anti-virus program, it may be required to turn that off before simulation can be done.

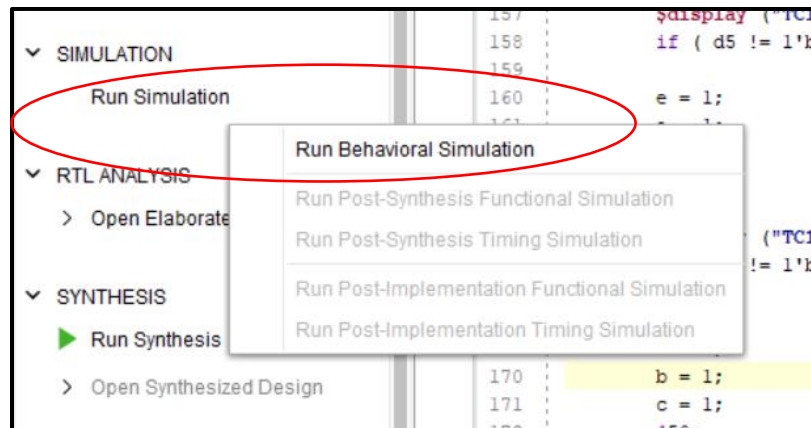


Figure 20. Running Simulation

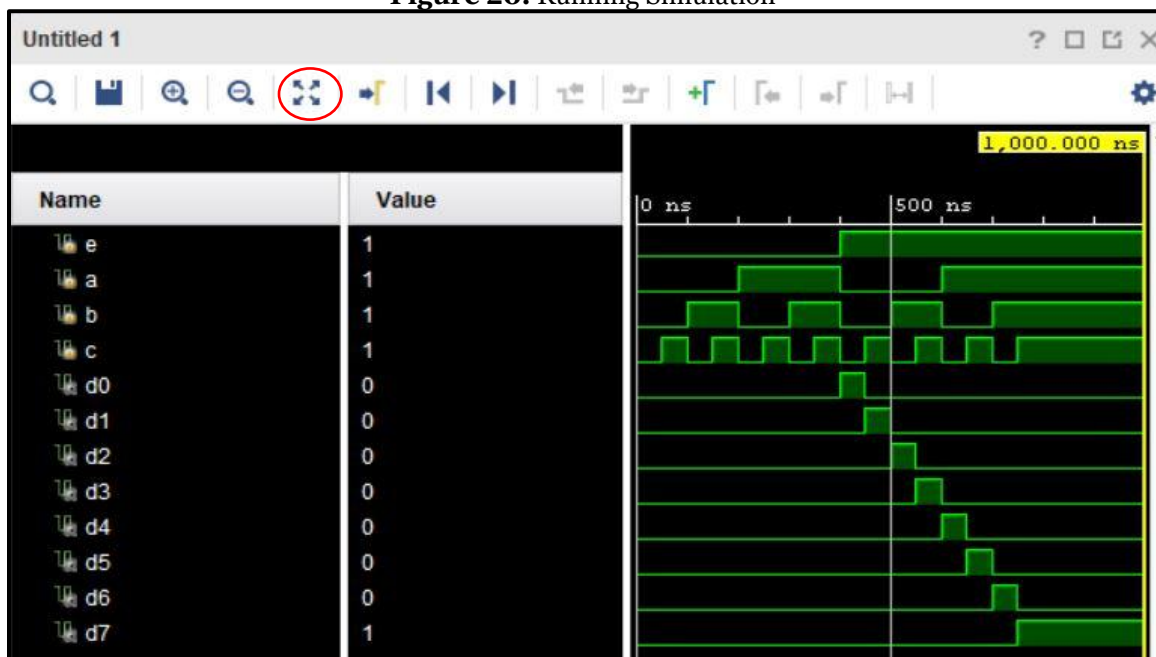


Figure 21. Behavioral Simulation of Sprinkler Controller Circuit

The sequence of input and output signals can be re-arranged by pressing and holding the signal line and moving it up or down. Also, signals can be grouped by selecting the signals to be grouped, right clicking and selecting New Group.

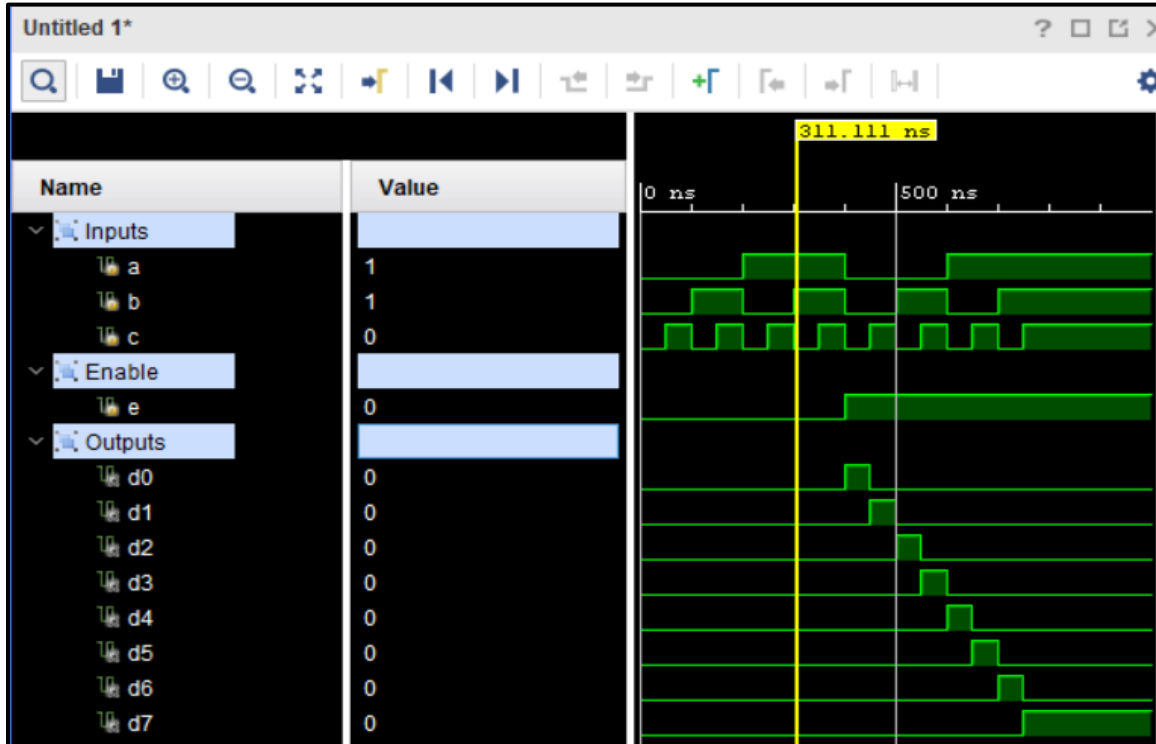


Figure 22. Behavioral Simulation Waveform Window with Inputs, Outputs and Enable grouped

It should be noted from the simulation that when the enable is '0', none of the outputs is '1' (meaning that all the valves are closed), but when enable is '1', only one of the outputs is '1' based on the input combination, thus ensuring that only one valve is open at a time as required.

A lot of other customizations like adding cursors, running the simulation for more time, changing signal colors, etc. be done from the waveform window options. It is highly recommended to explore the various options available, as they might be helpful in the future labs. However, for this lab, only the simulation waveforms are required to be submitted.

For closing the simulation, right click on the Simulation tab in the left pane and click on Close Simulation.

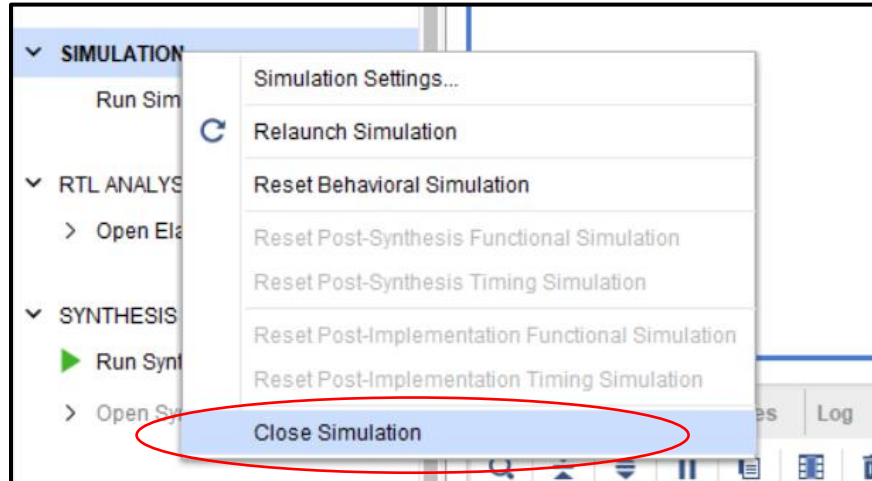


Figure 23. Option to close the simulation

Part B. Behavioral Modeling

In this part, the same decoder circuit will be modeled using the behavioral modeling technique. The code for the module is also provided on Canvas, and the simulation is required to be done following the same steps listed above. **(Comment the structural modeling code and uncomment the behavioral modeling code)**

Note -> *It should be noted that the behavioral modeling in this part is done using case statements, which is just one way to model the circuits behaviorally. There are other ways which can be used to model the circuits behaviorally (for example, using “if” statements only).*

Since the functionality of the decoder is the same no matter how it is modeled (structurally or behaviorally), **the same set of stimuli developed in Part A** can be used to test the behaviorally modeled testbench as well. Also, we expect to obtain the same simulation waveforms as Part A, since the functionality of the circuit remains the same.

PART 2. Design of Computer Data Bus

In this assignment, we will design a 4 x 1 multiplexer that will control the flow of data in a single wire data bus and study its basic properties. This technology allows to accomplish, for example, partial serial communication with multiple peripheral devices using just one output pin of a microcontroller.

Specification

Design a 1-wire data bus controller that performs the following function:

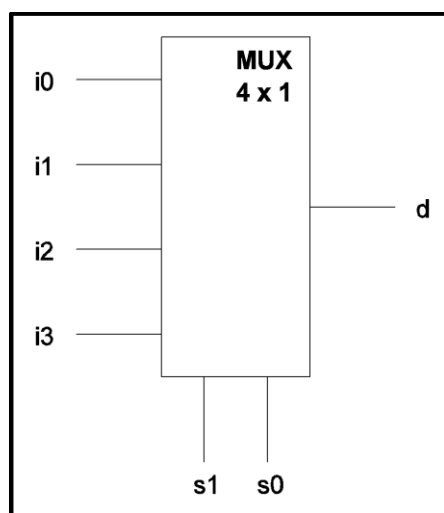


Figure 24. Single-wire data bus multiplexer

Inputs s_0, s_1 control which of the input data i_0, i_1, i_2, i_3 is present in the output d , where the binary s_1, s_0 represents the input pin number.

Example: $s_1, s_0 = 1, 0$ indicates that data in the input line i_2 appear in the output d .

Design a logic circuit that will perform this function and verify the logic functionality using Xilinx Vivado software environment.

As done in Part 1, the design needs to be modeled **structurally as well as behaviorally** and both the modules need to be tested using the testbenches .

The testbench should contain at least 8 cases. **Please follow these steps to build the testbench:**

1. Set i_3, i_2, i_1, i_0 to any values except 0000 and 1111.
2. Switch s_1, s_0 through all combinations from 00 to 11.
3. Set i_3, i_2, i_1, i_0 to a different value, excluding 0000 and 1111.
4. Switch s_1, s_0 through all combinations from 00 to 11 again.

Demonstration and Lab Report

During the lab hour, all the simulation waveforms need to be presented to the TAs with the correct explanation of why they are correct.

For Part 1, **all the simulation waveforms** should be submitted as part of the lab report.

For Part 2, **the truth table, algebraic expression of the logic function**, logic circuit **schematic**, Verilog **code for modules and testbenches** for both structural and behavioral modeling, and **simulation waveforms** for both structural and behavioral modeling should be submitted as part of the lab report.