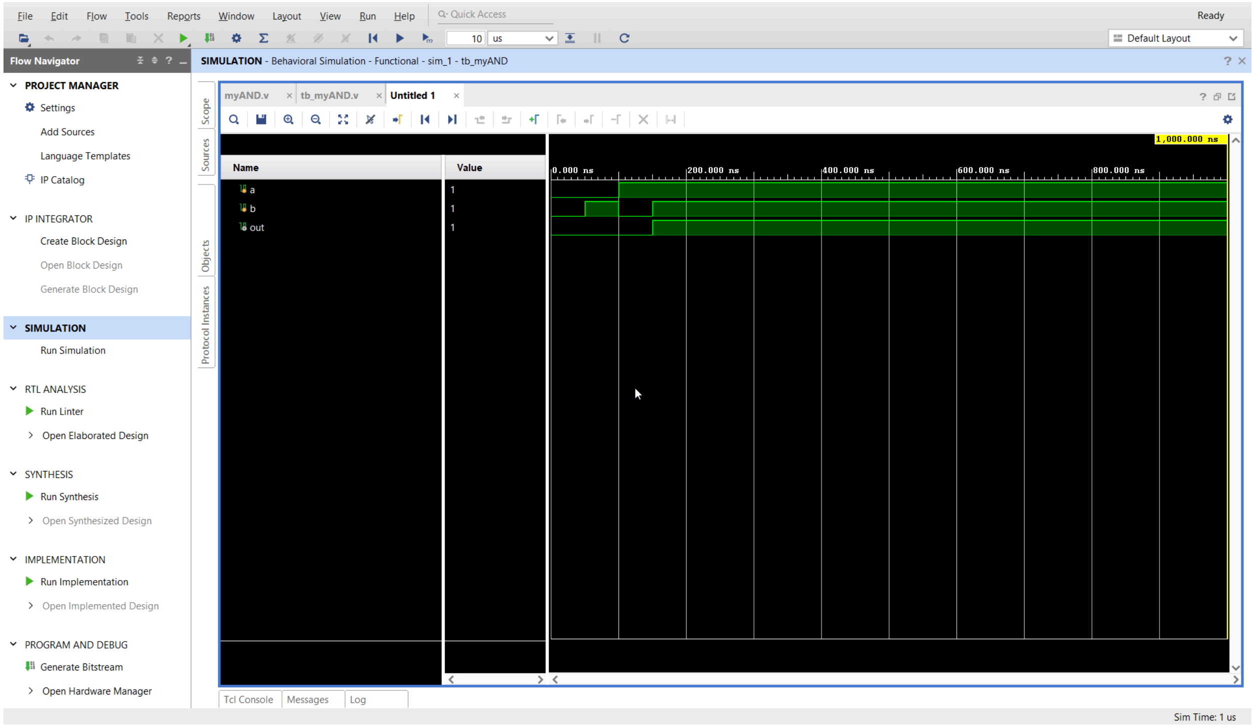
Part 1

i. Simulation of AND gate:



Name	Value
a	1
b	1
out	1

ii. Constraint File

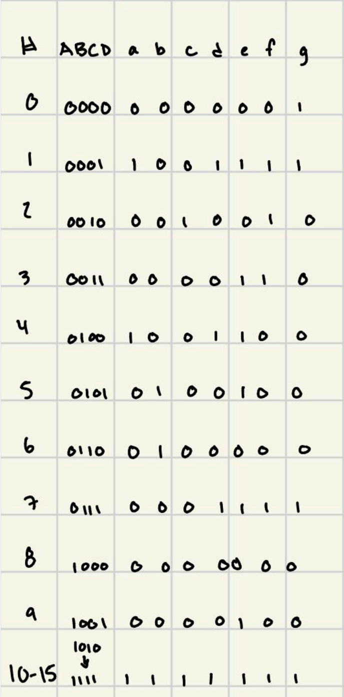
```
## Switches
## Connects pin V17 (SW0 on the board) to input b in our gate module
set_property PACKAGE_PIN V17 [get_ports {b}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]

## Connects pin V16 (SW1 on the board) to input a in our gate module
set_property PACKAGE_PIN V16 [get_ports {a}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]

#Deleted extra switches to fit in one screenshot

## LEDs
## Connects the output out in our gate module to pin U16 (LED0 on-board)
set_property PACKAGE_PIN U16 [get_ports {out}]
## Sets the LED to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {out}]
```

Part 2
iii. Constraints

```
## Switches
## Connects pin V17 (SW0 on the board) to input C in our gate module
set_property PACKAGE_PIN V17 [get_ports {c}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
## Connects pin V16 (SW1 on the board) to input b in our gate module
set_property PACKAGE_PIN V16 [get_ports {b}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
## Connects pin W16 (SW2 on the board) to input a in our gate module
set_property PACKAGE_PIN W16 [get_ports {a}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
## Connects pin W13 (SW7 on the board) to input e in our gate module
set_property PACKAGE_PIN W13 [get_ports {e}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]

  ## LEDs
## Connects the output d0 in our gate module to pin U16 (LED0 on-board)
set_property PACKAGE_PIN U16 [get_ports {d0}]
## Sets the LED to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
set_property PACKAGE_PIN E19 [get_ports {d1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN U19 [get_ports {d2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN V19 [get_ports {d3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN W18 [get_ports {d4}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN U15 [get_ports {d5}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN U14 [get_ports {d6}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN V14 [get_ports {d7}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
```

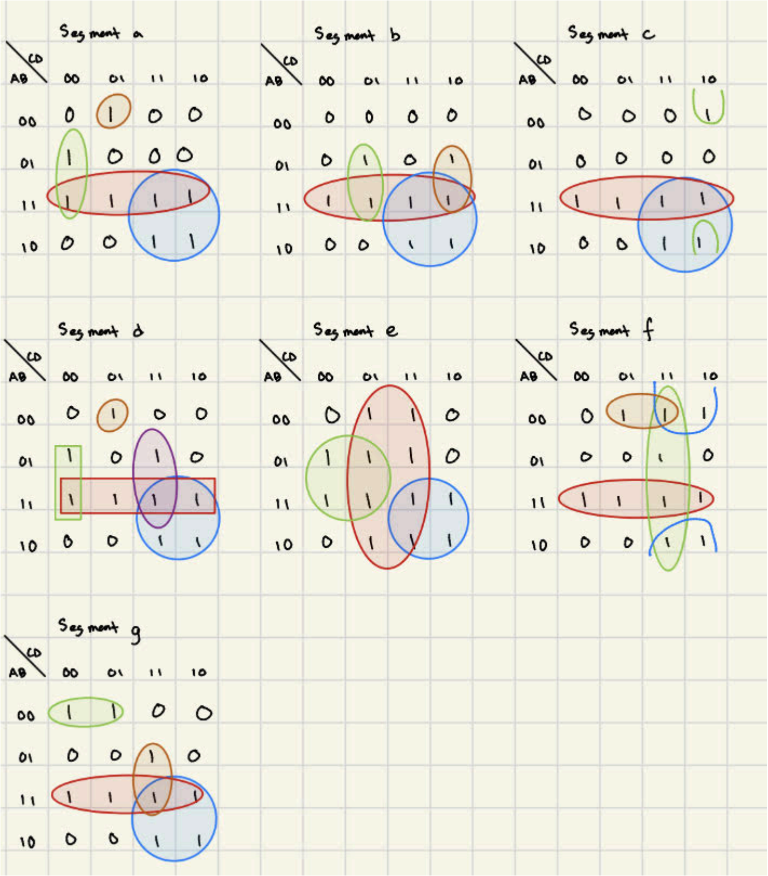
Part 3

iv. Truth Table



#	ABCD	a	b	c	d	e	f	g
0	0000	0	0	0	0	0	0	1
1	0001	1	0	0	1	1	1	1
2	0010	0	0	1	0	0	1	0
3	0011	0	0	0	0	1	1	0
4	0100	1	0	0	1	1	0	0
5	0101	0	1	0	0	1	0	0
6	0110	0	1	0	0	0	0	0
7	0111	0	0	0	1	1	1	1
8	1000	0	0	0	0	0	0	0
9	1001	0	0	0	0	1	0	0
10-15	1010 ↓ 1111	1	1	1	1	1	1	1

v. K-Maps



Segment a

AB \ CD	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	1	1	1	1
10	0	0	1	1

Segment b

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	1	1	1
10	0	0	1	1

Segment c

AB \ CD	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

Segment d

AB \ CD	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	1	1	1	1
10	0	0	1	1

Segment e

AB \ CD	00	01	11	10
00	0	1	1	0
01	1	1	1	0
11	1	1	1	1
10	0	1	1	1

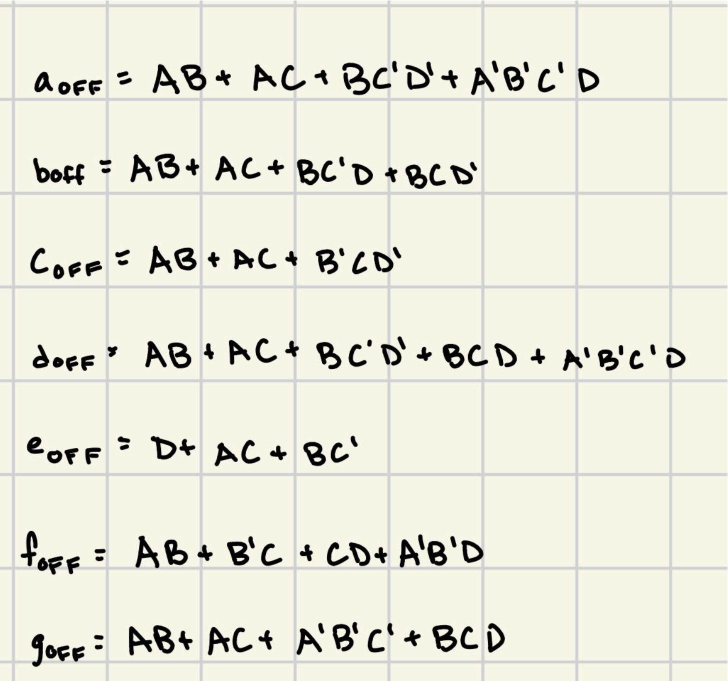
Segment f

AB \ CD	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	1	1	1	1
10	0	0	1	1

Segment g

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	1	1	1
10	0	0	1	1

vi. Equation



$$a_{OFF} = AB + AC + BC'D' + A'B'C'D$$

$$b_{off} = AB + AC + BC'D + BCD'$$

$$c_{OFF} = AB + AC + B'CD'$$

$$d_{OFF} = AB + AC + BC'D' + BCD + A'B'C'D$$

$$e_{OFF} = D + AC + BC'$$

$$f_{OFF} = AB + B'C + CD + A'B'D$$

$$g_{OFF} = AB + AC + A'B'C' + BCD$$

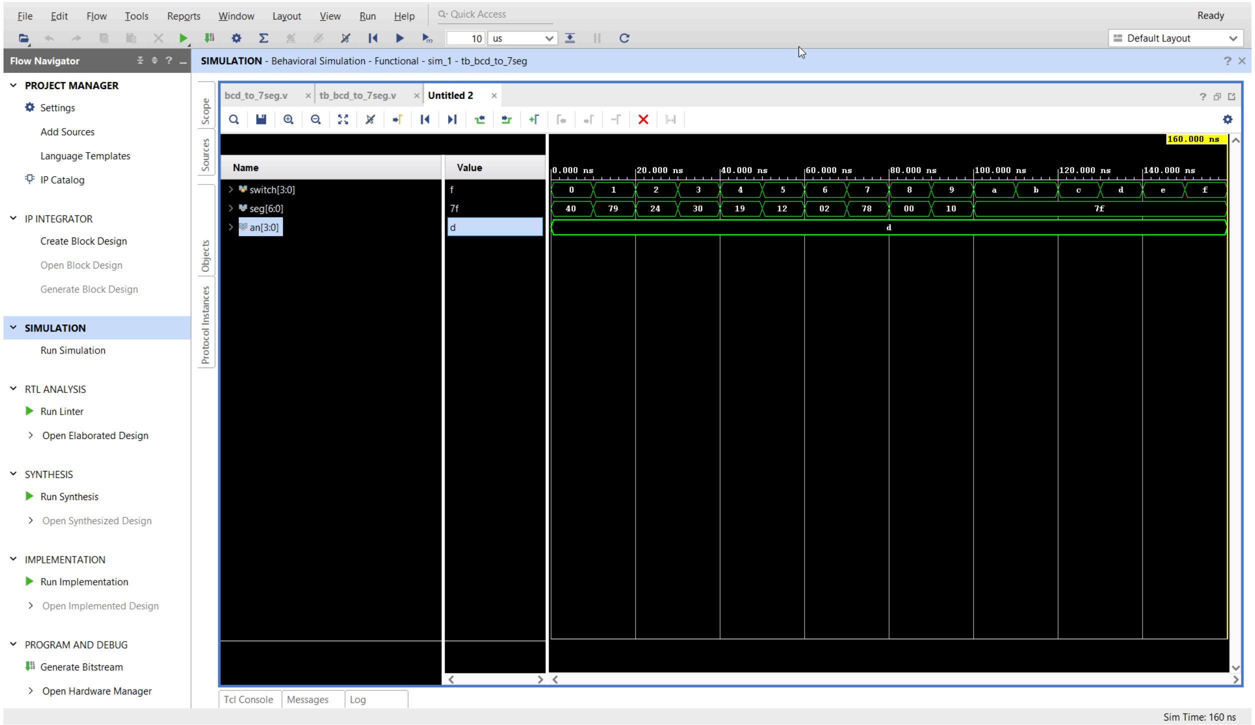
vii. Module and Testbench

```
module bcd_to_7seg(
    input [3:0] switch,   // switch[3] is A, ..., switch[0] is D
    output [6:0] seg,     // seg[0] is a, ..., seg[6] is g
    output [3:0] an       // Anodes
    );

    // not inputs
    wire An, Bn, Cn, Dn;
    not (An, switch[3]); // switch[3] = A
    not (Bn, switch[2]); // switch[2] = B
    not (Cn, switch[1]); // switch[1] = C
    not (Dn, switch[0]); // switch[0] = D

    // turn on only the one digit
    assign an = 4'b1101;

    // seg a
    wire a1, a2, a3, a4;
    and (a1, switch[3], switch[2]);          // AB
    and (a2, switch[3], switch[1]);          // AC
    and (a3, An, Bn, Cn, switch[0]);          // A'B'C'D
    and (a4, switch[2], Cn, Dn);             // BC'D'
    or  (seg[0], a1, a2, a3, a4);
```

```
// seg b
wire b1, b2, b3, b4;
and (b1, switch[3], switch[2]);          // AB
and (b2, switch[3], switch[1]);          // AC
and (b3, switch[2], Cn, switch[0]);      // BC'D
and (b4, switch[2], switch[1], Dn);      // BCD'
or  (seg[1], b1, b2, b3, b4);

// seg c
wire c1, c2, c3;
and (c1, switch[3], switch[2]);          // AB
and (c2, switch[3], switch[1]);          // AC
and (c3, Bn, switch[1], Dn);             // B'CD'
or  (seg[2], c1, c2, c3);

// seg d
wire d1, d2, d3, d4, d5;
and (d1, switch[3], switch[2]);          // AB
and (d2, switch[3], switch[1]);          // AC
and (d3, switch[2], Cn, Dn);             // BC'D'
and (d4, switch[2], switch[1], switch[0]); // BCD
and (d5, An, Bn, Cn, switch[0]);         // A'B'C'D
or  (seg[3], d1, d2, d3, d4, d5);

// seg e
wire e1, e2;
and (e1, switch[3], switch[1]);          // AC
and (e2, switch[2], Cn);                 // BC'
or  (seg[4], switch[0], e1, e2);         // D + AC + BC'

// seg d
wire f1, f2, f3, f4;
and (f1, switch[3], switch[2]);          // AB
and (f2, Bn, switch[1]);                 // B'C
and (f3, switch[1], switch[0]);          // CD
and (f4, An, Bn, switch[0]);             // A'B'D
or  (seg[5], f1, f2, f3, f4);

// seg g
wire g1, g2, g3, g4;
and (g1, switch[3], switch[2]);          // AB
and (g2, switch[3], switch[1]);          // AC
and (g3, An, Bn, Cn);                    // A'B'C'
```

```
    and (g4, switch[2], switch[1], switch[0]); // BCD
    or  (seg[6], g1, g2, g3, g4);

endmodule


module tb_bcd_to_7seg;

    // inputs and outputs
    reg [3:0] switch;
    wire [6:0] seg;
    wire [3:0] an;

    bcd_to_7seg dut (.switch(switch), .seg(seg),.an(an));

    // test
    initial begin

        switch = 4'b0000;
        #10;
        switch = 4'b0001;
        #10;
        switch = 4'b0010;
        #10;
        switch = 4'b0011;
        #10;
        switch = 4'b0100;
        #10;
        switch = 4'b0101;
        #10;
        switch = 4'b0110;
        #10;
        switch = 4'b0111;
        #10;
        switch = 4'b1000;
        #10;
        switch = 4'b1001;
        #10;
        switch = 4'b1010;
        #10;
        switch = 4'b1011;
        #10;
        switch = 4'b1100;
        #10;
        switch = 4'b1101;
        #10;
        switch = 4'b1110;
        #10;
        switch = 4'b1111;
        #10;

        $finish;
    end

endmodule
```

viii. Simulation



SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_bcd_to_7seg

```
Name          Value
switch[3:0]   f
seg[6:0]      7f
an[3:0]       d

160.000 ns
0.000 ns  20.000 ns  40.000 ns  60.000 ns  80.000 ns  100.000 ns  120.000 ns  140.000 ns
switch: 0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
seg:    40 79 24 30 19 12 02 78 00 10 7f
an:     d
```

Sim Time: 160 ns

ix. Constraints

```
## Switches
## Connects pin V17 (SW0 on the board) to input D (on switch 0) in our gate module
set_property PACKAGE_PIN V17 [get_ports {switch[0]}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {switch[0]}]
set_property PACKAGE_PIN V16 [get_ports {switch[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {switch[1]}]
set_property PACKAGE_PIN W16 [get_ports {switch[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {switch[2]}]
set_property PACKAGE_PIN W17 [get_ports {switch[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {switch[3]}]



## 7 segment display
set_property PACKAGE_PIN W7 [get_ports {seg[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {seg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {seg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {seg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {seg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {seg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {seg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]

## Anodes
set_property PACKAGE_PIN U2 [get_ports {an[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]
```