Lab 1 Report

Name: **UT EID:** **Section:**

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Note Only one student per group needs to submit the lab report and zip file on Canvas

Report Checklist:

Part 1 –

i. Simulation waveforms for Structural as well as Behavioral modelling (Screenshots)

Part 2 –

ii. Truth table of the function
iii. Algebraic expression of the logic function
iv. Logic circuit schematic for structural modelling
v. Verilog codes for module and testbench for structural modelling
vi. Simulation waveform for structural modelling (Screenshot)
vii. Verilog codes for module and testbench for behavioral modelling
viii. Simulation waveform for behavioral modelling (Screenshot)

Note

Please include legible screenshots of all required content (e.g., complete Verilog code) in the report, so the TAs can grade without unpacking anything.

Please name the report as "labx_name1_name2"

Zip File Checklist:

Part 2 –

i. Verilog codes for module and testbench for structural modelling
ii. Verilog codes for module and testbench for behavioral modelling

Note

Please zip all the items listed in the "Zip File Checklist" and name the zip file as "labx_name1_name2".

You are not allowed to modify your code after the final submission, as grading will be based on the version submitted on Canvas.