LAB 2 Report

Name: **UT EID:** **Section:**

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Note Only one student per group needs to submit the lab report and zip file on Canvas

Report Checklist:

Part 1 -

i. Waveform of the structural AND gate
ii. Constraint File (Just the uncommented portion)

Part 2 -

iii. Constraint File (Just the uncommented portion)

Part 3 -

iv. Truth Table of the function
v. K-maps showing minimization of the logic functions (outputs)
vi. Algebraic expression of the minimized logic functions (outputs)
vii. Verilog codes of module and testbench for structural modelling
viii. Simulation waveform for structural modelling
ix. Constraint File (Just the uncommented portion)

Note

Please include legible screenshots of all required content (e.g., complete Verilog code) in the report, so the TAs can grade without unpacking anything.

Please name the report as "labx_name1_name2"

Zip File Checklist:

Part 1 -

i. Constraint File
ii. Bitstream file

Part 2 -

iii. Constraint File
iv. Bitstream file

Part 3 -

v. Verilog codes of module and testbench for structural modelling
vi. Constraint File
vii. Bitstream file

Note

Please zip all the items listed in the "Zip File Checklist" and name the zip file as "labx_name1_name2".

You are not allowed to modify your code after the final submission, as grading will be based on the version submitted on Canvas.