Technical Guide

COLOUR TELEVISION
GP 3 Chassis

Circuit Explanations

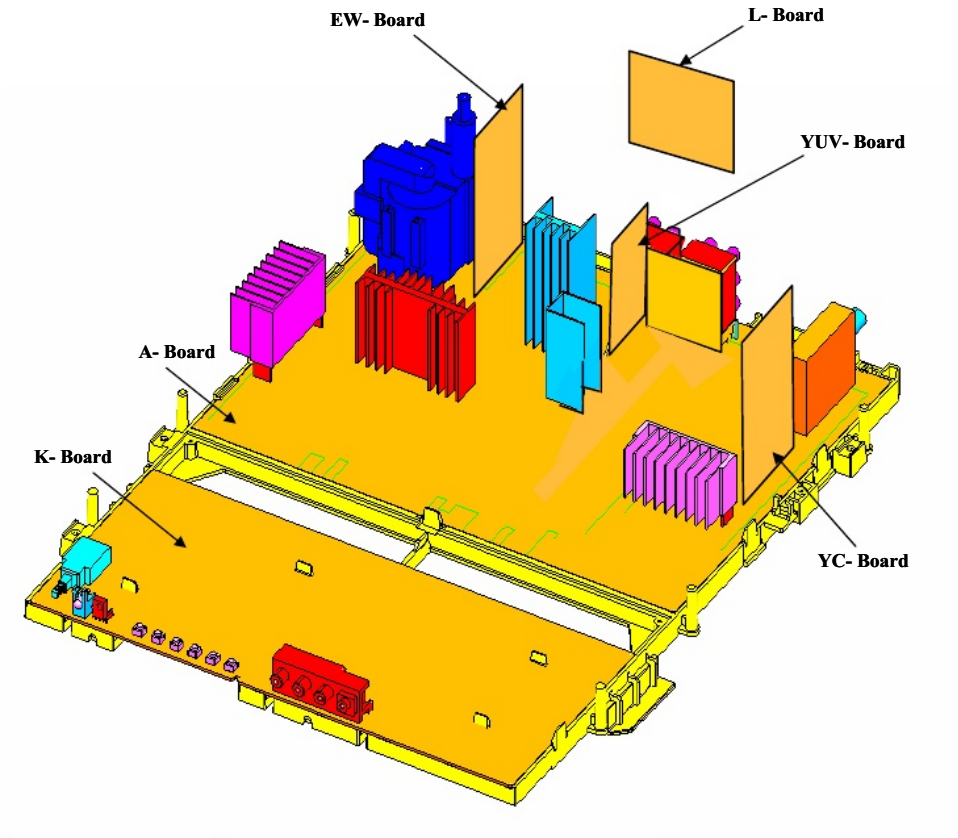
Panasonic

Panasonic AVC Networks
Kuala Lumpur Malaysia Sdn. Bhd.

Contents

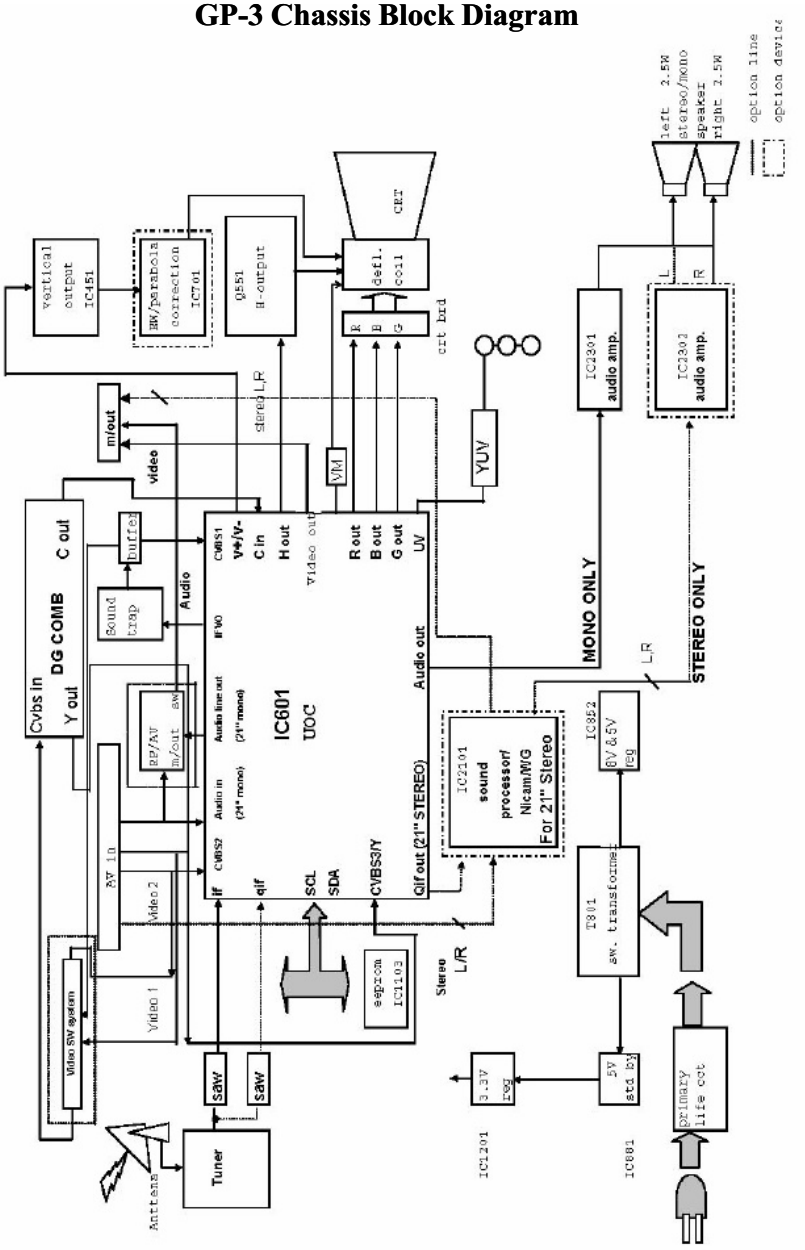
Location of Control & Circuit Boards	**3**
GP-3 Chassis Block Diagram	**4**
1. Ultimate One Chip IC601	**7**
1.1 Features	**7**
1.2 IIC Bus	**8**
1.3 Memory IC	**9**
1.4 Reset Circuit	**10**
1.5 IC601 Pin Configuration	**10**
2. Tuning	**13**
2.1 AFT Tuning Operation	**13**
3. VIF and Demodulation	**15**
4. Deflection Circuit	**16**
4a. Horizontal Output Circuit	**18**
4b. Vertical Output Circuit	**22**
4c. Geomagnetic Circuit	**24**
5. Audio Circuit	**26**
6. Protection Circuit	**27**
7. Power Circuit	**30**
7.1 Start-up Circuit	**30**
7.2 Output Voltage Control	**31**
7.3 Over Voltage Protection Circuit	**31**
7.4 Over Current Protection Circuit	**31**
7.5 Overload Protection Circuit	**31**
7.6 Standby Operation	**31**

Location of Control & Circuit Boards

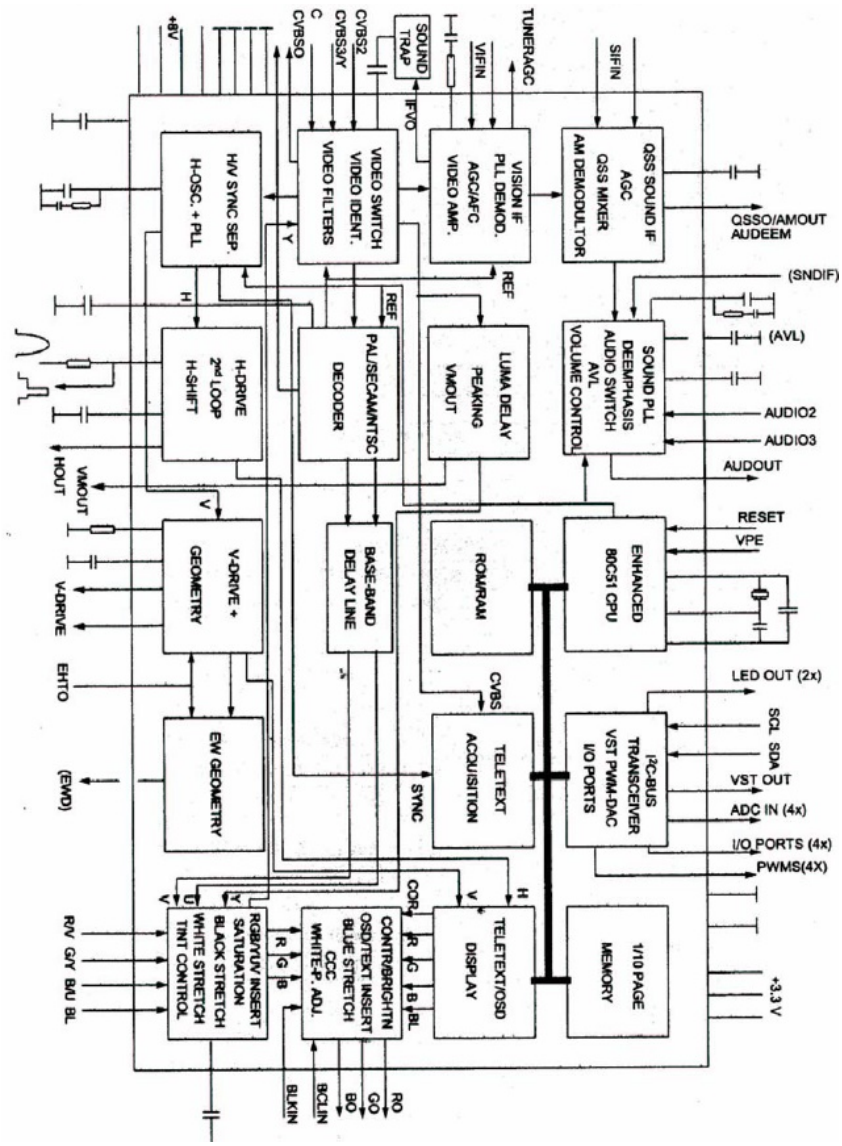


Board Name	Function
A-Board	Main Board
YC-Board	Y/C Separation Board
L-Board	CRT Board
K-Board	Front AV Board
YUV-Board	Rear YUV Board
EW-Board	East-West Drive Board

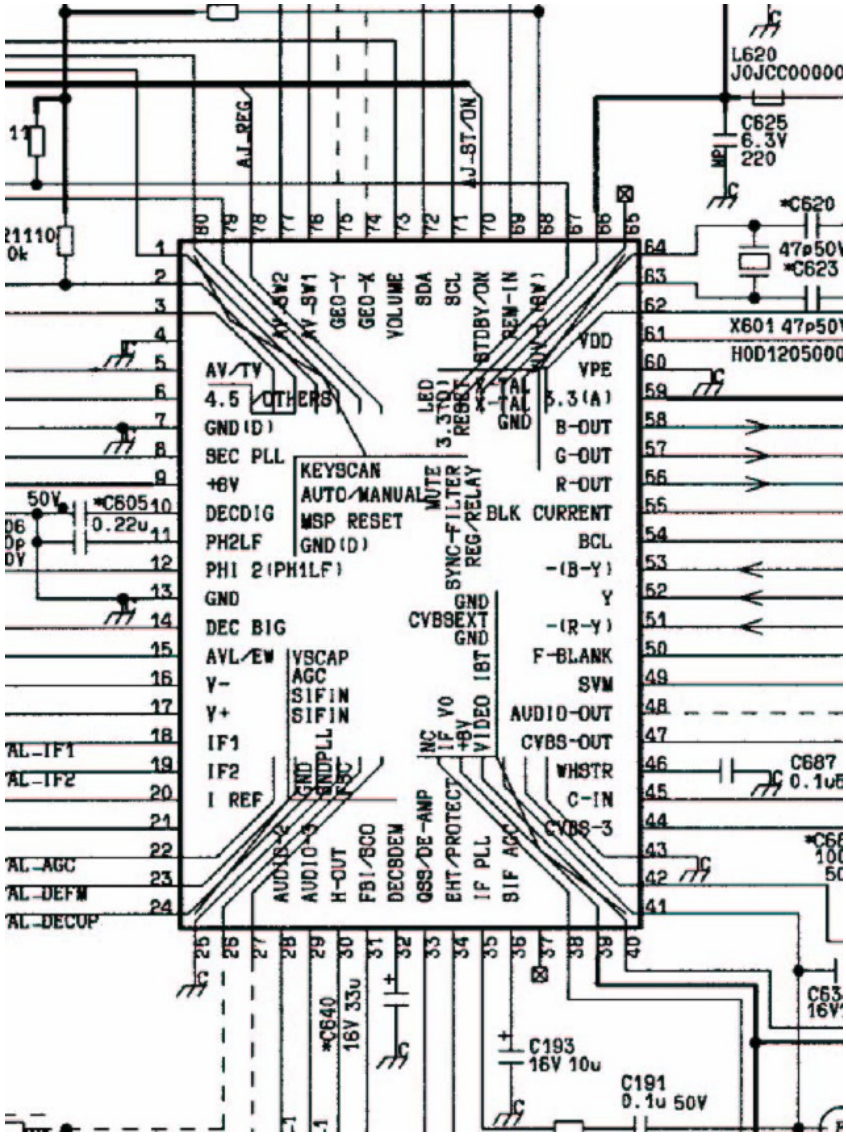
GP-3 Chassis Block Diagram



UOC IC601


+8V
CVBSO
C
CVBS3Y
CVBS2
SOUND TRAP
IF I/O
VIFIN
TUNERAGC
SIFIN
H/V SYNC SEP.
H-OSC. + PLL
VIDEO FILTERS
VIDEO SWITCH
VIDEO IDENT.
VISION IF PLL DEMOD.
AGC/AFC
VIDEO AMP.
QSS SOUND IF
AGC
QSS MIXER
AM DEMODULTOR
QSSO/AMOUT
AUDEEM
(SNDIF)
H-DRIVE
2nd LOOP
H-SHIFT
PAL/SECAM/NTSC
DECODER
LUMA DELAY
PEAKING
VMOUT
SOUND PLL
DEEMPHASIS
AUDIO SWITCH
AVL
VOLUME CONTROL
(AVL)
AUDIO2
AUDIO3
AUDOUT
HOUT
VMOUT
V-DRIVE +
GEOMETRY
BASE-BAND
DELAY LINE
ROM/RAM
ENHANCED
80C51 CPU
RESET
VPE
V-DRIVE
EHTO
(EWD)
EW GEOMETRY
CVBS
SYNC
TELETEXT
ACQUISITION
I²C-BUS
TRANSCEIVER
VST PWM-DAC
I/O PORTS
LED OUT (2x)
SCL
SDA
VST OUT
ADC IN (4x)
I/O PORTS (4x)
PWMS(4X)
R/V
G/Y
B/U
BL
WHITE STRETCH
TINT CONTROL
BLACK STRETCH
SATURATION
RGB/YUV INSERT
CCC
WHITE-P. ADJ.
BLUE STRETCH
OSD/TEXT INSERT
CONTR/BRIGHTN
TELETEXT/OSD
DISPLAY
1/10 PAGE
MEMORY
+3.3 V
BLKIN
BCLIN
BO
GO
RO

UOC IC601


L620
J0JCC00000
C625
6.3V
220
*C620
47p50V
*C623
X601 47p50V
H0D1205000
AV/TV
4.5
OTHERS
GND(D)
SEC PLL
+8V
DECDIG
PH2LF
PHI 2(PH1LF)
GND
DEC BIG
AVL/EW
V-
V+
IF1
IF2
I REF
KEYSCAN
AUTO/MANUAL
MSP RESET
GND(D)
VSCAP
AGC
SIFIN
SIFIN
VDD
VPE
5.3(A)
B-OUT
G-OUT
R-OUT
BLK CURRENT
BCL
-(B-Y)
Y
-(R-Y)
F-BLANK
SVM
AUDIO-OUT
CVBS-OUT
WHSTR
C-IN
CVBS-3
*C605
0.22u
50V
C687
0.1u
*C640
16V 33u
C193
16V 10u
C191
0.1u 50V

1. Ultimate One Chip IC601

Outline

The IC TDA9590N combines the functions of a video processor together with a micro-controller. This IC also has a Teletext Decoder on board. It is simple, efficient instruction set helps making it both economical and fast.

The video processor contains VIF, SIF, Video, Chroma and Deflection blocks. It can be applied for PAL/ NTSC/ SECAM system colour TV. TDA9590N incorporates a high performance picture quality compensation circuit in the video section. A crystal oscillator that externally generates 12MHz clock signal for colour demodulation and micro-controller. It also has a built in I²C Bus line to set or control various functions.

Micro-controller output switching and control signals for the circuit equipped with GP-3 chassis which depends on the commands from remote control transmitter or the circuit equipped with.

1.1 Features

a. Video Processor

1. **IF Section**
   - Integrated VIF VCO, alignment-free
   - SIF demodulator
2. **Video Section**
   - Chroma band-pass and trap
   - Y internal base-band delay line
   - Pre / over shoot control
   - White, Blue, black stretch
   - VM signal output
3. **Chroma Section**
   - PAL/ NTSC/ SECAM decoder
   - TINT control
   - Automatic Colour Limiting (ACL)
4. **RGB Section**
   - RGB control circuit with ‘Continuous Cathode Calibration’
   - RGB cut-off/ drive control by bus
5. **Sync./ DEF Section**
   - EW output
   - V sawtooth output

b. Micro-controller

- 80C51 CPU
- 128 Kbytes program ROM
- 12Kbytes Data RAM
- A minimum instruction execution time of 1 μs machine cycle
- Storage of 100 positions / channels
- On Screen Display (OSD)
  Output of RGB signal for ON-Screen Display message to be displayed on CRT
- Data Back-up
  Storage of tuning, switching, control and adjustment data to the memory (IC1103) and reading out the data
- Switching and Control
  Output of the control signal for picture and sound, etc., and switching signal for TV/AV mode and so on
- Adjustment
  Output of adjustment levels for OUC (IC601) through I²C bus.

c. Teletext Decoder

- Internal RAM memory for 10 page text.
- Automatic detection of FASTEXT transmission

1.2 I²C bus

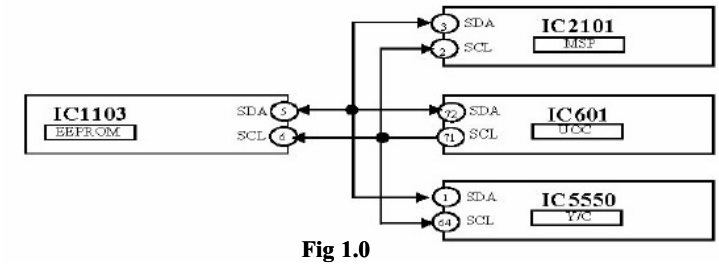


Fig 1.0

- The I²C bus is a two bus system consisting of a data line and a clock line.
- 5V is set for SDA / SCL. [Fig 1.0]
- Allow a large number of switching and control functions of GP-3 chassis.

The UOC IC601 generates bus signals which control the following hardware configuration.

1. EEPROM IC1103 (C3EBFC000021)
   These memories are 8k-bit, non-volatile memories of microchips, and bit pattern of 1024 x 8 bits.

2. Sound Processor IC2101 (MSP3460GAB83)
The sound processor IC will cover the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards.

3. YC Separation IC5550 (MN82362)
The YC IC will produce Y and C output for UOC IC601

1.3 Memory IC

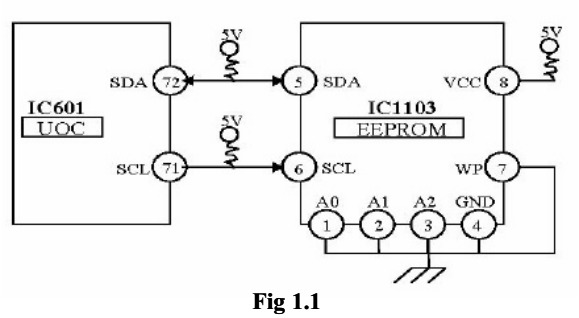


Fig 1.1

The memory IC1103 receives the data listed below as supplied from the UOC IC601 through I²C bus [Fig 1.1]. It is input or output whenever it is necessary. This memory IC is a non-volatile type, which data is maintained permanently although the power is cut off.

Last Memory Location

These memory locations will contain the following information that must be stored inside even if power to the EEPROM is interrupted.

1. 100 channels of BT voltage and band (VL, VH, U) information.
2. 100 channels of AFC, SKIP, COLOR SYSTEM and SIF information.
3. Last position for each switching mode.
4. Volume data.
5. TV/ AV1/ AV2 mode.
6. Recall ON/ OFF.
7. Power and auto off timer setting.
8. Service mode setting.
9. The COLOUR, NTSC TINT, BRIGHT, CONTRAST and SHARPNESS DAC data, and each SUB-DAC data, CUT-OFF, RGB-DRIVE etc.
10. PICTURE MENU & SOUND MENU.
11. AVL

Pin No.	Name	Function
1	A0	GROUND
2	A1	GROUND
3	A2	GROUND
4	GND	GROUND
5	SDA	Serial Data In/Out
6	SCL	Serial Clock Input
7	WP	GROUND
8	VCC	5V

1.4 Reset circuit

1. Power on reset is generated internally to the UOC IC601; hence no external reset is required. (The TV processor generates the master reset in the system, which in turn will reset the micro-controller.)
2. During power on/off operation, or during a momentary drop in the +B voltage, insufficient voltage supply to UOC IC601 may will occur. Thus, there is a possibility that incorrect operation of the UOC occur.
3. In order to prevent incorrect operation, a resetting pulse is activated until the voltage fed to the UOC is normalized.
4. When the power switch is turned on, if the VDD of the UOC is less than 3.3V then UOC starts to reset.
5. UOC start to function again when VDD becomes more than 3.3V.

1.5 IC601 Pin Configuration

Pin No.	Name	Description
1	KEYSCAN	Panel key
2	AUTO / MANUAL	Geomagnetic controlling H: Auto L: Manual
3	MSP RESET	H: Normal L: Reset (During power ON)
4	GND (D)	Digital ground for µ-Controller core and periphery
5	AV/TV	TV / AV search H: AV / Auto Search L: TV
6	4.5V / OTHERS	H: 4.5MHz L: Other / AV
7	GND (D)	Digital ground of TV-processor
8	SECPLL	SECAM PLL decoupling
9	+8V	2nd supply voltage TV-processor
10	DECDIG	Supply voltage decoupling of digital circuit of TV-processor
11	PH2LF	Phase-2 filter
12	PH1LF	Phase-1 filter
13	GND3	Ground 3 for TV-processor
14	DECBG	Bandgap decoupling
15	AVL / EWD	East-West drive output
16	VDRB	Vertical drive B output
17	VDRA	Vertical drive A output

18	IFIN1	IF input 1
19	IFIN2	IF input 2
20	IFREF	Reference current input
21	VSC	Vertical sawtooth capacitor
22	AGCOUT	Tuner AGC output
23	SIFIN1	SIF input 1
24	SIFIN2	SIF input 2
25	GND2	Ground 2 for TV-processor
26	SNDPLL	Narrow band PLL filter
27	FSC	Sub-carrier reference output
28	AUDIO2	Audio 2 input
29	AUDIO3	Audio 3 input
30	HOUT	Horizontal output
31	FBISO	Flyback input / Sandcastle output
32	DESCDEM	Decoupling sound demodulator
33	QSS / DEAMP	QSS intercarrier output / AM output in stereo applications or deemphasis (front-end audio out) / AM output in mono applications
34	EHT / PROTECT	EHT / overvoltage protection input
35	PLLIF	IF-PLL loop filter
36	SIFAGC	AGC sound IF
37	INTCO	Not used
38	IFVO/SVO	IF video output / selected CVBS output
39	+8V	Main supply voltage for TV-processor
40	CVBS1	Internal CVBS input
41	GND	Ground for TV-processor
42	CVBS2	External CVBS2 input
43	GND	Ground for TV-processor
44	CVBS3/Y	CVBS3/Y input
45	C	Chroma input
46	WHSTR	White stretch capacitor
47	CVBSO	CVBS output
48	AUDOUT / AMOUT	Audio output / AM audio output (volume controlled)
49	SVM	Scan velocity modulation output
50	INSSW2	2nd RGB / YUV insertion input
51	R2/VIN	2nd R input / V (R-Y) input / P_R input
52	G2/YIN	2nd G input / Y input
53	B2/UIN	2nd B input / U (B-Y) input / P_B input
54	BCLIN	Beam current limiter input
55	BLKIN	Black current input / V-guard input
56	RO	Red output
57	GO	Green output
58	BO	Blue output
59	+3.3V	Analog supply of Teletext decoder and digital supply of TV-processor (3.3V)
60	VPE	OTP Programming Voltage
61	VDDC	Digital supply to core (3.3V)
62	OSCGND	Oscillator ground supply
63	XTALIN	Crystal oscillator input
64	XTALOUT	Crystal oscillator output
65	RESET	Not used
66	+3.3V	Digital supply to periphery (+3.3V)
67	LED	Red LED (Wake up timer) [Normal] H: STDBY L: Power off

		[Wake up] H: ON (1 sec) L: OFF (1 sec) [Protect Mode] 0.5 sec : ON 4 sec : OFF
68	YUV-L (SW)	Input for YUV H: YUV Input L: Manual
69	REM-IN	Input for the remote control signal
70	STDBY / ON	Power ON/OFF switching signal for main power circuit H: ON L: Standby
71	SCL	I²C-bus clock line (+5V)
72	SDA	I²C-bus data line (+5V)
73	VOLUME	Tuning PWM output (0 ~ 3.3V)
74	GEO-X	PWM control
75	GEO-Y	PWM control
76	AV-SW1	AV switch 1 H: AV1/DVD L: TV/AV2
77	AV-SW2	AV switch 2 H: AV2/DVD L: TV/AV1
78	REG / RELAY	H: Relay ON L: Relay OFF
79	SYNC_FILTER	Sync filter input
80	MUTE	Monitor defeat controlling H: Monitor defeat L: Defeat OFF

2. Tuning

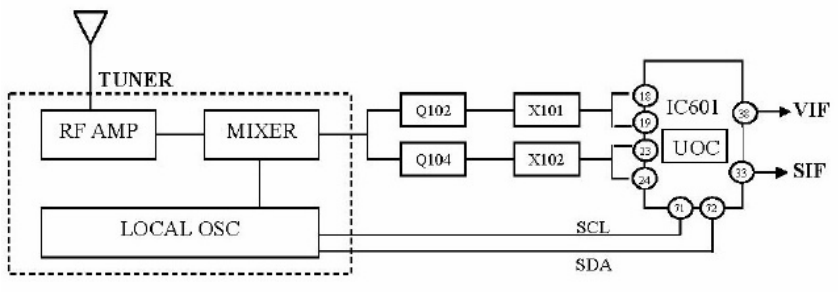


Fig 2.0

1. The purpose of the tuner is to convert the VHF/ UHF TV broadcast signal (RF) into intermediate frequency signal, IF (38.0MHz) [Fig 2.0].
2. The aerial intercepts the TV signal and amplified by the RF amplifier.
3. The local oscillator generates basic frequency to convert RF signal into IF signal (intermediate signal) in the mixer.
4. GP-3 chassis tuner's is a Frequency Synthesizer type. A Frequency Synthesizer is a circuit that generates precise frequency signal by means of a single crystal oscillator in conjunction with frequency dividers and multipliers. Frequency Synthesizer is digital device and it is characterized by discrete steps in frequency rather then adjustability over a continuous range. The steps can be rather large or very small, depending upon the application in which the device to be used.
5. In this tuner, many configurations were combined into tuner like VIF part, band selection IC and also SIF selection part.
6. By using the FS tuner, many different configurations were applied if compared with the Voltage Synthesizer such as BT Voltage and Band Selection. Both data from the BT Voltage and Band Selection were applied to the tuner from UOC by input signal voltage through SDA and SCL bus.
7. PLL function is built in the UOC.

AFT Tuning Operation

1. UOC output AFT by I²C Bus [Fig 2.0].
2. When UOC receives Tuning demand, it sends data to Tuner. If it is without demand, data will be refreshed.
3. IF signal is sent to UOC after the Tuner received the data from UOC. Then, Search Mode is carried out by UOC. The output status is as the following table.

Read out	Frequency range for '1' output
IF Lock	f_o-1.8MHz --f_o-- f_o+1.8MHz
AFT-W (w) (n)	f_o-200kHz --f_o-- f_o+200kHz f_o-50kHz --f_o-- f_o+50kHz
AFT-C	--f_o--

- IF Lock shows the locked/ unlocked status of IF APC
- AFT-W shows that the VCO oscillation frequency is within or without the set range (wide/narrow).
- AFT-C shows higher or lower status than center frequency, f_o.

4. UOC is ready to send the next data to Tuner and the whole process repeats.
5. During standby or 1 sec after switch off, UOC will not send data to Tuner.
6. 1 sec after switch ON, UOC will send the data to Tuner.

Search Mode

1) The sequence for searching in GP-3 is set to search from Lower channel to Upper channel. Beside this, it is also set to search from AFT-W (w) to AFT-W (n).
2) The IF center frequency is set to be 38.0MHz.
3) The followings describe the sequence of represent Lower channel to Upper channel searching. The tuned frequency is the point when AFT-C turns from 0 to 1.

Repeat the process for AFT-W (n)

Phase	IF Lock	AFT-W (w) *(n)*	AFT- C
1. IF Lock = 0 while unlocked	0	?	?
2. After Tuner sweep and IF is locked, the IF Lock turns to '1'	1	0	0
3. Sweep the Tuner more, AFT- W (w) or *(n)* turns to '1'	1	1	0
4. Sweep the Tuner more, AFT-C turns to '1'	1	1	1

3. VIF and Demodulation

Outline

1. The VIF circuit generates the necessary VIF signal by passing the receiving signal converted in the tuning circuit through the amplifier with the predetermined selectivity characteristic.
2. The VIF circuit consists of the following parts in the UOC IC601:
   - The video detection circuit employs the synchronous detection system. [ie. when power ON or Tuning, UOC synchronized with VIF signal which is ensured by APC].
   - The video signal is obtained by switching the reference signal (38.0MHz) which is generated from the VIF signal through VCO (Voltage Controlled Oscillator) and PLL (Phase Locked Loop) in the VIF Detection.
   - VCO and APC circuits generate the frequency signal for detection.
   - AFC circuit keeps Tuner local oscillator frequency constant so that it may not fluctuate due to changes of temperature and voltage during reception.

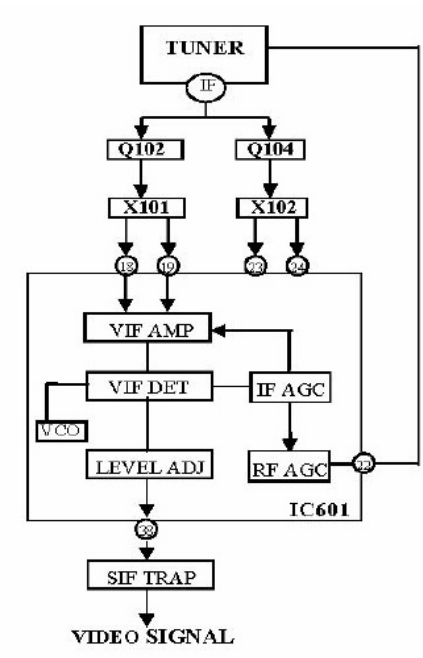


Fig 3.0

The IF signal leaving from the Tuner is separated into two paths [Fig 3.0].

One for SIF processing and the other for VIF processing.

For VIF processing, it passes through transistor Q102 making up for input loss in X101.

VIF signal is applied to SAW filter X101 in order to provide the required bandpass shaping.

From X101 the signal is fed to the first stage of VIF amplification.

After amplification, the signal is passed to the VIF DETECT. VCO free runs at 38MHz. APC compare the unmodulated portion of VIF frequency with VCO frequency and correct the VCO output until VCO frequency corresponds with that of VIF.

Since brightness of picture and depth of colour changes when IF strength of receiving radio wave changes, AGC keep video detection output constant.

The IF AGC controls the level of amplification in the VIF AMP while RF AGC controls amplification degree of the RF amplifier of Tuner.

After detection, the signal is fed to an external SIF trap circuit to remove / filter the SIF component.

4. Deflection Circuit

Outline

1. The diagram in Fig 4.0 shows the signal flow for the deflection circuits.
2. The composite video signal is input to IC601 pin 44 and is separated by the horizontal and vertical sync separator circuits in order to provide scan synchronizing pulses.
3. The vertical synchronous signal is fed from pin 16 and 17 of IC601 to pin 1 and 7 of vertical drive IC451.
4. The IC451 consists of vertical drive, vertical output and pump up circuits. It sends sufficient sawtooth current to the vertical deflection coil for vertical scanning.
5. The horizontal synchronous signal from pin 30 of IC601 goes through the H-drive circuit, transistor Q501 and then to the drive transformer T553 in A-Board to produce large driving current needed to drive the horizontal output transistor Q551.
6. The Q551 amplifies the horizontal synchronous signal before sending to the horizontal deflection coil.

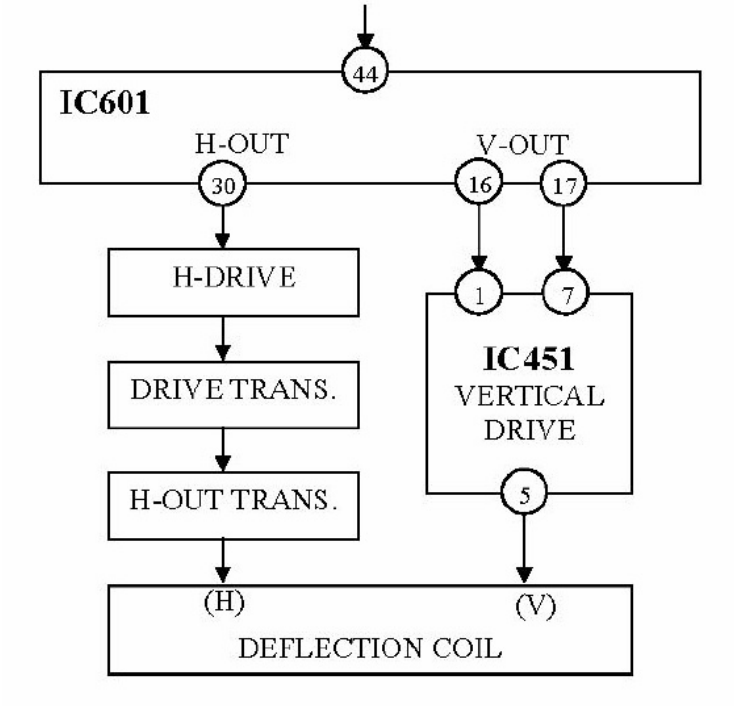
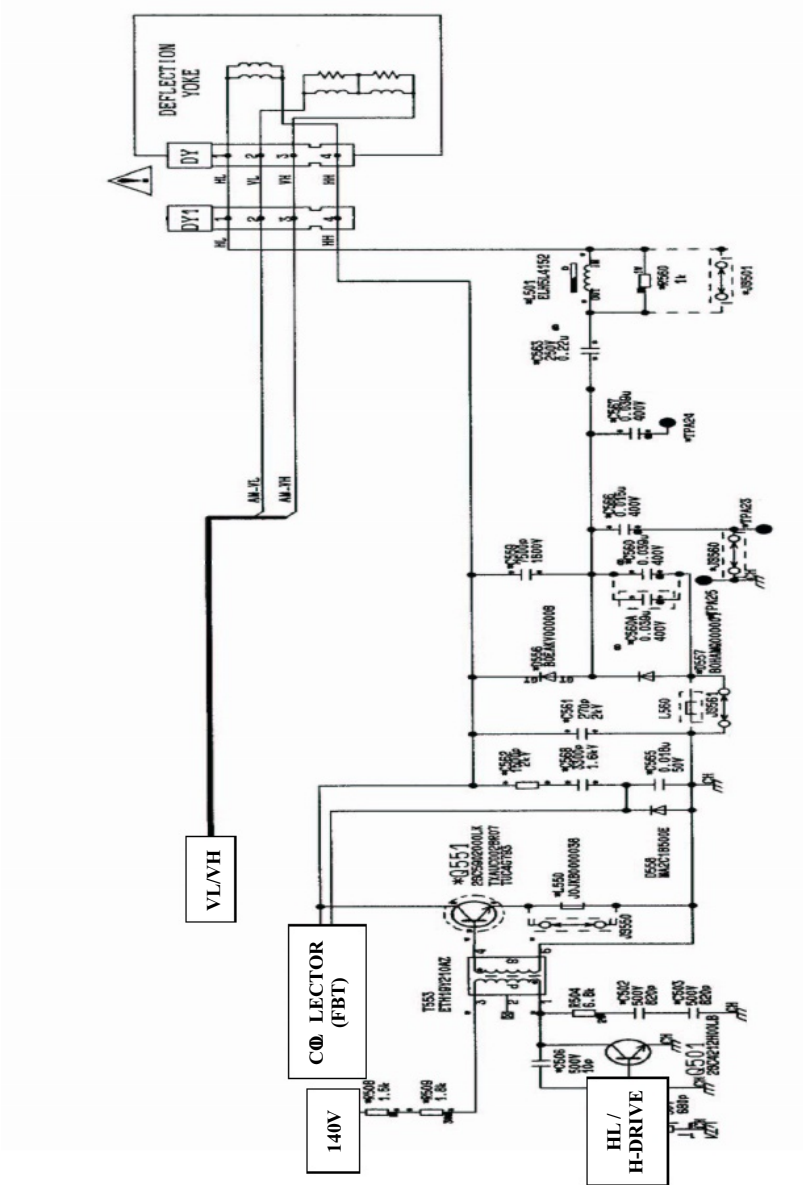


Fig 4.0

Horizontal Output Circuit



a) Horizontal Output Circuit

Outline

1. The horizontal synchronous pulse output from IC601 pin 30 is then input to the A-Board Horizontal Drive Circuit (Q501, T553).
2. The horizontal drive circuit creates a base current (drive current) fully sufficient to turn the horizontal output circuit (Q551) ON and OFF quickly, and inputs this current to the horizontal output circuit (Q551).
3. The horizontal output circuit (Q551) has the function of sending the deflection current to DY in order to make the electrical beam scans horizontally. Beside this, it also has an additional function of generating a high voltage in the second stage voltage coil of the Flyback Transformer (FBT) and supplying this voltage to the CRT anode pole and the focus pole.
4. A number of voltages are taken for using in Focus, CRT, and Heaters etc from the secondary of the Flyback Transformer.

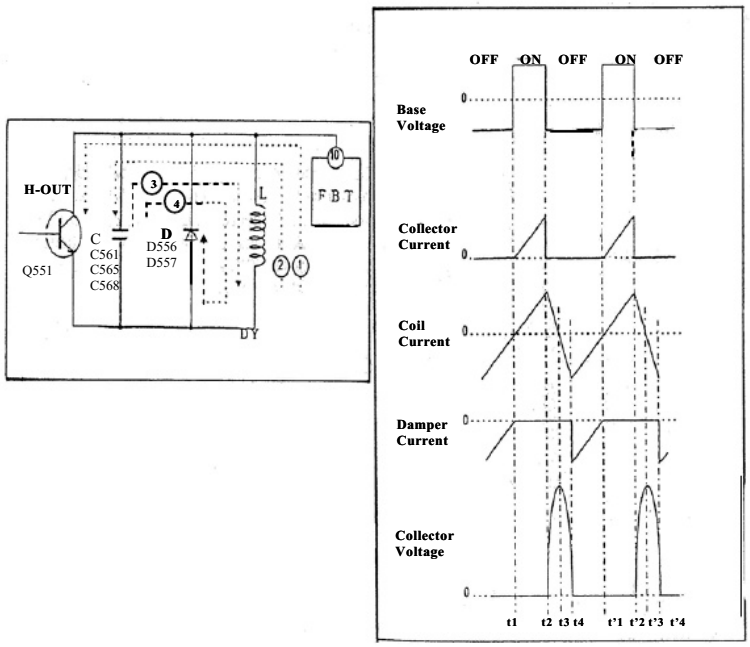


Fig 4.1

Horizontal Output Operation

1. Tr (Q551) base input does not work until it exceeds a certain level [Fig 4.1].
2. A positive polarized pulse is added to the base and as the base voltage exceeds a certain level, Tr turns ON. Then the collector current increases and the current flows into the deflection coil (t1- t2).
3. If the base input falls to a certain level, Tr turns OFF. The collector current become zero, but the coil current continues to flow and while charging the resonance capacitor C, it gradually decreases until finally reaching zero (t2-t3).
4. Then discharging begins along the path 3 going to the deflection coil from the resonance capacitor. A current opposes to the present current flows into the deflection coil (t3-t4).
5. Then the deflection coil current begins charging the capacitor with an opposite characteristic in the LC only resonance circuit.
6. However, since the damper diode D is connected, the deflection coil voltage between terminals biases the diode in a forward direction, the deflection coil current does not flow in to the resonance capacitor so the damper current flows into the diode. As a result, the resonance phenomenon is absorbed (t4-t1).
7. When the diode current reaches zero, a positively polarized pulse is added again to the Tr base. Therefore, it returns to Step 1.
8. Thus, operation is repeated from Step 2 to 5 and saw tooth wave flows regularly into the deflection coil.
9. At the moment the Tr turns OFF, a positive flyback pulse voltage greater than the power supply voltage is generated.
10. The flyback transistor uses this flyback pulse to generate the CRT anode voltage, Focus voltage and the Screen voltage.

Horizontal Scanning

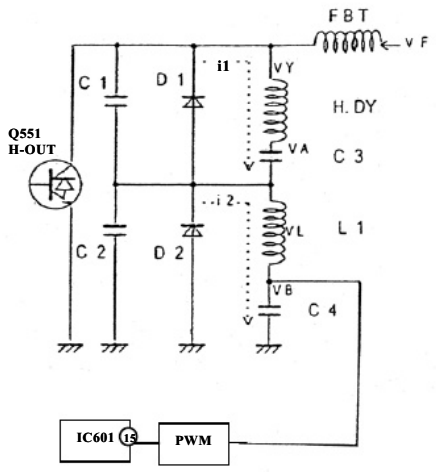


Fig 4.2

Diode modulation method— using the bridge circuit formed by the resonance capacitor (C1, C2), damper diode (D1,D2), horizontal deflection coil (H,DY), L1 and modulates the current flowing into horizontal deflection coil (H, DY) with the parabolic wave of the V-rate (vertical parabola) added to the PWM.

Operation

1. During the first half of the horizontal scanning, which takes place without adding vertical parabolic voltage at PWM [Fig 4.2], i1 and i2 currents flow as power supply and VA becomes VF= VA+VB. Then, during the second half of horizontal scanning, it takes the sum voltage of the counter- electromotive voltage VY generate in the horizontal deflection coil enclosure and the VL generated in L1. This voltage size is fixed by VF= VY+VL because the current that flows is proportioned to the current i1 and i2 that flowed during the first half of the scanning period.

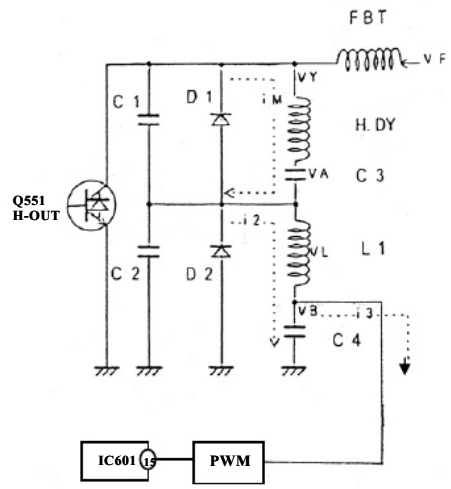


Fig 4.3

2. By adding the vertical parabolic voltage for correction to the PWM and it sends current i3 during that first half of scanning [Fig 4.3]. Thus, C4 enclosure voltage decreases and VA supersedes VB. However, since the current I'M flows, VA increases and VF is fixed.

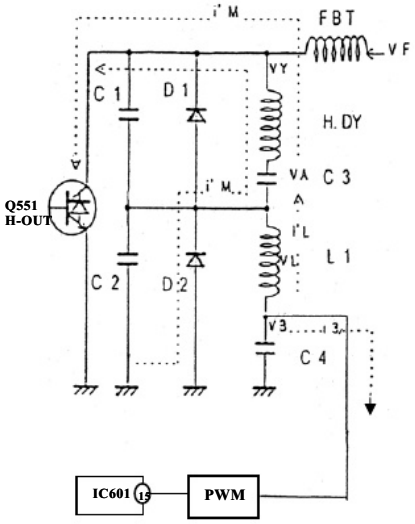
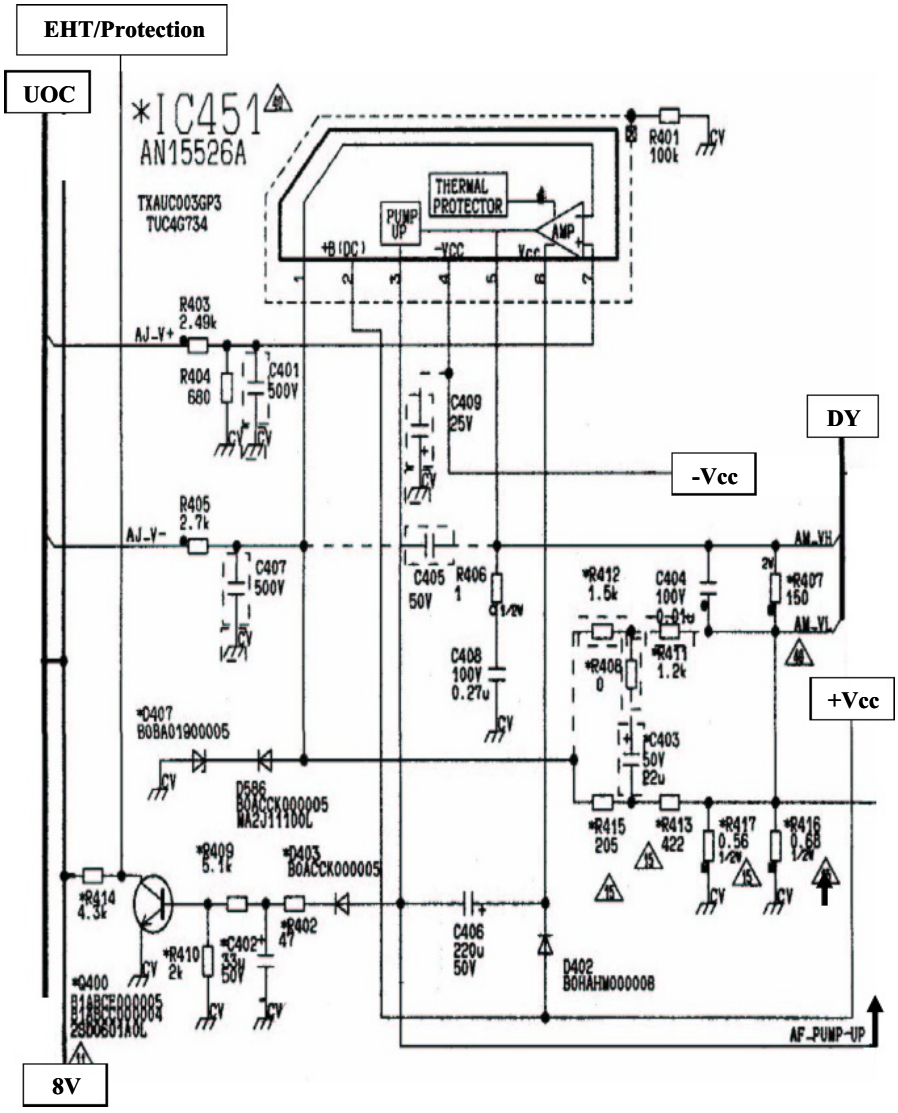


Fig 4.4

3. During the second half of scanning [Fig 4.4], current I'M flows, VA increases, VY increases and VB decreases resulting in decrement in VL.

VA : C4 enclosed voltage
VF : FBT primary side voltage
VL : counter- electromotive voltage generated at the L1 enclosure
VY : counter- electromotive voltage generated at the H- deflection coil enclosure.

Vertical Output Circuit



b) Vertical Synchronous Processing Circuit

Outline

1. The main function of this circuit is to produce a sawtooth deflection current and amplify the vertical sawtooth waveform to the vertical deflection coil for vertical scanning.
2. The output IC451 is a vertical IC to provide output deflection current to the vertical coil of the deflection yoke.
3. The vertical sync. pulse output from pin 16 and 17 of IC601 is fed into pin 1 and 7 of IC451. The sawtooth waveform is then compared with the V_{ref} from non-inverting input at pin 7 IC451. Then, sawtooth waveform is then amplified and output through pin 5 IC451 to the vertical deflection coil.
4. The Pump Up circuit in IC451 works along with the external components C406 and D402 to boost the vertical sawtooth waveform peak value.

IC451 Vertical Out

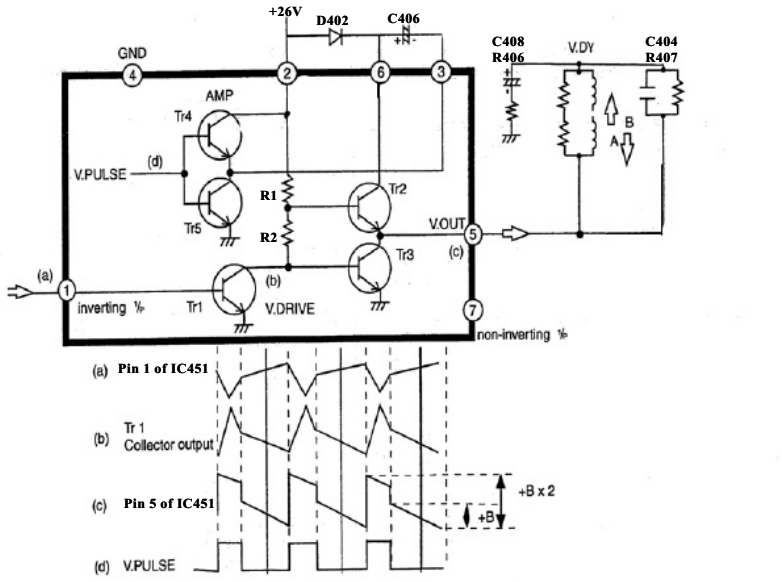


Fig 4.5

Signal Flow

1. The vertical drive signal (sawtooth wave voltage) enters IC451 at pin 1 and 7[Fig 4.5].
2. After the input sawtooth wave voltage is inverted by Tr1(b), it is input into the base of Tr2 and Tr3.
3. The threshold voltage of Tr2 and Tr3 are set by R1 and R2 at the center of the sawtooth wave. While scanning the upper half of the screen, Tr2 switches ON and Tr3 switches OFF.
4. As Tr2 switches ON, the following occurs:
   - +26V is input into pin6 of IC451 via D402.
   - The input +26V is output from pin5 of IC451 via Tr2 to deflection yoke to achieve scan.
5. As a result, a directed magnetic field is generated in DY, and it scans with an electronic beam from the top to the center of the screen. (As this progress, the density of magnetic flux decrease)
6. C408 is charged by the current flowing through DY. The operations of Tr4 and Tr5 are controlled by the vertical pulse.
7. During the scanning period, Tr4 switches to OFF and Tr5 to ON since the vertical pulse is zero. Thus, a current runs to the Tr5 collector via D402 and C406, and +26V charges up C406.
8. Next during the scanning period, Tr3 switches ON and Tr2 turns OFF. Therefore, C406 discharges from pin5 of IC451 via Tr3.
9. At this point, a B-directed magnetic field is generated in DY and an electronic beam is passed from the center to the lower side of the screen. (As this progress, the density of magnetic flux decrease)
10. The scanning process of the lower side is completed and as the flyback line period begins, a vertical pulse is added to the pulse amplification circuit (Tr4 and Tr5 base).
11. During the pulse's High period, Tr5 switches OFF and Tr4 switches ON, the +26V added to pin2 is added to pin3 via Tr4.
12. As a result, a current of the opposite direction flows in to C406. Beside this, Tr3 switches OFF and Tr2 switches ON during the scanning period. Therefore, this +26V is added to the +26V discharged by C406 resulting in a 52V of voltage applied to vertical DY.
13. As a result of the above operation, the +B is added to vertical DY only during the vertical flyback line period is doubled, the line period is shortened and the start of raster at the top of the screen is erased.
14. C404 and R407 are included for prevention of abnormal oscillation.

c) Geomagnetic Circuit

Outline

TV's with 29'' in CRT's requires an additional circuit which is used for picture geomagnetic adjustment [Fig 4.6]. This additional circuit is used to cancel the effects of the earth's magnetic field. On GP-3 chassis, this geomagnetic circuit is provided in the form of IC4803.

Signal Flow

1. The control line from IC601 pin 74 is fed to pin 3 of IC4803 in DC form.
2. When the geomagnetic change in Features Menu, output voltage frequency changes in IC601.
3. Rotation of the picture is achieved by controlling only the output from pin 1 and pin 7 by increasing and decreasing its DC output.
4. Signal is output via pin 1 and 7 and is fed to the rotation coil.

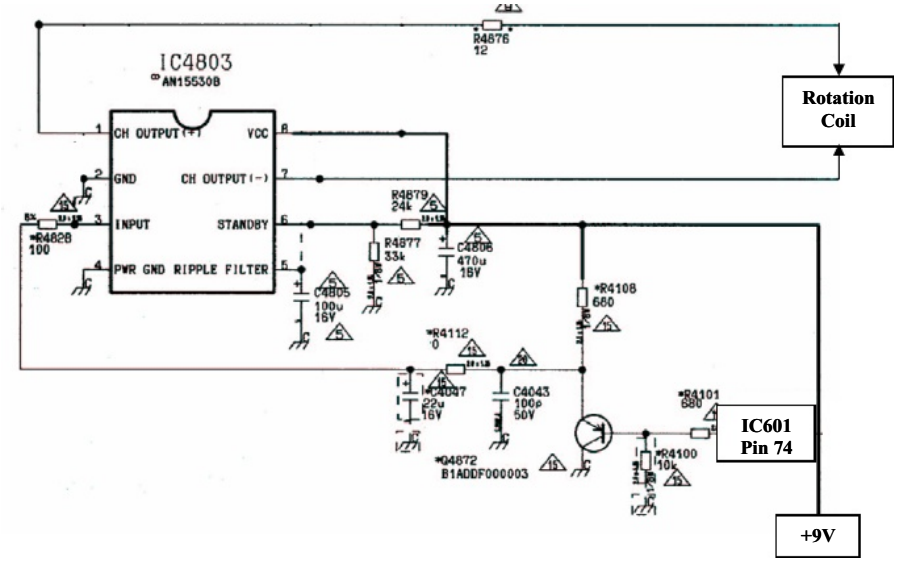
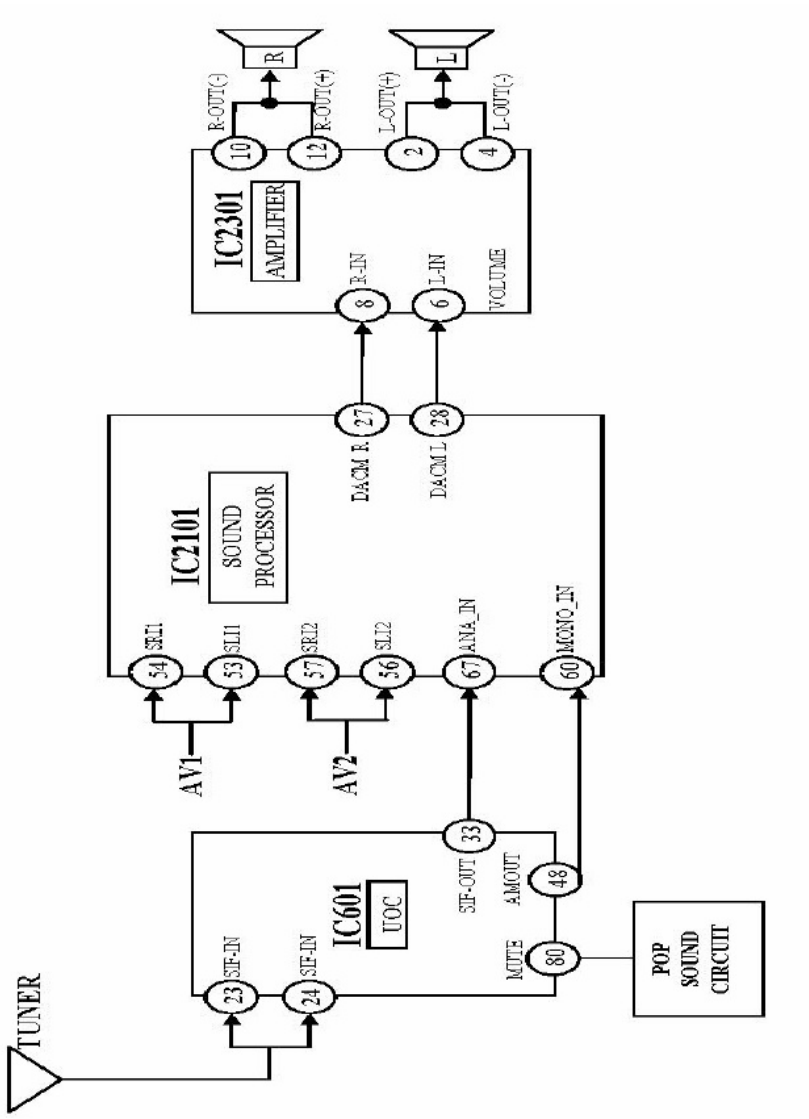


Fig 4.6

Audio Circuit



5. Audio Circuit

Outline

The SIF circuit is built inside the UOC IC601 in GP-3 chassis. The SIF output from UOC IC601 is sent to Sound Processor IC2101 at pin 60 and pin 67. Then the sound signals are sent to audio amplifier IC2301.

Audio Processor

Two different sound processors are used in GP-3. IC2101 is used as Sound Processor and IC2301 as Audio Amplifier.

a) Sound Processor (IC2101)

Outline

IC2101 is a single-chip multi-standard Sound Processor that simultaneously performs digital demodulation and decoding of NICAM-coded TV stereo sound, as well as demodulation of FM-mono TV sound. It covers the sound processing of all analog TV-Standards worldwide (B/G, L, I, D/K, M, M-KOREA, Satellite) for Mono and stereo demodulation. The full sound processing starts with analog SIF signal-in until to process analog AF-out, is done on this single chip.

RF Input

1. The analog- to- digital conversion of the pre-selected sound SIF signal from pin 60 (MONO) and pin 67 (STEREO) is done by an A/D-converter.
2. An analog automatic gain circuit (AGC) allows a wide range of inputs level.
3. Then, this converted signal is gone through the demodulation in order to generate the Mono/Stereo sound.

AV Input

1. Audio outputs from AV terminals are fed into pin 56 and 57 (AV2), and pin 53 and 54 (AV1).
2. The selected audio signal source then will be processed and output to Audio Amplifier IC2301.
3. At the same time, the selected unprocessed audio signal is also output to IC2101 pin 36 and 37 for Monitor Out purpose.

b) Audio Amplifier (IC2301)

Outline

The sound signal from IC2101 pin 27 and 28 is amplified by IC2301 and passes it to loudspeakers.

6. Protection Circuit

Outline

1. The main function of the protection circuit is to prevent main chassis of TV set from serious damage when faults occur in the circuit.
2. The protection on the EHT input (Pin 34 of IC601) is intended for overvoltage (X-ray) protection. When this protection is activated, the horizontal drive is directly switched off (protection mode).

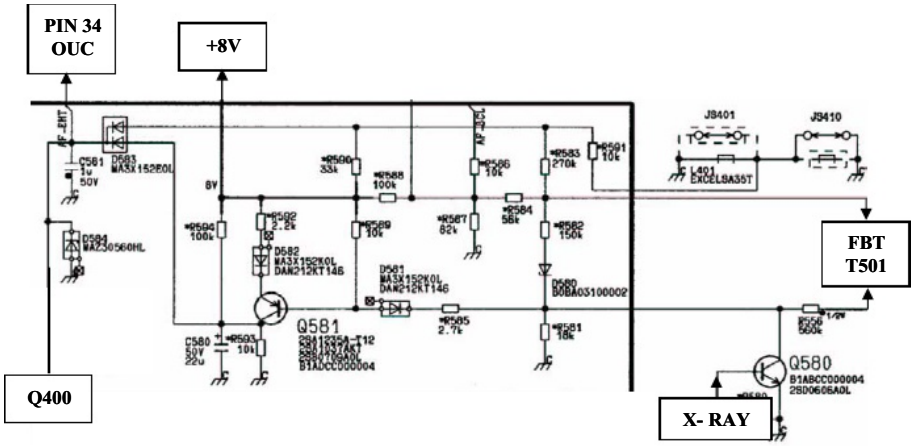


Fig 6.0

3. This circuit will function whenever X-ray stage starts operation. The X-ray voltage will trigger Q580 ON → Q581 ON → D583 ON → EHT/ PROTECTION input (Pin 34) pulled HIGH → UOC OFF. [Fig 6.0]
4. Therefore, EHT/ PROTECTION input will pull down to latch mode by the emitter of Q581 and circuit will go to shut down mode until reset by main power switch.

Operation

- **Power Supply Protection**
  Condition 1: power supply interruption during power ON
  If the power supply is interrupted, pin 34 of IC601 pulled HIGH, then TV set will go to standby (protection mode).

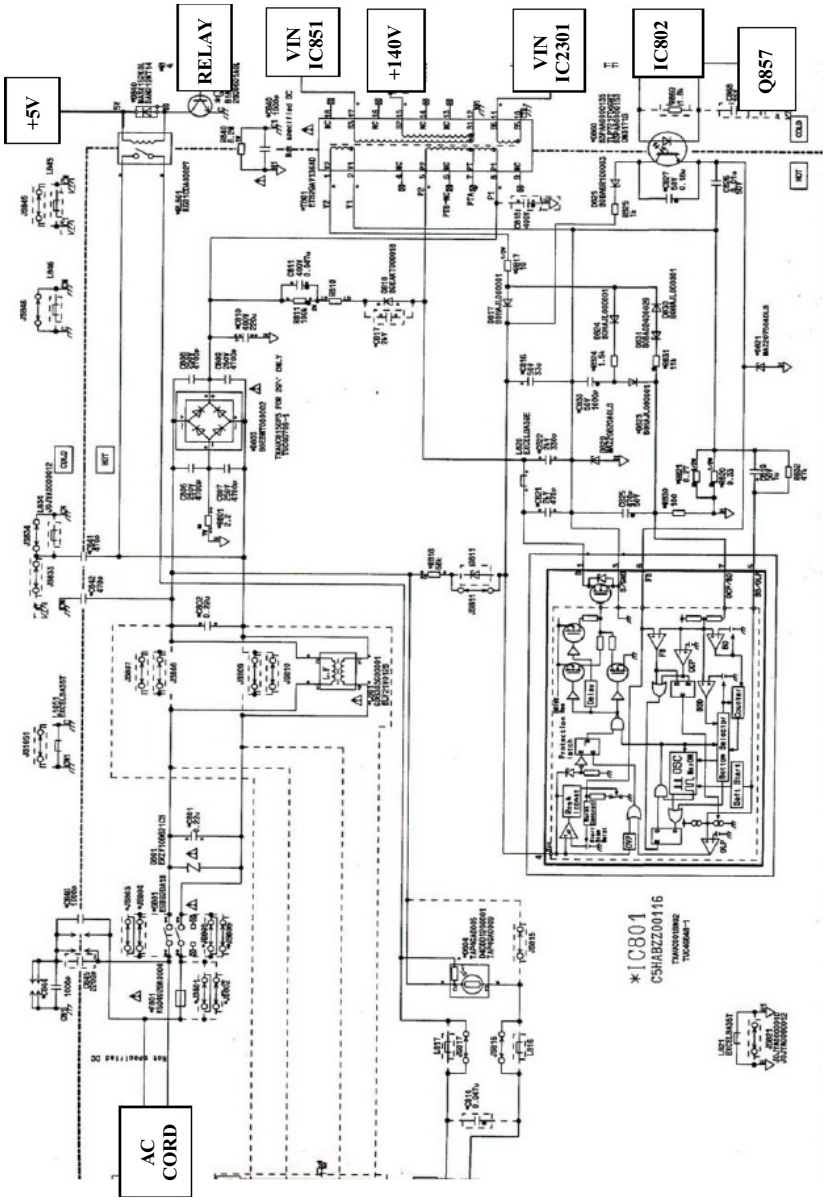
  Condition 2: circuit malfunction when TV set is already ON
  If TV set is under ON condition and circuit malfunction happened, pin 34 of IC601 pulled HIGH, then TV set will go to standby (protection mode).

- **Excessive Current in +140V line :**
  When the break over voltage of D520 is exceeded, a HIGH level is applied to the base of Q580.
  Q520 ON → D520 ON → Protection circuit ON → Pin 34 of UOC High → UOC OFF

- **Overvoltage Of CRT Heater in X- Ray Protector Circuit :**
  When the heater voltage exceeds the zener (D511) breakover voltage, a HIGH level is applied to base of Q580.
  D511 ON (X-ray protector circuit) → Protection circuit ON → Pin 34 of UOC High → UOC OFF

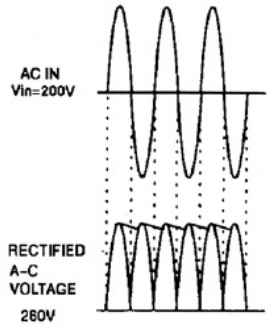
- **Excessive Voltage In Vertical Deflection Chip IC451 :**
  When an error in the vertical deflection circuit occurs, a LOW level is applied to the base of Q400 causing the transistor to switch OFF. A HIGH level is fed via D404 to base of protection Q581.
  Q400 OFF → D404 ON → D583 ON → Pin 34 of UOC High → UOC OFF

Power Circuit



7. Power Circuit

Outline



The supply voltage for the main power supply circuit is fed to the bridge rectifier D803 where the AC voltage is fully rectified and smoothed. [Fig 7.0].

Fig 7.0

7.1 Start-Up Circuit

1. The start-up circuit detects Vin terminal (pin 4 IC801) voltage, and makes the control IC (IC801) start and stop.
2. At start-up, C816 is charged through the start-up resistor R818. Once the Vin terminal pin 4 voltage reaches 18.2V, the control circuit starts operating by the function of the start-up circuit.
3. After the control circuit starts its operation, power supply is fed to pin 4 by smoothing and rectifying the voltage of the drive winding (V2-V1) through R817, C816 and D817.
4. The drive winding voltage does not increase to the set voltage after the control circuit starts its operation, and the Vin terminal voltage starts decreasing.
5. However, because the shutdown voltage is set as low as 9.6V, the drive winding voltage reaches stabilizing voltage before falling to the operation stop voltage, and the control circuit continues its operation.
6. If voltage at pin 4 is below 9.6V, IC801 stop functioning.

7.2 Output Voltage Control

1. Output voltage is controlled by voltage at pin 7 of IC801. This control system is called DC bias control system.
2. Threshold voltage of the internal oscillation circuit at pin 7 of IC801 is 0.95V.
3. Voltage at pin 7 is determined by feedback current flow through R820, R821 and R830.

7.3 Over Voltage Protection Circuit

1. When the voltage imposed between Vin and Ground terminals exceeds 27.5V, this circuit starts its operation and turns latch-mode, and the control IC stops its oscillation.
2. Although this circuit basically functions as protection of the Vin terminal, it also prevents overvoltage at the secondary output (ie open circuited or by some other event), since the Vin terminal voltage is supplied from the drive winding of the transformer, whose voltage is proportional to the output voltage from the secondary windings.

7.4 Over Current Protection Circuit

1. This is a pulse-by-pulse type overcurrent protection circuit, which detects the peak of the MOSFET drain current per pulse and reverses the oscillator output.
2. When the output voltage drops in the overload condition, the drive winding voltage of the primary side also goes down proportionally, and the Vin terminal voltage drops below the shutdown voltage to stop the operation.
3. In this case, as the circuit current also decreases simultaneously, the Vin terminal voltage increases again and the circuit operates intermittently by restoring the operation start voltage.
4. R830 and C825 construct the filter circuit that prevents malfunctions caused by the surge current generating at the MOSFET turn-ON. Threshold voltage at pin 7 is 0.95V.

7.5 Overload Protection Circuit

1. When the output voltage at secondary side falls below the overload mode, the auxiliary winding voltage of the primary side also falls proportionally, and the Vin terminal voltage falls below shutdown voltage to stop the operation.
2. Thus, the error-amplifier and photo-coupler in secondary side will be cut-off.
3. Threshold voltage at pin 5 is 5V.

7.6 Stand- by Operation

1. During standby operation, output voltage is decreased.
2. At the same time V2-V1 winding voltage is decreased, voltage at pin 4 also drops. It reaches operation stop voltage and IC801 stops its operation.
3. IC801 operates again when pin 4 voltage reaches the operation starting voltage when current flows through R818 and C816. The operation is repeated.
4. D862 and R867 are designed in such a way that when output voltage drops, error amplifier gain is reduced. Thus, resulting lower feedback current to IC801.