2024 Digital IC Design Homework II

NAME	
Student ID	

Functional Simulation Result

FIFO Pass	LIFO Pass	CIPU Pass

Stage 1

```
#
# There are total    0 errors in FIFO   !!
#
```

Stage 2

```
#
# There are total    0 errors in LIFO   !!
#
```

Stage 3

```
#
# There are total    0 errors in FIFO2 !!
#
```

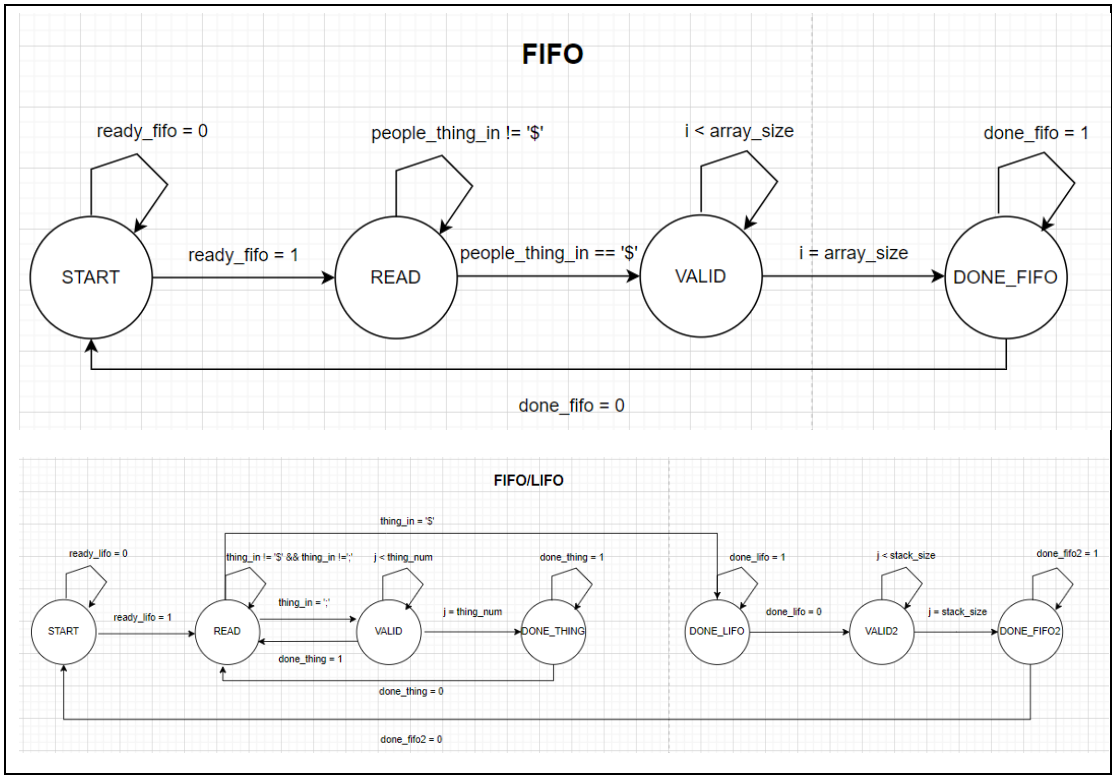
```
# ************************************************
# ***********      Simulation Start      ***********
# ************************************************
#
#
# There are total    0 errors in FIFO   !!
#
#
# There are total    0 errors in LIFO   !!
#
#
# There are total    0 errors in FIFO2 !!
#
#
#          ****************************
#          **                        **       |\__||
#          **  Congratulations!!     **      / O.O  |
#          **                        **    /_____   |
#          **  Simulation PASS!!     **   /^ ^ ^ \  |
#          **                        **  |^ ^ ^ ^ |w|
#          ****************************   \m___m__|_|
#
#          Correct / Total :   100 / 100
#
#
# ** Note: $finish    : E:/NCKU-Digital_IC_Design/HW2_P76124265/RTL/ref/tb.sv(300)
#    Time: 1365 ns  Iteration: 1  Instance: /textfixture
```

Description of your design

LIFO 和 LIFOFIFO 架構如下:

- State register: 循序電路，存 next stage 模組產生的 state
- Next stage: 組合電路，根據 input 和目前的 state 決定下一個 state
- Output logic: 循序電路，根據 state 決定 output
- Datapath: 循序電路，根據 state 和 input 進行運算

下圖是 FSM 的 state:


FIFO
ready_fifo = 0
people_thing_in != '$'
i < array_size
done_fifo = 1
START
ready_fifo = 1
READ
people_thing_in == '$'
VALID
i = array_size
DONE_FIFO
done_fifo = 0
FIFO/LIFO
thing_in = '$'
ready_lifo = 0
thing_in != '$' && thing_in !=';'
j < thing_num
done_thing = 1
done_lifo = 1
j < stack_size
done_fifo2 = 1
START
ready_lifo = 1
READ
thing_in = ';'
VALID
j = thing_num
DONE_THING
DONE_LIFO
done_lifo = 0
VALID2
j = stack_size
DONE_FIFO2
done_thing = 1
done_thing = 0
done_fifo2 = 0