2024 Digital IC Design
Homework 3: matrix multiplier

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Simulation Result

Functional simulation	Score: 100	Gate-level simulation	Score: 100	Clock width	25.0(ns)	Gate-level simulation time	137550 simulation time (ns)

your pre-sim result of test patterns

```
# Pattern 3 pass
# ---------------------------- Simulation FINISH !!----------------------------
# score =          100/100
# ============================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ============================================================================
# ** Note: $stop    : E:/Downloads/NCKU-Digital_IC_Design/HW3_P76124265/RTL/testfixture.v(351)
#    Time: 137550 ns  Iteration: 0  Instance: /testfixture1
# Break in Module testfixture1 at E:/Downloads/NCKU-Digital_IC_Design/HW3_P76124265/RTL/testfixture.v line 351
```

your post-sim result of test patterns

```
# Pattern 3 pass
# ---------------------------- Simulation FINISH !!----------------------------
# score =          100/100
# ============================================================================
#
#  \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!
#
# ============================================================================
# ** Note: $stop    : E:/Downloads/NCKU-Digital_IC_Design/HW3_P76124265/RTL/testfixture.v(351)
#    Time: 137550 ns  Iteration: 0  Instance: /testfixture1
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```

Synthesis Result

Total logic elements	453 / 55,856 (< 1 %)
Total memory bit	0 / 2,396,160 (0 %)
Embedded multiplier 9-bit element	1 / 308 (< 1 %)

your flow summary

Flow Summary

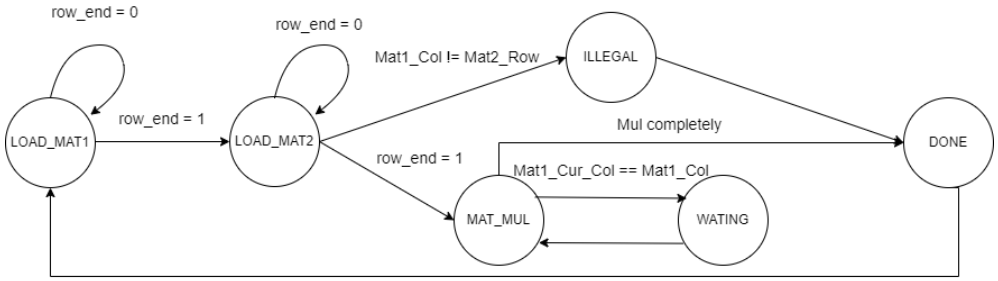
<<Filter>>

Flow Status	Successful - Wed May 08 14:47:25 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MM
Top-level Entity Name	MM
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	453 / 55,856 (< 1 %)
Total registers	310
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

MM 架構如下:

- State register: 循序電路，存 next stage 模組產生的 state
- Next stage: 組合電路，根據 input 和目前的 state 決定下一個 state
- Output logic: 循序電路，根據 state 決定 output
- Datapath: 循序電路，根據 state 和 input 進行運算



Load 完 mat1 和 mat2，如果 mat1 和 mat2 無法相乘，就進到 Illegal; 否則就到 MAT_MUL，MAT_MUL 將一個 row 乘一個 col 拆成 MAT1_COL 個 clock 完成，即每個 clock 只做一次乘法。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*