2024 Digital IC Design Homework 1

NAME	
Student ID	

Functional Simulation Result

Stage 1 Pass	Stage 2 Pass	Stage 3 Pass

Stage 1

```
VSIM 12> run -all
# ----------------------------------------
# -----------------Stage 1-----------------
# --------- ALU Simulation Begin ---------
# ----------------------------------------
# ----------------------------------------
# -------- ALU Simulation Success --------
# ----------------------------------------
# ----------------------------------------
# --------- ALU Simulation  End  ---------
# ----------------------------------------
#
```

Stage 2

```
# ----------------------------------------
# -----------------Stage 2-----------------
# ----- Comparater Simulation Begin -----
# ----------------------------------------
# ----------------------------------------
# ---- Comparater Simulation Success -----
# ----------------------------------------
# ----------------------------------------
# ------ Comparater Simulation End -------
# ----------------------------------------
#
```

Stage 3

```
# -----------------Stage 3-----------------
# ----------------------------------------
# ----- 2-input MAS Simulation Begin -----
# ----------------------------------------
# ----------------------------------------
# ---- 2-input MAS Simulation Success ----
# ----------------------------------------
# ----------------------------------------
# ------ 2-input MAS Simulation End ------
# ----------------------------------------
#
#                                      /|__/|
####################################  / 0,0  |
###            Pass!              ###  /_____   |
####################################  /^ ^ ^ \  |
#                                    |^ ^ ^ ^ |w|
#                                     \m___m__|_|
# ** Note: $finish    : C:/Users/p7612/Desktop/NCKU_Digital_IC_Design/HW1_P76124265/RTL/tb.v(163)
#    Time: 3007500 ps  Iteration: 1  Instance: /test
```

Description of your design

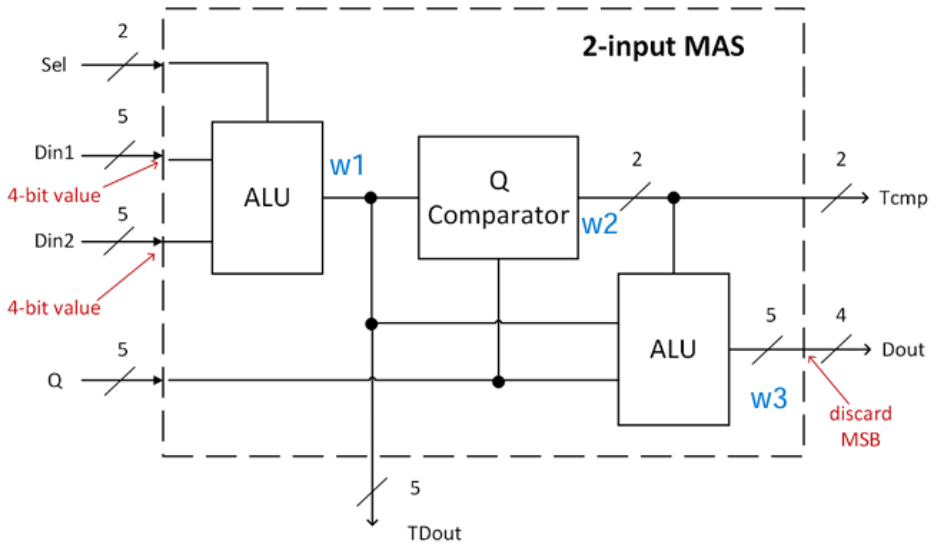

Fig. 1 The logic diagram of the 2-input MAS

設計圖如上

分成 **ALU.v、Q comparator.v、MAS_2input.v:**

ALU.v:

IO:

```
module ALU(
    input signed [4:0] Din1,
    input signed [4:0] Din2,
    input [1:0] Sel,
    output reg signed [4:0] Tmp
);
```

Sel == 2'b00, Tmp = Din1 + Din2;

Sel == 2'b11, Tmp = Din1 - Din2;

Sel == others, Tmp = Din1;

Q comparator.v:

IO:

```
module Q_Comparator(
    input signed [4:0] Din,
    input signed [4:0] Q,
    output [1:0] Tmp
);
```

assign Tmp[0] = (Din >= 0); assign Tmp[1] = (Din >= Q);

MAS_2input:

根據圖接線，w1 為 TDout、Q Comparator 的 Din; w2 為 ALU 的 SEL; w3 是 ALU Output，最後 discard w3 的 MSB 並輸出。