2024 Digital IC Design
Homework 4: Max-Priority Queue

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Simulation Result

Functional simulation	Score: 100	Gate-level simulation	Score: 100	Clock width	32 (ns)	Gate-level simulation time	(see below for details)

your pre-sim result of test patterns

P0

```
VSIM 11> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2010 ns  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

P1

```
VSIM 14> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2842 ns  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

P2

```
VSIM 17> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 3418 ns  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

P3

your post-sim result of test patterns

P0

```
VSIM 18> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2016827 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

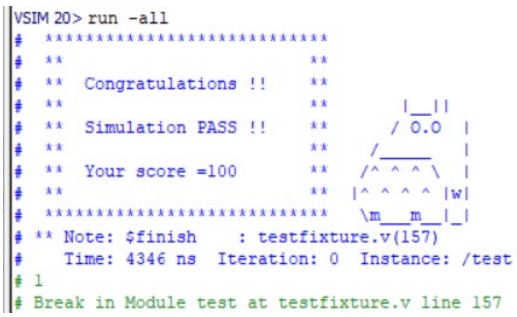
P1

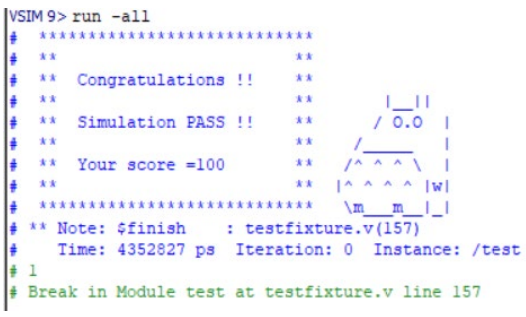
```
VSIM 15> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 2848827 ps  Iteration: 0  Instance: /test
# 1
```

P2

```
VSIM 12> run -all
#  ****************************
#  **                        **
#  **  Congratulations !!    **
#  **                        **        |__||
#  **  Simulation PASS !!    **       / 0.0  |
#  **                        **      /_____  |
#  **  Your score =100       **    /^ ^ ^ \  |
#  **                        **   |^ ^ ^ ^ |w|
#  ****************************    \m___m__|_|
# ** Note: $finish    : testfixture.v(157)
#    Time: 3424827 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at testfixture.v line 157
```

P3





Synthesis Result

Total logic elements	17695 / 55836 (32 %)
Total memory bit	0 / 2396160 (0 %)
Embedded multiplier 9-bit element	0 / 308 (0%)

your flow summary

Flow Summary

<<Filter>>

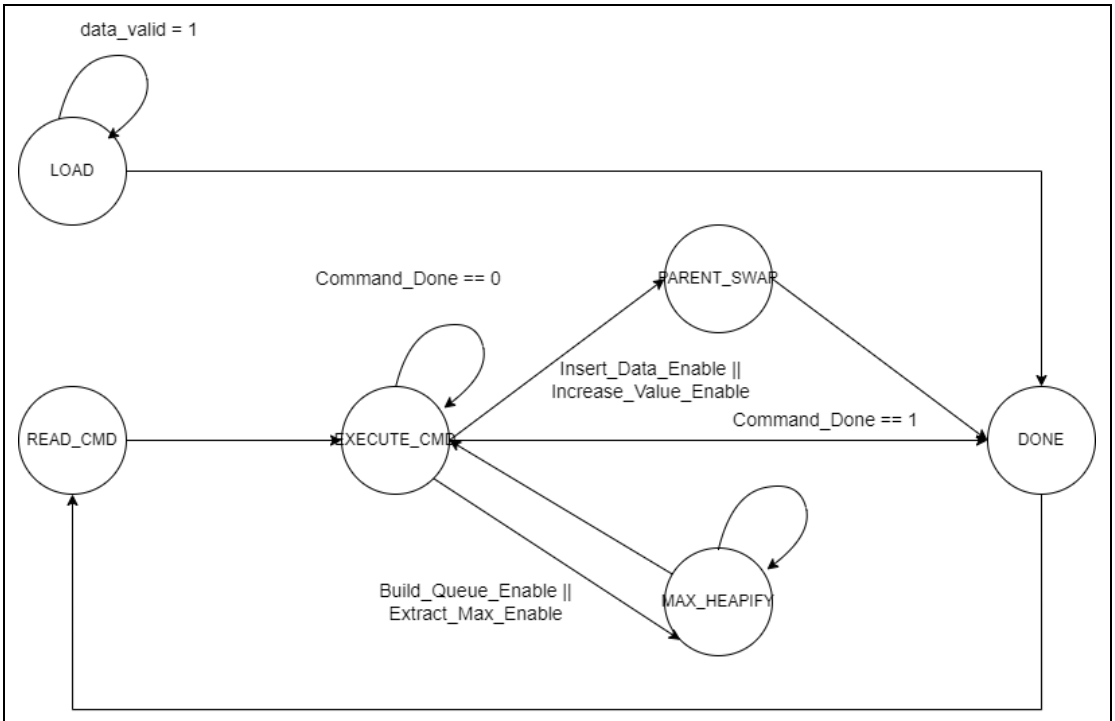
Flow Status	Successful - Sun May 26 15:10:55 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MPQ
Top-level Entity Name	MPQ
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	17,695 / 55,856 (32 %)
Total registers	2104
Total pins	50 / 325 (15 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

MPQ.v架構如下:

- State register: 循序電路，存 next stage 模組產生的 state
- Next stage: 組合電路，根據 input 和目前的 state 決定下一個 state
- Output logic && Datapath: 循序電路，根據 state 決定 output，和根據 state 和 input 進行運算

FSM state 如下:



分成 6 個 state，根據 cmd 的值執行不同指令。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*