2024 Digital IC Design

Homework 3: matrix multiplier

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| **Simulation Result** | | | | | | | | |
| Functional simulation | Score: 100 | | Gate-level simulation | Score: 100 | Clock  width | 25.0(ns) | Gate-level simulation time | 137550 simulation time (ns) |
| your pre-sim result of test patterns | | | | | your post-sim result of test patterns | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 453 / 55,856 ( < 1 % ) | | | |
| Total memory bit | | | | | 0 / 2,396,160 ( 0 % ) | | | |
| Embedded multiplier 9-bit element | | | | | 1 / 308 ( < 1 % ) | | | |
| your flow summary | | | | | | | | |
| **Description of your design** | | | | | | | | |
| MM架構如下:   * State register: 循序電路，存 next stage 模組產生的 state * Next stage: 組合電路，根據 input 和目前的 state 決定下一個 state * Output logic: 循序電路，根據 state 決定 output * Datapath: 循序電路，根據 state和 input 進行運算   Load 完 mat1 和 mat2，如果 mat1 和 mat2 無法相乘，就進到 Illegal; 否則就到 MAT\_MUL，MAT\_MUL 將一個 row 乘一個 col 拆成MATl\_COL個 clock 完成，即每個 clock 只做一次乘法。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*