2024 Digital IC Design

Homework 4: Max-Priority Queue

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| NAME | |  | | | | | | |
| Student ID | | P76124265 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Score: 100 | | Gate-level simulation | Score: 100 | Clock  width | 35 (ns) | Gate-level simulation time | ( see below for details ) |
| your pre-sim result of test patterns  P0    P1    P2    P3 | | | | | your post-sim result of test patterns  P0    P1    P2    P3 | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 19365 / 55836 (35 %) | | | |
| Total memory bit | | | | | 0 /2396160 (0 %) | | | |
| Embedded multiplier 9-bit element | | | | | 0 / 308 (0%) | | | |
| your flow summary | | | | | | | | |
| **Description of your design** | | | | | | | | |
| MPQ.v架構如下:   * State register: 循序電路，存 next stage 模組產生的 state * Next stage: 組合電路，根據 input 和目前的 state 決定下一個 state * Output logic && Datapath: 循序電路，根據 state 決定 output，和根據state和 input 進行運算   FSM state 如下:    分成 4 個 state，根據 cmd 的值執行不同指令。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*