HLS error-edits	1000 posts to get the categories			
	initial categories are based on analyzing 50 posts			
Csynq Failures				
1. Dynamic Memory Allocation!	52			
post	description	**How to fix suggested by experts**	**Implied Edits and Dependency**	
https://forums.xilinx.com/t5/Hig	[Divergence]why I get segmentation faults when running the Vivad	1. make big array static	make array static	
		2. use memory allocator / #ifdef statement with the __SYNTHESIS__ flag	-> use specific allocator / add pragma (SYNTHESIS)	
		3. increase the size of array / stack	-> increase the array size / restrict the size with special handling of corner cases	
		4. restrict the size. Handle the common cases but handle the beyond ones separately	-> completely rewrite the algorithm	
		5. completely rewrite the algorithm		
https://forums.xilinx.com/t5/Hig	design compiler doesn't synthesis shared memory / dynamic mem	use the RESOURCE pragma with core=RAM_1P_BRAM	add pragma (RESOURCE)	
https://forums.xilinx.com/t5/Hig	"unsupported memory access on variable 'line_buf_a' which is (or	The solution is to make it large enough for the maximum number of colum	make array static	-> increase the array size
https://forums.xilinx.com/t5/Hig	Calloc, Malloc and free	create your arrays with the maximum size you will need	estimate the expected max valu	-> allocate a max array
https://forums.xilinx.com/t5/Hig	segmentation fault with new() in C++	remove new() and check the read/write interface	replace new() with static allocat	-> read/write interface
2. Dataflow Optimizaton	161			
https://forums.xilinx.com/t5/Hig	Dataflow strict check failed	the student didn't follow dataflow pragma	update the dataflow pragma	-> check the system configuration
https://forums.xilinx.com/t5/Hig	HLS failed dataflow checking	turn out to be an HLS bug but can be avoid by merging two loops to a sing	merge two loops to a single loop	
https://forums.xilinx.com/t5/Hig	HLS failed dataflow checking: it should only be read in one proces	1. insert a pragma #pragma HLS INLINE in my_func	add pragma (inline, array_partition)	
		2. try array_partition pragma such that that each copy may be independantly optimized		
https://forums.xilinx.com/t5/Hig	HLS failed dataflow checking: cannot communicate over function (	Refactor the program. Data has to flow from one process to the next.	Refactor the dataflow	
https://forums.xilinx.com/t5/Hig	HLS cannot implement 'store' operation of constant 1 on array sig	remove the FIFO pragma	remove pragma	
https://forums.xilinx.com/t5/Hig	[Divergence] Difference between C-code, RTL-simulation and the	1. incorrect HLS version	Try out different FIFO sizes	
		2. change the FIFO size		
3. Type Error	257			
https://forums.xilinx.com/t5/Hig	Synthesizability check failed in C++ objects	1. use explict constructor	use explict constructor	
		2. "static" make the connecting stream "static"	"static" make the connecting stream "static"	
		3. provide a function name	provide a function name	
https://forums.xilinx.com/t5/Hig	unsupported pointer	make memory access to static	estimate array size	
			-> make array static	
			-> change pointer to array index	
https://forums.xilinx.com/t5/Hig	[Divergence] a fixed point arithmetic in HLS gives different results	possible	be careful of the bitwidth	
https://forums.xilinx.com/t5/Hig	bool type can't be resolved	typedef uint<1> data_bool;	use specific type with explicit bitwidth	
https://forums.xilinx.com/t5/Hig	STL items are not supported	You can use a fixed (known maximum sized) array instead. As for the dele	make array static	
https://forums.xilinx.com/t5/Hig	lots of errors	remove #define N 5. N is used as a template parameter almost everywher	check declaration of N	
https://forums.xilinx.com/t5/Hig	"no match for 'operator<<'" type conversion from uchar to float	no explicit type conversion in HLS. Anything that's currently "float" or "doul	add type casting	
https://forums.xilinx.com/t5/High-Level-Synthesis-HLS/How-to-convert-floating-point-to-fixed-point-using-System/m-p/817902				
https://forums.xilinx.com/t5/Hig	error when using custom type	use "typedef" to define a new type		
https://forums.xilinx.com/t5/Hig	[Divergence] caused by global variable			
4. Loop Optimization	161			
https://forums.xilinx.com/t5/Hig	The memory core 'RAM' has insufficient ports, for array 'data' in fu	change the while loop to for loop	transform while to for loop	
https://forums.xilinx.com/t5/Hig	[Divergence] for loop gives different result when overwriting in a lo	divergence caused by parallelism of the loop itself	return the explicit indexed item	
https://forums.xilinx.com/t5/Hig	[Divergence] top function skipping inner loop logic entirely, outputt	1. explict re-initialize array	explict re-initialize array	
		2. change variable / array to static	change variable / array to static	
https://forums.xilinx.com/t5/Hig	dataflow and unroll generate an error during the pre-synthesis	try out different combination options	pragma / directive exploration	
https://forums.xilinx.com/t5/Hig	loop failed synthesis check	misuse of pragma "stream"	insert pragma	
https://forums.xilinx.com/t5/Hig	[Divergence] loop gives a different result	Although the C simulation looks correct, there is no way to initialize the ar	add synsizable init() module	
			insert RESET pragma	
5. Top Function	198			
https://forums.xilinx.com/t5/Hig	cannot find top function	check project setting	update script	
7. Struct Error	141			
https://forums.xilinx.com/t5/Hig	pointer type member field	pointer->array index		
https://forums.xilinx.com/t5/Hig	pointer in a struct, linked list	struct -> static array		
https://forums.xilinx.com/t5/Hig	unsynthesizable struct type	1. array size should be known at compile time	fix array size	
		2. HLS was fully partitioning the structure, and then getting confused because not all elements were the si	-> fix the wide of all elements / insert pragma in top-level function	
		3. "#pragma HLS DATA_PACK variable=patch_pairs" (inside the top-level function) to force everything to be packed in together		
https://forums.xilinx.com/t5/Hig	fail to synthesis for struct with an array as one of the members	insert DATA_PACK pragma		
Co-sim Errors(Divergence)	**125**			
https://forums.xilinx.com/t5/Hig	segmentation fault with co-sim	write to an array out of bound	bug in code	
https://forums.xilinx.com/t5/Hig	csim / c syns passed, but cosim failed	there is no " " in the script	check the script file	
https://forums.xilinx.com/t5/Hig	array_partition in top function			

Csyns Failures	Counts	Repair Candidate	Performance Implication
Dynamic Memory Allocation/Deallocation	52	Specify the array size	Reduces communication frequency between CPU and FPGA
Dataflow Optimizaton	161	Type transformation, followed by explicittype casting and operator overloading	Segmenting data creates finer-grained tasks, leading to increased degree of parallelism
Type Error	257	Pragma exploration	Customizing data types reducesresource consumption, which directly impacts the paral-lelism level and operating frequency
Loop Optimization	161	Pragma exploration	Unrolling a loop appropriately leads to parallelization and performance improvement
Top Function	198	Insert an explict constructor andmake the connecting stream static	No significant impact on performance
Struct Error	141	Configuration exploration	Supporting structs andunions also reduces fallback and communication