Attempt all questions

Due Date: 16 March 2017, Thursday **(hard)**

1. Derived voltage gain for capacitor coupled two-stage Common Emitter (CE) Amplifier with circuit diagram and its h-parameter equivalent circuit. **(pages 378-381)**
2. Describe simple circuit diagram for two stage circuit with emitter follower output and its design procedure. **(pages 387-389)**
3. Describe operation of differential amplifier and derive the relation for voltage gain also input and output impedance. **(pages 399-405)**
4. Define parameters for operational amplifiers **(for questions 4 to 8 go through pages 465-485)**
    a. Input offset voltage
    b. input offset current
    c. common mode rejection ratio
    d. input bias current
5. Describe basic op-amp circuit consisting BJT as input and output stage and FET as input and output stages.
6. Describe about voltage follower circuits and why it is called so?
7. Write short notes on inverting and non-inverting amplifiers with appropriate circuit diagrams.
8. Derive expression for output voltage for summing amplifier and difference amplifier.

Lab Design assignment (will take viva for the problem)

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1. Do examples 12-1, 12-2, 12-3 **(pages 369-373)**
2. Do examples 12-4, 12-5 **(pages 376-378)**
3. Do examples 12-18, 12-19 **(pages 404-405)**