Features

HDMI Input

- True 4K/60 4:4:4 and HDR
- 18 Gb/s HDMI 2.0 compatible input port
- HDCP 2.2 and 1.4 support
- Support resolutions up to Ultra HD 4K x 2K 50/60 Hz, RGB/YCbCr with 4:4:4-pixel encoding
- Programmable EDID

HDMI Output

- True 4K/60 4:4:4 and HDR
- 18 Gbps HDMI 2.0 compatible output port
- HDCP 2.2 and 1.4 support
- Support resolutions up to Ultra HD 4x2K 50/60 Hz, RGB/YcbCr with 4:4:4 pixel encoding
- Read Display EDID

Audio IO

- Quad Synchronized I2S (slave) inputs for multichannel audio (up to 8 channels)
- Quad Synchronized I2S (master) stereo output for multichannel audio (up to 8 channels)
- Single Bidirectional I2S (master) (48kHz left justified)

10G IEEE 802.3 Transport

- XFI Compatible Interface
- 10GBASE-T 100m using Cat6a cabling or better
- Multi-mode fiber (SFP+) 300/550m with OM3/OM4 fiber
- Single-mode fiber (SFP+) UP TO 30KM
- Compatible with “off-the-shelf” standard 10G Ethernet switches
- IGMPv2 support for multicast channel management

Video Routing

- End to end latency under 120 microseconds when device set to Genlock mode
- Time to switch between sources (source switching time) in under 100 milliseconds (NT2000 only)
- Lightweight 1.4 to 1 artifact-free compression is used as needed when video exceeds 10G network bandwidth (e.g. 4K60 8-bit 4:4:4)

Audio Routing

- Lossless audio transmission
- Routing up to 8 channels of original HDMI audio
- Routing up to 8 channels of I2S audio
- HDMI downmixed stereo channel (NT2000 TX only)

1G IEEE 802.3 Transport

- RGMII compatible interface
- Extension of Gigabit Ethernet data network
- Built-in Ethernet switch connects 1GbE Ethernet to 10GbE interface
- Device Control

USB Over IP

- USB 2.0 with third party chipset (Icron)
- Full USB support, up to 480 Mbps

RS232

- Serial data routing between devices and between device and application control software
- 4x independent UART interfaces
- Baud rate up to 115 200
- Unicast and broadcast routing between devices

Infrared

- IR data routing between devices and between device and application control software
- ”Pronto” code injection and extraction from application control software

AV Processing (NT2000 only)

- Broadcast quality video upscaling and downscaling
- Color space, Chroma sampling and frame-rate conversion
- Multi-sources video compositing
- Video wall processing with bezel correction and display synchronization
- Downmixing multichannel HDMI LPCM audio

System control

- Remote device control using BlueRiver API over 1GbE or 10GbE interface
- Local I2C interface
- Remotely update devices using BlueRiver’s API over 1GbE or 10GbE interface
- Failsafe update using local fallback firmware

Applications

The Semtech BlueRiver platform offers a complete audio, video and control transceiver chipset designed from the ground up to address all professional AV market requirements.

- Two feature sets are available:
  - BlueRiver NT1000
  - BlueRiver NT2000
- Each have reference designs available, based on whether the AQLX107 or Kintex-7 device is being used as the implementation vehicle.

General Description

Using a synchronous, packet-based architecture for pixel transmission, the chipset can extend and independently switch video, audio, Gigabit Ethernet and other control signals through “off-the-shelf” 10G Ethernet switches.

This document targets technical managers and hardware engineers designing AV products and services using the AptoVision BlueRiver NT1000 and/or NT2000 chipsets.

It provides a comprehensive look at board design techniques for the successful implementation of transmitter and receiver devices based on the Semtech BlueRiver platform.

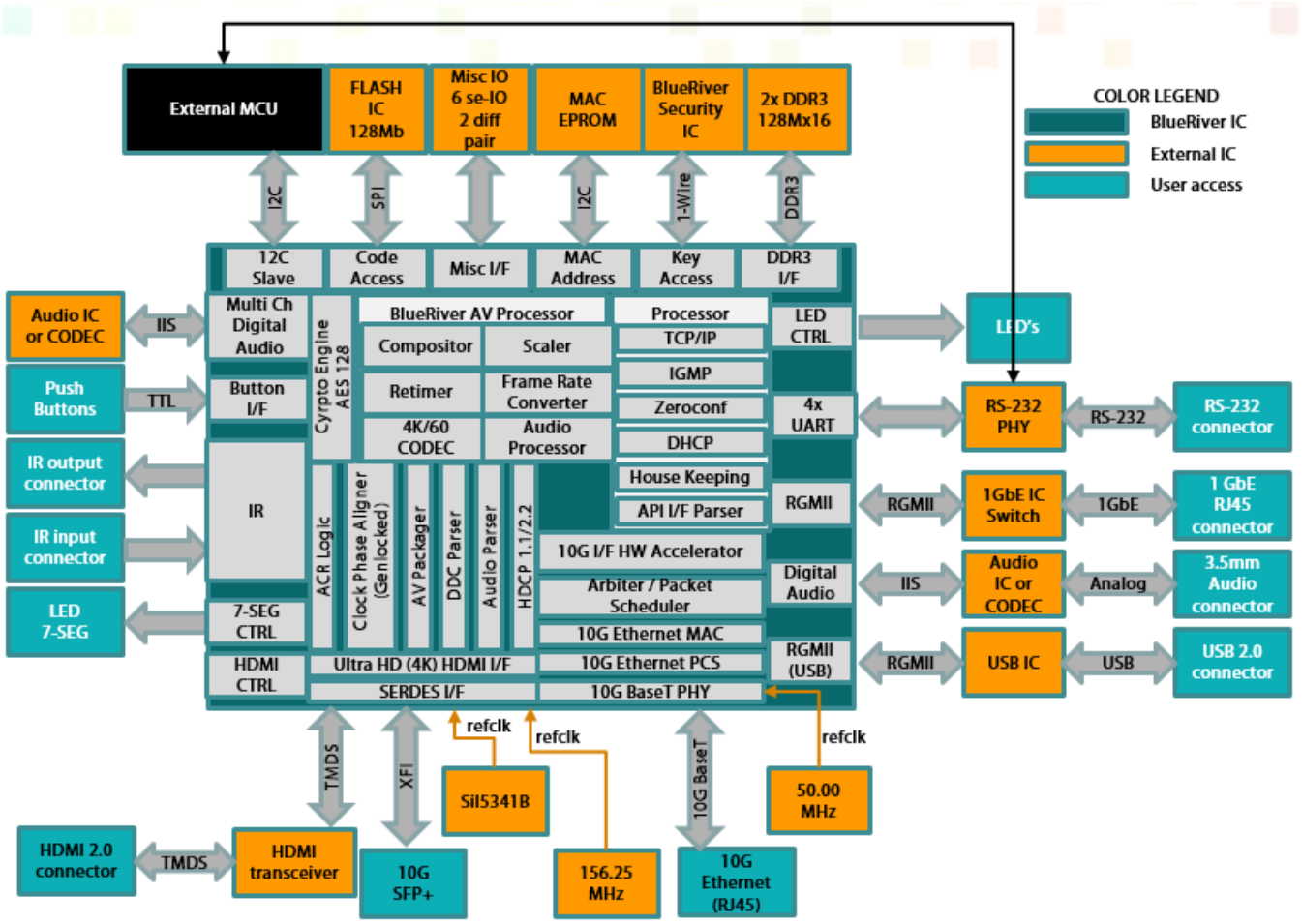

Figure 1 BlueRiver NT2000 Chipset

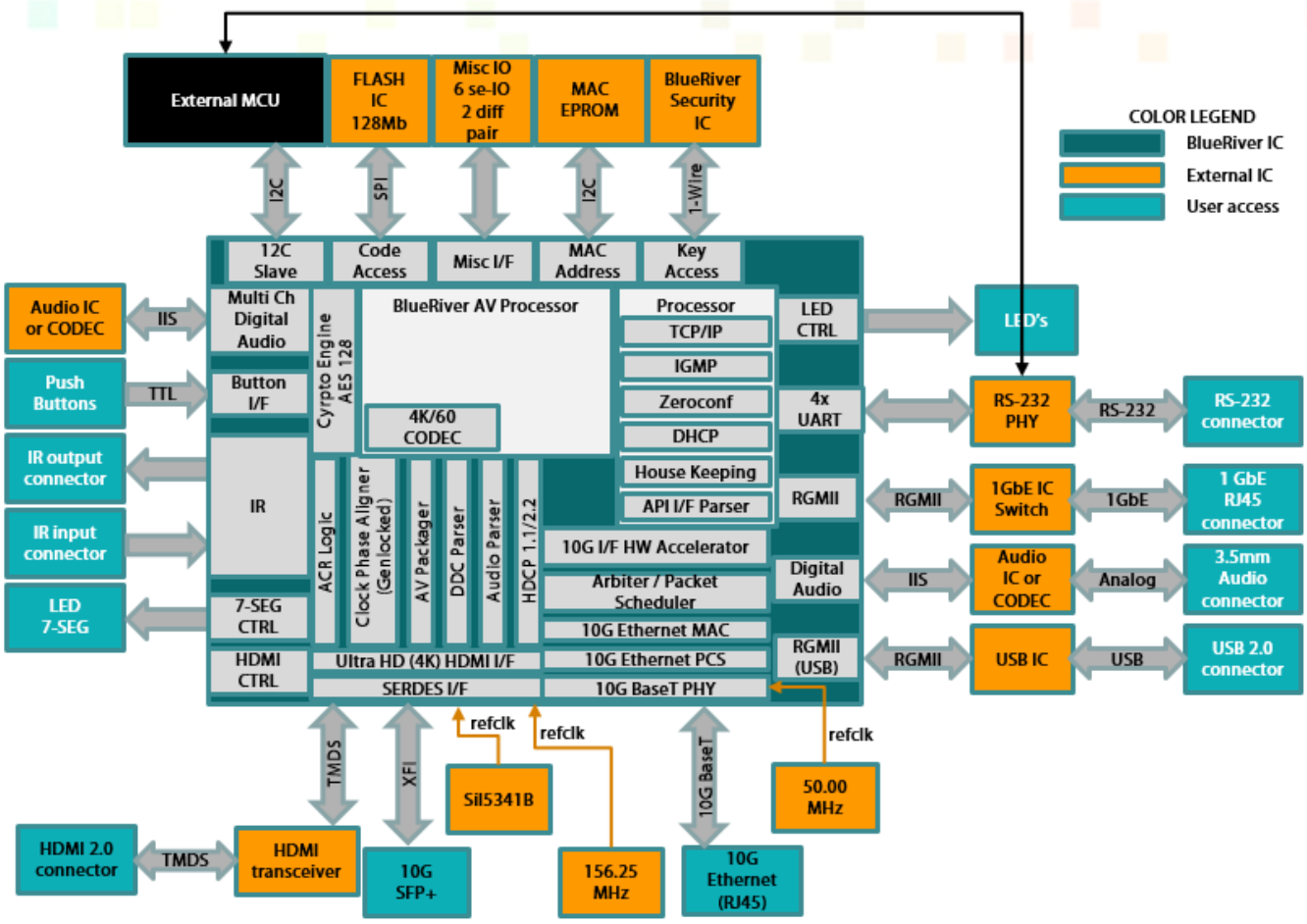

Figure 2 BlueRiver NT1000 Chipset

Revision History

Version	Date	Changes and/or Modifications
1.2	April 19, 2018	I2C register table updated.
1.1	April 16, 2018	Data updated for release 3.5, including I2C register table and added reference to AQLX107 dual mode BlueRiver authentication chip.
1.0	January 31, 2018	Initial release of document.

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1 Ball Out

The following section outlines the hardware interface description for the BlueRiver platform. There are two options available based on the implementation vehicle used, either the AQLX107 or the Kintex-7 160T. Refer to the appropriate section.

For details not covered here on these components recommend referring to the product's data sheets. Should be noted that a non-disclosure agreement could be required by the third party to be provided access by the third-party vendor.

- For additional information on either the Xilinx XC7K160T-2FBG484C4416 (commercial part) or the Xilinx XC7K160T-2FBG484I4416 (industrial part), referred to as the Kintex-7 160T in this document, refer to the data sheet Xilinx UG.475.
- For additional information on the AQLX107K7-B0000-S-C, referred to in this document simply as AQLX107, refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet.

1.1 BlueRiver NT2000 Ball Descriptions AQLX107

The series of tables outlined in the following section contain a list of the balls used and the key role they play for the BlueRiver chipset.

The AQLX107 is used in the following BlueRiver platform hardware reference designs:

Taizi:

- revision 1, pending release
- Schematic dated: January 2018 pending release

Princess:

- revision 4
- Schematic dated: Friday, December 15, 2017.

Duchess:

- revision 3
- Schematic dated: Friday, December 28, 2017.

Prince:

- revision 3
- Schematic dated: Friday, December 28, 2017.

Note: BOM and schematic provided only for Prince, no layout available for this design.

1.1.1 AQLX107 Clock Management

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_clk_mng_sda	Clock Mgt I2C interface data	Bidir	Y21	Pull Up	No	Yes
wb_clk_mng_scl	Clock Mgt I2C interface clock	Output	V20	Pull Up	No	Yes
ob_clk_mng_finc	Clock Mgt frequency increment	Output	W22	None	No	Yes
ob_clk_mng_fdec	Clock Mgt frequency decrement	Output	Y22	None	No	Yes
ob_clk_mng_duty_cycle	Clock Mgt duty cycle	Output	AB23	None	No	Yes

1.1.2 AQLX107 FPGA Configuration

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_fpga_config_flash_spi_si	SPI data from FPGA to serial FLASH	Output	P24	None	Yes	Yes
ob_fpga_config_flash_spi_cs_n	SPI chip selects from FPGA to serial FLASH • Active low	Output	R22	None	Yes	Yes
ib_fpga_config_flash_spi_so	SPI data from serial FLASH to FPGA	Input	N24	Pull Up	Yes	Yes

1.1.3 AQLX107 HDMI RX

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_rx_ddc_sda	HDMI RX DDC SDA	Bidir	Y18	Pull Up	Yes	No
wb_hdmi_rx_ddc_scl	HDMI RX DDC SCL	Bidir	AC10	Pull Up	Yes	No
wb_hdmi_rx_cec	HDMI RX CEC (Consumer Electronic Control) • Used to transmit control over HDMI cable	Bidir	AD23	Pull Up	Yes	No
ob_hdmi_rx_hpd	HDMI RX HPD (Hot Plug Detect) • Inform HDMI source sink is present.	Output	AD22	None	Yes	No
ib_hdmi_rx_tmds_d2_n	HDMI RX TMDS Data 2 differential input (positive lane)	Input	E4	None	Yes	No
ib_hdmi_rx_tmds_d2_p	HDMI RX TMDS Data 2 differential input (negative lane)	Input	E3	None	Yes	No
ib_hdmi_rx_tmds_d1_n	HDMI RX TMDS Data 1 differential input (positive lane)	Input	G4	None	Yes	No
ib_hdmi_rx_tmds_d1_p	HDMI RX TMDS Data 1 differential input (negative lane)	Input	G3	None	Yes	No
ib_hdmi_rx_tmds_d0_n	HDMI RX TMDS Data 0 differential input (positive lane)	Input	C4	None	Yes	No
ib_hdmi_rx_tmds_d0_p	HDMI RX TMDS Data 0 differential input (negative lane)	Input	C3	None	Yes	No
ib_hdmi_rx_tmds_clk_p	HDMI RX TMDS Clock differential input (positive lane)	Input	H5	None	Yes	No
ib_hdmi_rx_tmds_clk_n	HDMI RX TMDS Clock differential input (negative lane)	Input	H6	None	Yes	No
ib_hdmi_rx_5v	HDMI RX +5V signal • Informs HDMI RX module source available • Despite its name, it's not 5V compatible.	Input	Y16	None	Yes	No

1.1.4 AQLX107 HDMI Transceiver

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_xcvr_i2c_sda	HDMI transceiver I2C interface data	Bidir	AC20	Pull Up	Yes	Yes
wb_hdmi_xcvr_i2c_scl	HDMI transceiver I2C interface clock	Bidir	AC16	Pull Up	Yes	Yes
ob_hdmi_xcvr_rst_n	HDMI transceiver reset • Active low	Output	T19	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_si	HDMI transceiver FLASH configuration SPI interface serial out	Output	L24	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_cs_n	HDMI transceiver FLASH configuration SPI interface chip select • Active low	Output	H16	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_clk	HDMI transceiver FLASH configuration SPI interface clock	Output	G17	None	Yes	Yes
ib_hdmi_xcvr_int	HDMI transceiver interrupt	Input	P23	Pull Down	Yes	Yes
ib_hdmi_xcvr_flash_spi_so	HDMI transceiver FLASH configuration SPI interface serial in	Input	M21	None	Yes	Yes

1.1.5 AQLX107 HDMI TX

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_tx_ddc_sda	HDMI TX DDC SDA	Bidir	AB22	Pull Up	No	Yes
wb_hdmi_tx_ddc_scl	HDMI TX DDC SCL	Bidir	AC22	Pull Up	No	Yes
wb_hdmi_tx_cec	HDMI TX CEC (Consumer Electronic Control) • Used to transmit control over HDMI cable	Bidir	L18	Pull Up	No	Yes
ob_hdmi_tx_tmds_d2_p	HDMI TX TMDS Data 2 differential input (positive lane)	Output	D2	None	No	Yes
ob_hdmi_tx_tmds_d2_n	HDMI TX TMDS Data 2 differential input (negative lane)	Output	D1	None	No	Yes
ob_hdmi_tx_tmds_d1_p	HDMI TX TMDS Data 1 differential input (positive lane)	Output	F2	None	No	Yes
ob_hdmi_tx_tmds_d1_n	HDMI TX TMDS Data 1 differential input (negative lane)	Output	F1	None	No	Yes
ob_hdmi_tx_tmds_d0_p	HDMI TX TMDS Data 0 differential input (positive lane)	Output	H2	None	No	Yes
ob_hdmi_tx_tmds_d0_n	HDMI Receiver TMDS Data 0 differential input (negative lane)	Output	H1	None	No	Yes
ob_hdmi_tx_tmds_clk_p	HDMI TX TMDS Clock differential input (positive lane)	Output	D9	None	No	Yes
ob_hdmi_tx_tmds_clk_n	HDMI TX TMDS Clock differential input (negative lane)	Output	D10	None	No	Yes

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_hdmi_tx_5v	HDMI TX +5V signal • Despite its name, it's not 5V compatible • Inform sink module that source available	Output	AB11	None	No	Yes
ib_hdmi_tx_hpd	HDMI TX HPD (Hot Plug Detect) • Inform HDMI source a sink is present	Input	G18	None	No	Yes
ib_hdmi_tx_rec_clk_p	HDMI TX recovered clock (positive lane)	Input	H5	None	No	Yes
ib_hdmi_tx_rec_clk_n	HDMI TX recovered clock (negative lane)	Input	H6	None	No	Yes

1.1.6 AQLX107 ICRON USB

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_icron_mdio	ICRON MDIO	Bidir	L20	Pull Up	Yes	Yes
ob_icron_prog	ICRON	Output	H19	None	Yes	Yes
ov_icron_rx_data	ICRON	Output	3:W24 2:U24 1:R20 0:T20	None	Yes	Yes
ob_icron_usb_mode	ICRON	Output	P19	Pull Up	Yes	Yes
ob_icron_uart_rx	ICRON UART	Output	H23	None	Yes	Yes
ob_icron_rx_ctl	ICRON	Output	U23	None	Yes	Yes
ob_icron_rx_clk	ICRON	Output	U20	None	Yes	Yes
ob_icron_rst	ICRON Reset • Active low.	Output	M20	None	Yes	Yes
ob_icron_rex_lex_n	ICRON	Output	N23	Pull Up	Yes	Yes
ob_icron_phy2len	ICRON	Output	J20	None	Yes	Yes
ob_icron_pair_n	ICRON	Output	J18	None	Yes	Yes
ob_icron_clk_125	ICRON Reference CLK • Run at 125 MHz	Output	AD17	None	Yes	Yes
ob_icron_boot_sel0	ICRON	Output	K24	None	Yes	Yes
iv_icron_tx_data	ICRON	Input	3:R17 2:T17 1:T18 0:U22	None	Yes	Yes
ib_icron_vbus_en	ICRON	Input	J24	Pull Down	Yes	Yes
ib_icron_uart_tx	ICRON UART	Input	H24	Pull Up	Yes	Yes
ib_icron_tx_ctl	ICRON	Input	W23	None	Yes	Yes
ib_icron_tx_clk	ICRON	Input	V22	None	Yes	Yes
ib_icron_mdc	ICRON MDIO	Input	K18	Pull Up	Yes	Yes
ib_icron_link	ICRON	Input	J19	Pull Down	Yes	Yes
ib_icron_host	ICRON	Input	M19	Pull Down	Yes	Yes
ib_icron_eth_rst_n	ICRON	Input	AD21	Pull Down	Yes	Yes
ib_icron_activity	ICRON	Input	N19	Pull Down	Yes	Yes

1.1.7 AQLX107 Infrared

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_ir_data_out	Infrared output	Output	R21	None	Yes	Yes
ib_ir_data_in	Infrared input	Input	P21	Pull Down	Yes	Yes

1.1.8 AQLX107 MAC Flash

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_mac_sda	FLASH MAC I2C data	Bidir	AB14	Pull Up	Yes	Yes
wb_mac_scl	FLASH MAC I2C clock	Bidir	AB13	Pull Up	Yes	Yes

1.1.9 AQLX107 Memory (NT2000 only)

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ib_ddr3_clk_p	DDR3 Source Clock (Positive Lane)	Input	R7	Pull Up	Yes	Yes
ib_ddr3_clk_n	DDR3 Source Clock (Negative Lane)	Input	R8	Pull Down	Yes	Yes
ddr3_we_n	DDR3 Command • Write Enable (WE) • Active low	Output	N4	None	Yes	Yes
ddr3_reset_n	DDR3 Reset Active LOW	Output	L7	None	Yes	Yes
ddr3_ras_n	DDR3 Command • Row Access Strobe (RAS) • Active low.	Output	M4	None	Yes	Yes
ddr3_odt	DDR3 On-die termination • ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to DDR3 SDRAM	Output	0:M6	None	Yes	Yes
ddr3_dqs_p	DDR3 Data strobe • Output with read data • Edge-aligned with read data • Input with write data • Center-aligned to write data	Bidir	3:AB5 2:AD7 1:V3 0:Y4	None	Yes	Yes
ddr3_dqs_n	DDR3 Data strobe • Output with read data • Edge-aligned with read data • Input with write data • Center-aligned to write data	Bidir	3:AA5 2:AC7 1:V4 0:Y5	None	Yes	Yes
ddr3_dq	DDR3 Data input/output • Bidirectional data bus for x4 configuration	Bidir	31:Y6 30:AD6 29:AC3 28:AA6 27:AB4 26:AC6 25:AC4 24:AB6 23:Y8 22:AC8 21:Y9 20:AB9 19:AA8 18:AD5 17:AB8 16:AD4 15:W4 14:AA1 13:V6 12:W2 11:V7	None	Yes	Yes

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
			10:V1 9:W5 8:W1 7:AD2 6:AA2 5:AD3 4:Y3 3:AC1 2:Y2 1:AC2 0:W7			
ddr3_dm	DDR3 Input data mask • DM is mask signal for write data • Input data is masked when DM is sampled HIGH along with input data during write access	Output	3:AB3 2:AB7 1:V2 0:AA3	None	Yes	Yes
ddr3_cs_n	DDR3 Chip select • CS# enables (registered LOW) and disables (registered HIGH) command decoder • All commands masked when CS# registered HIGH	Output	0:N2	None	Yes	Yes
ddr3_cke	DDR3 Clock enable • CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on DRAM	Output	0:P2	None	Yes	Yes
ddr3_ck_p	Clock. Differential clock outputs • All address and control input signals are sampled on crossing of positive edge of ck_p and negative edge of ck_n • Input data strobe is referenced to crossings of ck_p and ck_n	Output	0:T5	None	Yes	Yes
ddr3_ck_n	Clock • Differential clock outputs • All address and control input signals sampled on crossing of positive edge of ck_p and negative edge of ck_n. Input data strobe referenced to crossings of ck_p and ck_n.	Output	0:T6	None	Yes	Yes
ddr3_ba	Bank address inputs • BA[2:0] define bank to which ACTIVATE, READ, WRITE, or PRECHARGE command applied	Output	2:M1 1:T1 0:L6	None	Yes	Yes
ddr3_addr	Address • Provide row address for ACTIVATE commands • Plus column address and auto pre-charge	Output	14:U4 13:K5 12:U5 11:T2 10:U6 9:K6 8:U3 7:L5 6:T3 5:L3 4:R3 3:L4 2:P4 1:R4 0:R2	None	Yes	Yes
ddr3_cas_n	Chip select:	Output	N3	None	Yes	Yes

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
	• CS# enables (registered LOW) and disables (registered HIGH) command decoder • All commands masked when CS# registered HIGH.					

1.1.10 AQLX107 Miscellaneous

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wv_gpio	General purpose IO	Bidir	11:AC12 10:M17 9:M16 8:L17 7:K17 6:J17 5:P16 4:L22 3:M22 2:J16 1:J22 0:K22	Pull Down	Yes	Yes
ov_led	LED used to show different FPGA status	Output	6:U18 5:U17 4:V19 3:AA24 2:Y23 1:W21	None	Yes	Yes
ob_int	FPGA interrupt to signal an event to an external microcontroller	Output	M24	None	Yes	Yes
ob_fan_ctrl	FAN control	Output	K23	None	Yes	Yes
iv_sw	Switch 1: Reset device to factory default. Switch 2: Reserved.	Input	2:U19 (unused) 1:AB24 (reset)	Pull Up	Yes	Yes
ib_rstn	FPGA Main reset	Input	R16	Pull Up	Yes	Yes

1.1.11 AQLX107 PHY 1GbE

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_phy_1g_sda	PHY 1G I2C interface SDA	Bidir	AB21	Pull Up	Yes	Yes
wb_phy_1g_scl	PHY 1G I2C interface (SCL)	Bidir	AA20	Pull Up	Yes	Yes
wb_phy_1g_gpio_3	PHY 1G General Purpose IO 3	Bidir	AB16	Pull Down	Yes	Yes
wb_phy_1g_gpio_2	PHY 1G General Purpose IO 2	Bidir	AB15	Pull Down	Yes	Yes
wb_phy_1g_gpio_0	PHY 1G General Purpose IO 0	Bidir	AC14	Pull Down	Yes	Yes
ov_phy_1g_rx_data	PHY 1G RGMII RX DATA • DDR interface	Output	3:AA18 2:AB17 1:AA19 0:AB18	None	Yes	Yes
ob_phy_1g_spdif	PHY 1G S/PDIF interface • Used in audio return channel feature when enabled.	Output	AB20	None	Yes	Yes
ob_phy_1g_rx_ctl	PHY 1G RGMII RX CTL	Output	W19	None	Yes	Yes
ob_phy_1g_rx_clk	PHY 1G RGMII RX CLK • Run at 125 MHz	Output	AD12	None	Yes	Yes
ob_phy_1g_rst_n	PHY 1G Reset. Active Low.	Output	AC13	None	Yes	Yes
ob_phy_1g_crs	PHY 1G GMII CRS Not used in RGMII interface.	Output	AA16	None	Yes	Yes
ob_phy_1g_col	PHY 1G GMII COL • Not used in RGMII interface.	Output	AA17	None	Yes	Yes

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_phy_1g_clk	PHY 1G Clock	Output	AC21	None	Yes	Yes
iv_phy_1g_tx_data	PHY 1G RGMII TX DATA • DDR interface synchronized with ib_rtl8305_p3_tx_ctl	Input	3:AD19 2:AD18 1:AC19 0:AC18	None	Yes	Yes
ib_phy_1g_tx_ctl	PHY 1G RGMII TX CTL	Input	W18	None	Yes	Yes
ib_phy_1g_tx_clk	PHY 1G RGMII TX clock • Run at 125 MHz	Input	AD13	None	Yes	Yes

1.1.12 AQLX107 QUAD I2S

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ov_quad_i2s_sd	QUAD I2S data out	Output	3:L19 2:K20 1:N21 0:AC24	None	Yes	Yes
ob_quad_i2s_ws	QUAD I2S ws out	Output	V21	None	Yes	Yes
ob_quad_i2s_sck	QUAD I2S serial clock out	Output	AD11	None	Yes	Yes
ob_quad_i2s_mclk	QUAD I2S master clock out	Output	L23	None	Yes	Yes
iv_quad_i2s_sd	QUAD I2S data in	Input	3:T22 2:T24 1:AA21 0:AA23	Pull Down	Yes	Yes
ib_quad_i2s_ws	QUAD I2S ws in	Input	AC15	Pull Down	Yes	Yes
ib_quad_i2s_sck	QUAD I2S serial clock in	Input	AD15	Pull Down	Yes	Yes
ib_quad_i2s_mute	QUAD I2S mute input	Input	N22	Pull Down	Yes	Yes
ib_quad_i2s_mclk	QUAD I2S master clock in	Input	AD10	Pull Down	Yes	Yes

1.1.13 AQLX107 Register Access

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_reg_sda	FPGA register I2C access (SDA)	Bidir	N16	Pull Up	Yes	Yes
wb_reg_scl	FPGA register I2C access (SDA)	Bidir	H18	Pull Up	Yes	Yes

1.1.14 AQLX107 Reserved

Notes:

1. Reserved pins are unused, they should not be connected and therefore have no direction or internal pull.
2. Pins present in the design schematic that are not listed in this table should be considered reserved.

Name	Description	AQLX Ball
Unassigned	Reserved	U21, U16, T16, P20, J14, J13, H11, G11, G10, F10, E10, C10, B9, AD9, AC9, AB10.

1.1.15 AQLX107 Security IC

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_security_chip	Security chip interface	Bidir	V24	None	Yes	Yes

1.1.16 AQLX107 SFP+

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
wb_sfp_sda	SFP+ control I2C interface SDA	Bidir	J11	Pull Up	Yes	Yes
wb_sfp_scl	SFP+ control I2C interface SCL	Bidir	J12	Pull Up	Yes	Yes
ob_sfp_tx_disable	SFP+ TX disable	Output	K16	None	Yes	Yes
ob_sfp_rate_sel	SFP+ rate select	Output	NOT USED	None	Yes	Yes
ib_sfp_present	SFP+ Present	Input	K10	Pull Up	Yes	Yes
ib_sfp_loss	SFP+ Loss	Input	J10	Pull Up	Yes	Yes

1.1.17 AQLX107 Single I2S

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_single_i2s_spi_sdin	Single I2S ADC/DAC control SPI SDIN Only Wolfson WM8731SEDS supported	Output	Y17	None	Yes	Yes
ob_single_i2s_spi_sclk	Single I2S ADC/DAC control SPI sclk Only Wolfson WM8731SEDS supported	Output	Y19	None	Yes	Yes
ob_single_i2s_spi_csb	Single I2S ADC/DAC control SPI csb Only Wolfson WM8731SEDS supported	Output	U15	None	Yes	Yes
ob_single_i2s_sd	Single I2S data out	Output	V16	None	Yes	Yes
ob_single_i2s_lrc	Single I2S lrc	Output	Y20	None	Yes	Yes
ob_single_i2s_dir	Single I2S direction	Output	W16	None	Yes	Yes
ob_single_i2s_bclk	Single I2S bclk	Output	V18	None	Yes	Yes
ob_single_i2s_mclk	Single I2S mclk	Output	V17	None	Yes	Yes
ib_single_i2s_sd	Single I2S data in	Input	AD16	Pull Down	Yes	Yes

1.1.18 AQLX107 UART

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_uart_4_tx	UART #4 Out	Output	H21	None	Yes	Yes
ob_uart_3_tx	UART #3 Out	Output	P18	None	Yes	Yes
ob_uart_2_tx	UART #2 Out	Output	K21	None	Yes	Yes
ob_uart_1_tx	UART #1 Out	Output	T23	None	Yes	Yes
ib_uart_4_rx	UART #4 In	Input	H22	Pull Up	Yes	Yes
ib_uart_3_rx	UART #3 In	Input	P17	Pull Up	Yes	Yes
ib_uart_2_rx	UART #2 In	Input	J21	Pull Up	Yes	Yes
ib_uart_1_rx	UART #1 In	Input	R23	Pull Up	Yes	Yes

1.1.19 AQLX107 XFI

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
ob_xfi_tx0_p	XFI Serial Out (positive lane)	Output	B6	None	Yes	Yes
ob_xfi_tx0_n	XFI Serial Out (negative lane)	Output	B5	None	Yes	Yes
ib_xfi_trx0_p	XFI Serial In (positive lane)	Input	C8	None	Yes	Yes
ib_xfi_trx0_n	XFI Serial In (negative lane)	Input	C7	None	Yes	Yes
ib_xfi_refclk_p	XFI Serial Clock (positive lane) • 156.25 MHz	Input	E7	None	Yes	Yes
ib_xfi_refclk_n	XFI Serial Clock (negative lane) • 156.25 MHz	Input	E8	None	Yes	Yes

1.1.20 AQLX107 10GbE RJ45

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
A_P	10GBASE-T MDI Pair A	Bidir	A19	None	Yes	Yes
A_N	10GBASE-T MDI Pair A	Bidir	A20	None	Yes	Yes
B_P	10GBASE-T MDI Pair B	Bidir	A22	None	Yes	Yes
B_N	10GBASE-T MDI Pair B	Bidir	A23	None	Yes	Yes
C_P	10GBASE-T MDI Pair C	Bidir	B24	None	Yes	Yes
C_N	10GBASE-T MDI Pair C	Bidir	C24	None	Yes	Yes
D_P	10GBASE-T MDI Pair D	Bidir	E24	None	Yes	Yes
D_N	10GBASE-T MDI Pair D	Bidir	F24	None	Yes	Yes

1.1.21 AQLX107 10GbE Management Interface

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
10G Management Interface	RG_B17	MDIO PHY Address	B17	Pull Up	Yes	Yes
10G Management Interface	RESET_N	Hard reset Input	A12	Pull Up	Yes	Yes

1.1.22 AQLX107 10GBASE-T Debug

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
smb_dat	Data signal for slave SMBus • used for debug port into PHY MDIO register space	Bidir	F14	None	Yes	Yes
smb_clk	Data signal for slave SMBus • used for debug port into PHY MDIO register space	Bidir	F15	None	Yes	Yes
smb_up_dat	Multi-master SMBus Data • used for inter-PHY communication and external SMBus control	Bidir	F16	None	Yes	Yes
smb_up_clk	Multi-master SMBus Data • used for inter-PHY communication and external SMBus control	Bidir	F17	None	Yes	Yes

1.1.23 AQLX107 JTAG

Name	Description	Direction	AQLX Ball	Internal Pull	BRNT TX	BRNT RX
tck	JTAG clock input • has associated pull-down	Input	G19	Pull Down	Yes	Yes
tdi	JTAG data input signal • has associated pull-down	Input	G22	Pull Down	Yes	Yes
tdo	JTAG data output signal • is 12 mA output • has associated pull-down	Output	G20	Pull Down	Yes	Yes
trst_n	JTAG reset signal • If JTAG not used, this pin must be pulled low • This input has pull-up associated with it	Input	G21	Pull Up	Yes	Yes
tms	JTAG test mode state signal • has associated pull-down with it	Input	G23	Pull Down	Yes	Yes

1.2 BlueRiver NT2000 Ball Descriptions Kintex-7 160T

The series of tables outlined in the following section contain a list of the balls used and the key role they play for the BlueRiver chipset.

The Kintex-7 is used in the following BlueRiver platform hardware reference designs:

Duchess:

- revision 3
- Schematic dated: Tuesday, November 28, 2017

Duke:

- revision 6
- Schematic dated: Wednesday, June 14, 2017

1.2.1 Kintex-7 160T Clock Management

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_clk_mng_sda	Clock Mgt I2C interface data	Bidir	P20	Pull Up	No	Yes
wb_clk_mng_scl	Clock Mgt I2C interface clock	Bidir	P21	Pull Up	No	Yes
ob_clk_mng_finc	Clock Mgt frequency increment	Output	N18	None	No	Yes
ob_clk_mng_fdec	Clock Mgt frequency decrement	Output	N19	None	No	Yes
ob_clk_mng_duty_cycle	Clock Mgt duty cycle	Output	R18	None	No	Yes

1.2.2 Kintex-7 160T FPGA Configuration

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_fpga_config_flash_spi_si	SPI data from FPGA to serial FLASH	Output	H18	None	Yes	Yes
ob_fpga_config_flash_spi_cs_n	SPI chip selected from FPGA to serial FLASH • Active low	Output	L16	None	Yes	Yes
ib_fpga_config_flash_spi_so	SPI data from serial FLASH to FPGA	Input	H19	Pull Up	Yes	Yes

1.2.3 Kintex-7 160T HDMI RX

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_rx_ddc_sda	HDMI RX DDC SDA	Bidir	V18	Pull Up	Yes	No
wb_hdmi_rx_ddc_scl	HDMI RX DDC SCL	Bidir	V17	Pull Up	Yes	No
wb_hdmi_rx_cec	HDMI RX CEC (Consumer Electronic Control) • Used to transmit control over HDMI cable	Bidir	N17	Pull Up	Yes	No
ob_hdmi_rx_hpd	HDMI RX HPD (Hot Plug Detect) • Inform HDMI source sink is present.	Output	P16	None	Yes	No
ib_hdmi_rx_tmds_d2_n	HDMI RX TMDS Data 2 differential input (positive lane)	Input	C4	None	Yes	No
ib_hdmi_rx_tmds_d2_p	HDMI RX TMDS Data 2 differential input (negative lane)	Input	C3	None	Yes	No
ib_hdmi_rx_tmds_d1_n	HDMI RX TMDS Data 1 differential input (positive lane)	Input	E4	None	Yes	No
ib_hdmi_rx_tmds_d1_p	HDMI RX TMDS Data 1 differential input (negative lane)	Input	E3	None	Yes	No
ib_hdmi_rx_tmds_d0_n	HDMI RX TMDS Data 0 differential input (positive lane)	Input	B6	None	Yes	No
ib_hdmi_rx_tmds_d0_p	HDMI RX TMDS Data 0 differential input (negative lane)	Input	B5	None	Yes	No
ib_hdmi_rx_tmds_clk_p	HDMI RX TMDS Clock differential input (positive lane)	Input	F6	None	Yes	No
ib_hdmi_rx_tmds_clk_n	HDMI RX TMDS Clock differential input (negative lane)	Input	F5	None	Yes	No
ib_hdmi_rx_5v	HDMI RX +5V signal. Informs HDMI RX module source available • Despite its name, it's not 5V compatible.	Input	V14	None	Yes	No

1.2.4 Kintex-7 160T HDMI Transceiver

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_xcvr_i2c_sda	HDMI transceiver I2C interface data	Bidir	U20	Pull Up	Yes	Yes
wb_hdmi_xcvr_i2c_scl	HDMI transceiver I2C interface clock	Bidir	AA14	Pull Up	Yes	Yes
ob_hdmi_xcvr_rst_n	HDMI transceiver reset • Active low	Output	J19	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_si	HDMI transceiver FLASH configuration SPI interface serial out	Output	D22	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_cs_n	HDMI transceiver FLASH configuration SPI interface chip select • Active low	Output	B17	None	Yes	Yes
ob_hdmi_xcvr_flash_spi_clk	HDMI transceiver FLASH configuration SPI interface clock	Output	A18	None	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ib_hdmi_xcvr_int	HDMI transceiver interrupt	Input	G18	Pull Down	Yes	Yes
ib_hdmi_xcvr_flash_spi_so	HDMI transceiver FLASH configuration SPI interface serial in	Input	B18	None	Yes	Yes

1.2.5 Kintex-7 160T HDMI TX

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_hdmi_tx_ddc_sda	HDMI TX DDC SDA	Bidir	P17	Pull Up	No	Yes
wb_hdmi_tx_ddc_scl	HDMI TX DDC SCL	Bidir	R17	Pull Up	No	Yes
wb_hdmi_tx_cec	HDMI TX CEC (Consumer Electronic Control) • used to transmit control over HDMI cable	Bidir	A14	Pull Up	No	Yes
ob_hdmi_tx_tmds_d2_p	HDMI TX TMDS Data 2 differential input (positive lane)	Output	A4	None	No	Yes
ob_hdmi_tx_tmds_d2_n	HDMI TX TMDS Data 2 differential input (negative lane)	Output	A3	None	No	Yes
ob_hdmi_tx_tmds_d1_p	HDMI TX TMDS Data 1 differential input (positive lane)	Output	B2	None	No	Yes
ob_hdmi_tx_tmds_d1_n	HDMI TX TMDS Data 1 differential input (negative lane)	Output	B1	None	No	Yes
ob_hdmi_tx_tmds_d0_p	HDMI TX TMDS Data 0 differential input (positive lane)	Output	D2	None	No	Yes
ob_hdmi_tx_tmds_d0_n	HDMI Receiver TMDS Data 0 differential input (negative lane)	Output	D1	None	No	Yes
ob_hdmi_tx_tmds_clk_p	HDMI TX TMDS Clock differential input (positive lane)	Output	H9	None	No	Yes
ob_hdmi_tx_tmds_clk_n	HDMI TX TMDS Clock differential input (negative lane)	Output	H8	None	No	Yes
ob_hdmi_tx_5v	HDMI TX +5V signal • despite name, it's not 5V compatible • inform sink module source available	Output	W15	None	No	Yes
ib_hdmi_tx_hpd	HDMI TX HPD (Hot Plug Detect) • inform HDMI source a sink is present	Input	B12	None	No	Yes
ib_hdmi_tx_rec_clk_p	HDMI TX recovered clock (positive lane)	Input	F6	None	No	Yes
ib_hdmi_tx_rec_clk_n	HDMI TX recovered clock (negative lane)	Input	F5	None	No	Yes

1.2.6 Kintex-7 160T ICRON USB

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_icron_mdio	ICRON MDIO	Bidir	C15	Pull Up	Yes	Yes
ob_icron_prog	ICRON	Output	A16	None	Yes	Yes
ov_icron_rx_data	ICRON	Output	3:F21 2:H22 1:E22 0:E21	None	Yes	Yes
ob_icron_usb_mode	ICRON	Output	B20	Pull Up	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_icron_uart_rx	ICRON UART	Output	C20	None	Yes	Yes
ob_icron_rx_ctl	ICRON	Output	J21	None	Yes	Yes
ob_icron_rx_clk	ICRON	Output	M20	None	Yes	Yes
ob_icron_rst	ICRON Reset • Active low	Output	C14	None	Yes	Yes
ob_icron_rex_lex_n	ICRON	Output	A21	Pull Up	Yes	Yes
ob_icron_phy2len	ICRON	Output	C13	None	Yes	Yes
ob_icron_pair_n	ICRON	Output	D14	None	Yes	Yes
ob_icron_clk_125	ICRON Reference CLK • run at 125 MHz	Output	AA15	None	Yes	Yes
ob_icron_boot_sel0	ICRON	Output	C22	None	Yes	Yes
iv_icron_tx_data	ICRON	Input	3:M17 2:H20 1:J20 0:J22	None	Yes	Yes
ib_icron_vbus_en	ICRON	Input	B22	Pull Down	Yes	Yes
ib_icron_uart_tx	ICRON UART	Input	C19	Pull Up	Yes	Yes
ib_icron_tx_ctl	ICRON	Input	G21	None	Yes	Yes
ib_icron_tx_clk	ICRON	Input	L20	None	Yes	Yes
ib_icron_mdc	ICRON MDIO	Input	E14	Pull Up	Yes	Yes
ib_icron_link	ICRON	Input	B16	Pull Down	Yes	Yes
ib_icron_host	ICRON	Input	A15	Pull Down	Yes	Yes
ib_icron_eth_rst_n	ICRON	Input	W22	Pull Down	Yes	Yes
ib_icron_activity	ICRON	Input	B15	Pull Down	Yes	Yes

1.2.7 Kintex-7 160T Infrared

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_ir_data_out	Infrared output	Output	L18	None	Yes	Yes
ib_ir_data_in	Infrared input	Input	K19	Pull Down	Yes	Yes

1.2.8 Kintex-7 160T MAC Flash

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_mac_sda	FLASH MAC I2C data	Bidir	U15	Pull Up	Yes	Yes
wb_mac_scl	FLASH MAC I2C clock	Bidir	T15	Pull Up	Yes	Yes

1.2.9 Kintex-7 160T Memory (NT2000 only)

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ib_ddr3_clk_p	DDR3 Source Clock (Positive Lane)	Input	P4	Pull Up	Yes	Yes
ib_ddr3_clk_n	DDR3 Source Clock (Negative Lane)	Input	R4	Pull Down	Yes	Yes
ddr3_we_n	DDR3 Command • Write Enable (WE)	Output	V2	None	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
	• Active low.					
ddr3_reset_n	DDR3 Reset • Active LOW	Output	R2	None	Yes	Yes
ddr3_ras_n	DDR3 Command • Row Access Strobe (RAS) • Active low.	Output	AA1	None	Yes	Yes
ddr3_odt	DDR3 On-die termination • ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to DDR3 SDRAM	Output	0:AB1	None	Yes	Yes
ddr3_dqs_p	DDR3 Data strobe • Output with read data • Edge-aligned with read data • Input with write data • Center-aligned to write data	Bidir	3:V10 2:U8 1:Y13 0:AA6	None	Yes	Yes
ddr3_dqs_n	DDR3 Data strobe • Output with read data • Edge-aligned with read data • Input with write data • Center-aligned to write data	Bidir	3:W10 2:V8 1:AA13 0:AB6	None	Yes	Yes
ddr3_dq	DDR3 Data input/output • Bidirectional data bus for x4 configuration	Bidir	31:T10 30:V9 29:U10 28:T9 27:U11 26:T8 25:T11 24:W9 23:Y6 22:U7 21:Y7 20:U6 19:Y8 18:R7 17:W6 16:R6 15:W12 14:V13 13:V12 12:AB11 11:AB13 10:U13 9:AA11 8:T13 7:AB8 6:AB5 5:AA9 4:AA5 3:AA10 2:AB7 1:AB10 0:AA8	None	Yes	Yes
ddr3_dm	DDR3 Input data mask • DM is mask signal for write data • Input data is masked when DM is sampled HIGH along with input data during write access	Output	3:U12 2:V7 1:AB12 0:W11	None	Yes	Yes
ddr3_cs_n	DDR3 Chip select • CS# enables (registered LOW) and disables (registered HIGH) command decoder	Output	0:AB2	None	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
	• All commands masked when CS# registered HIGH					
ddr3_cke	DDR3 Clock enable • CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on DRAM.	Output	0:AA3	None	Yes	Yes
ddr3_ck_p	Clock. Differential clock outputs • All address and control input signals are sampled on crossing of positive edge of ck_p and negative edge of ck_n • Input data strobe is referenced to crossings of ck_p and ck_n	Output	0:Y3	None	Yes	Yes
ddr3_ck_n	Clock • differential clock outputs • all address and control input signals sampled on crossing of positive edge of ck_p and negative edge of ck_n • input data strobe referenced to crossings of ck_p and ck_n	Output	0:Y2	None	Yes	Yes
ddr3_ba	Bank address inputs • BA[2:0] define bank to which ACTIVATE, READ, WRITE, or PRECHARGE command applied	Output	2:Y1 1:Y4 0:W1	None	Yes	Yes
ddr3_addr	Address • provide row address for ACTIVATE commands • plus column address and auto pre-charge	Output	14:T4 13:P2 12:P5 11:W5 10:N5 9:P1 8:U5 7:T1 6:V4 5:U2 4:AA4 3:U3 2:V3 1:T5 0:W4	None	Yes	Yes
ddr3_cas_n	Chip select: • CS# enables (registered LOW) and disables (registered HIGH) command decoder • All commands masked when CS# registered HIGH.	Output	W2	None	Yes	Yes

1.2.10 Kintex-7 160T Miscellaneous

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wv_gpio	General purpose IO	Bidir	11:AA16 10:F15 9:F16 8:G16 7:G15 6:G17 5:H15 4:J16 3:J17 2:H17 1:E17 0:E18	Pull Down	Yes	Yes
ov_led	LED used to show different FPGA status	Output	6:R21 5:R22 4:P22 3:M22 2:N22 1:K22	None	Yes	Yes
ob_int	FPGA interrupt to signal an event to an external microcontroller	Output	D21	None	Yes	Yes
ob_fan_ctrl	FAN control	Output	D20	None	Yes	Yes
iv_sw	Switch 1: Reset device to factory default. Switch 2: Reserved.	Input	2:L21 1:M21	Pull Up	Yes	Yes
ib_rstn	FPGA Main reset	Input	M18	Pull Up	Yes	Yes

1.2.11 Kintex-7 160T PHY 10GbE

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_phy_10g_mdio	MDIO data line	Bidir	D9	Pull Up	Yes	Yes
ob_phy_10g_tx_en	When pulled low, pin disables output line drivers on 10G PHY, and guarantees less than -53 dBm output power	Output	A9	None	Yes	Yes
ob_phy_10g_rst_n	Hard reset	Output	B8	None	Yes	Yes
ob_phy_10g_perst_n	PCI-Express Reset	Output	B10	None	Yes	Yes
ob_phy_10g_mdc	MDIO clock	Output	D10	None	Yes	Yes
ob_phy_10g_flsh_spi_sck	10G PHY FLASH CTRL clock	Output	F14	None	Yes	Yes
ob_phy_10g_flsh_spi_ce_n	10G PHY FLASH CTRL chip enable	Output	H12	None	Yes	Yes
ob_phy_10g_flsh_so	10G PHY FLASH CTRL data out	Output	E12	None	Yes	Yes
ib_phy_10g_wake	Wake signal	Input	C8	Pull Down	Yes	Yes
ib_phy_10g_rst_out_n	Reset signal from 10G PHY	Input	G10	Pull Up	Yes	Yes
ib_phy_10g_int_n	Interrupt signal from 10G PHY	Input	A8	Pull Up	Yes	Yes
ib_phy_10g_flsh_si	10G PHY FLASH CTRL data in	Input	E13	Pull Up	Yes	Yes
ib_phy_10g_clko_50m_a	Primary recovered clock output used for synchronous Ethernet	Input	G11	Pull Up	Yes	Yes

1.2.12 Kintex-7 160T PHY 1GbE

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_phy_1g_sda	PHY 1G I2C interface SDA	Bidir	U22	Pull Up	Yes	Yes
wb_phy_1g_scl	PHY 1G I2C interface (SCL)	Bidir	V22	Pull Up	Yes	Yes
wb_phy_1g_gpio_3	PHY 1G General Purpose IO 3	Bidir	W14	Pull Down	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_phy_1g_gpio_2	PHY 1G General Purpose IO 2	Bidir	Y14	Pull Down	Yes	Yes
wb_phy_1g_gpio_0	PHY 1G General Purpose IO 0	Bidir	W16	Pull Down	Yes	Yes
ov_phy_1g_rx_data	PHY 1G RGMII RX DATA. DDR interface	Output	3:Y22 2:AB22 1:Y21 0:AA21	None	Yes	Yes
ob_phy_1g_spdif	PHY 1G S/PDIF interface • used in audio return channel feature when enabled	Output	T20	None	Yes	Yes
ob_phy_1g_rx_ctl	PHY 1G RGMII RX CTL	Output	T21	None	Yes	Yes
ob_phy_1g_rx_clk	PHY 1G RGMII RX CLK • Run at 125 MHz	Output	W19	None	Yes	Yes
ob_phy_1g_rst_n	PHY 1G Reset • Active Low	Output	AB17	None	Yes	Yes
ob_phy_1g_crs	PHY 1G GMII CRS • not used in RGMII interface	Output	AB15	None	Yes	Yes
ob_phy_1g_col	PHY 1G GMII COL • not used in RGMII interface	Output	AB16	None	Yes	Yes
ob_phy_1g_clk	PHY 1G Clock	Output	W21	None	Yes	Yes
iv_phy_1g_tx_data	PHY 1G RGMII TX DATA • DDR interface synchronized with ib_rtl8305_p3_tx_ctl	Input	3:AA20 2:AA19 1:AB21 0:AB20	None	Yes	Yes
ib_phy_1g_tx_ctl	PHY 1G RGMII TX CTL	Input	U21	None	Yes	Yes
ib_phy_1g_tx_clk	PHY 1G RGMII TX clock • run at 125 MHz	Input	V19	None	Yes	Yes

1.2.13 Kintex-7 160T QUAD I2S

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ov_quad_i2s_sd	QUAD I2S data out	Output	3:A13 2:B13 1:A19 0:N20	None	Yes	Yes
ob_quad_i2s_ws	QUAD I2S ws out	Output	K21	None	Yes	Yes
ob_quad_i2s_sck	QUAD I2S serial clock out	Output	Y19	None	Yes	Yes
ob_quad_i2s_mclk	QUAD I2S master clock out	Output	D19	None	Yes	Yes
iv_quad_i2s_sd	QUAD I2S data in	Input	3:K17 2:G20 1:P19 0:R19	Pull Down	Yes	Yes
ib_quad_i2s_ws	QUAD I2S ws in	Input	Y16	Pull Down	Yes	Yes
ib_quad_i2s_sck	QUAD I2S serial clock in	Input	R16	Pull Down	Yes	Yes
ib_quad_i2s_mute	QUAD I2S mute input	Input	A20	Pull Down	Yes	Yes
ib_quad_i2s_mclk	QUAD I2S master clock in	Input	Y18	Pull Down	Yes	Yes

1.2.14 Kintex-7 160T Register Access

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_reg_sda	FPGA register I2C access (SDA)	Bidir	D12	Pull Up	Yes	Yes
wb_reg_scl	FPGA register I2C access (SDA)	Bidir	C12	Pull Up	Yes	Yes

1.2.15 Kintex-7 160T Reserved

Notes:

1. Reserved pins are unused, they should not be connected and therefore have no direction or internal pull.
2. Pins present in the design schematic that are not listed in this table should be considered reserved.

Name	Description	K7 Ball
Unassigned	Reserved	U16, M16, L19, K16, B21, AB18, AA18

1.2.16 Kintex-7 160T Security IC

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_security_chip	Security chip interface	Bidir	G22	None	Yes	Yes

1.2.17 Kintex-7 160T SFP+

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
wb_sfp_sda	SFP+ control I2C interface SDA	Bidir	G13	Pull Up	Yes	Yes
wb_sfp_scl	SFP+ control I2C interface SCL	Bidir	F13	Pull Up	Yes	Yes
ob_sfp_tx_disable	SFP+ TX disable	Output	E8	None	Yes	Yes
ob_sfp_rate_sel	SFP+ rate select	Output	F8	None	Yes	Yes
ib_sfp_present	SFP+ Rate present	Input	H10	Pull Up	Yes	Yes
ib_sfp_loss	SFP+ Loss	Input	G8	Pull Up	Yes	Yes

1.2.18 Kintex-7 160T Single I2S

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_single_i2s_spi_sdin	Single I2S ADC/DAC control SPI SDIN • Only Wolfson WM8731SEDS supported	Output	U17	None	Yes	Yes
ob_single_i2s_spi_sclk	Single I2S ADC/DAC control SPI sclk • Only Wolfson WM8731SEDS supported	Output	U18	None	Yes	Yes
ob_single_i2s_spi_csb	Single I2S ADC/DAC control SPI csb • Only Wolfson WM8731SEDS supported	Output	T19	None	Yes	Yes
ob_single_i2s_sd	Single I2S data out	Output	V20	None	Yes	Yes
ob_single_i2s_lrc	Single I2S lrc	Output	T18	None	Yes	Yes
ob_single_i2s_dir	Single I2S direction.	Output	W20	None	Yes	Yes
ob_single_i2s_bclk	Single I2S bclk	Output	Y17	None	Yes	Yes

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_single_i2s_mclk	Single I2S mclk	Output	W17	None	Yes	Yes
ib_single_i2s_sd	Single I2S data in	Input	T16	Pull Down	Yes	Yes

1.2.19 Kintex-7 160T UART

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_uart_4_tx	UART #4 Out	Output	F18	None	Yes	Yes
ob_uart_3_tx	UART #3 Out	Output	E16	None	Yes	Yes
ob_uart_2_tx	UART #2 Out	Output	C17	None	Yes	Yes
ob_uart_1_tx	UART #1 Out	Output	F20	None	Yes	Yes
ib_uart_4_rx	UART #4 In	Input	E19	Pull Up	Yes	Yes
ib_uart_3_rx	UART #3 In	Input	D17	Pull Up	Yes	Yes
ib_uart_2_rx	UART #2 In	Input	C18	Pull Up	Yes	Yes
ib_uart_1_rx	UART #1 In	Input	F19	Pull Up	Yes	Yes

1.2.20 Kintex-7 160T XFI

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
ob_xfi_tx0_n	XFI Serial Out (positive lane)	Output	F2	None	Yes	Yes
ob_xfi_tx0_p	XFI Serial Out negative lane)	Output	F1	None	Yes	Yes
ib_xfi_trx0_p	XFI Serial In (positive lane)	Input	G4	None	Yes	Yes
ib_xfi_trx0_n	XFI Serial In negative lane)	Input	G3	None	Yes	Yes
ib_xfi_refclk_p	XFI Serial Clock (positive lane). 156.25 MHz	Input	D6	None	Yes	Yes
ib_xfi_refclk_n	XFI Serial Clock (negative lane). 156.25 MHz	Input	D5	None	Yes	Yes

1.2.21 Kintex-7 160T JTAG

Name	Description	Direction	K7 Ball	Internal Pull	BRNT TX	BRNT RX
tck	JTAG clock input • has associated pull-down	Input	K7	Pull Down	Yes	Yes
tdi	JTAG data input signal • has associated pull-down	Input	K6	Pull Down	Yes	Yes
tdo	JTAG data output signal • is 12 mA output • has associated pull-down	Output	J6	Pull Down	Yes	Yes
tms	JTAG test mode state signal • has associated pull-down	Input	L6	Pull Down	Yes	Yes

2 Implementation Vehicles

The FPGA code for the BlueRiver NT1000/NT2000 can be run on different devices (vehicles), in accordance with the table supplied below:

Table 1: List of implementation vehicles for BlueRiver NT2000 and NT1000 chipsets

Product	Aquantia AQLX107	Xilinx Kintex-7 160T
NT2000 copper	Recommended	Requires external 10G PHY
NT2000 fiber	Suitable	Suitable
NT1000 copper	Recommended	Requires external 10G PHY
NT1000 fiber	Suitable	Suitable

For Copper designs, the `Aquantia AQLX107` is extremely well suited. This part integrates the Kintex-7 160T FPGA and the 10GBASE-T PHY into a single package, saving significant board real estate and complexity.

Notes:

i. For all new BlueRiver NT1000/NT2000 designs, Semtech's AptoVision Products Group strongly recommends using the Aquantia AQLX107.
ii. Legacy Copper designs can be implemented using discrete Kintex-7 160T FPGA when paired with a Broadcom BCM84851 10G PHY.
iii. For "fiber only" designs the Kintex-7 160T may be utilized if power consumption and cost are of concern.
iv. Starting in BlueRiver API version 3.13.0.0 and BlueRiver firmware 3.5.0.0, the BlueRiver AQLX107 supports both the copper and fiber interfaces being designed on the same hardware. These two interfaces can be switched between on "the fly". Should be noted however, that only one can be active at the same time.

2.1 Reference designs

Semtech offers several reference designs based on the chipset being implemented, refer to the table below for list of which designs implement which chipset and the device utilized.

Currently there is a series of BlueRiver NT1000/NT2000 reference designs available from Semtech AptoVision Products Group. Each design is "ready to manufacture" and includes the complete schematic, layout (Allegro file and Gerber's) and bill of materials (BOM).

Table 2: List of available reference designs

Reference Design	Chipset	Copper/Fiber	Device	Comment
Taizi	NT2000	Both	Aquantia AQLX107	Recommended reference design on which to base new projects.
Duchess	NT1000	Fiber	Kintex-7 160T	Minimalistic reference design for fiber. Lowest cost, smallest BOM.
Princess	NT1000	Copper	Aquantia AQLX107	Minimalistic reference design for copper. Lowest cost, smallest BOM.
Duke	NT2000	Both	Kintex-7 160T	Original reference design. Not recommended for new design projects.

Contact your Semtech AptoVision Products Group sales representative for details on obtaining the BlueRiver reference schematics and reference layout files.

2.1.1 Duchess

Duchess reference design is a BlueRiver NT1000 *fiber* design utilizing the Xilinx Kintex-7 160T and a SFP+ cage for flexible fiber optic design, allowing the choice of different 10G optical modules.

- Simple design, outlines what is possible in terms of minimum size, power and cost with the NT1000 fiber chipset.
- This design supports HDMI Video and Audio only. Does not include the BlueRiver AV Processor and so does not provide the auxiliary capabilities of the BlueRiver NT2000 chipset. Should be noted that this is not a limitation of BlueRiver NT1000 chipset but allows the simple minimalistic design.
- Includes the following for the BlueRiver TX Encoder and RX Decoder:
    - Schematics;
    - Layout;
    - and BOM.

2.1.2 Princess

Princess is a BlueRiver NT1000 *copper* reference design that utilizes the Aquantia AQLX107 to implement 10GBASE-T.

- Minimalistic design, showcasing what is possible in terms of minimum size, power and cost with the BlueRiver NT1000 chipset for 10G copper design.
- As with the Duchess, this design also supports HDMI Video and Audio only. It does not include the BlueRiver AV Processor, therefore does not provide the auxiliary capabilities of the BlueRiver NT2000 chipset. Should be noted that this is not a limitation of BlueRiver NT1000 chipset but allows for a simple minimalistic design.
- Includes the following for the BlueRiver TX Encoder and RX Decoder:
    - Schematics;
    - Layout;
    - and BOM.

2.1.3 Taizi

The Taizi design provides hardware designers and manufacturers a reference product design that can be deployed in high volume with minimal modifications. It is a fully featured NT2000 design, based on the Aquantia AQLX107.

Taizi is the newest reference design, as well as the one that Semtech AptoVision Products Group recommends referencing for all new BlueRiver design projects.

- Unlike the other BlueRiver ready-to-manufacture reference designs, this design provides more of a developer platform. Its exposes the NT2000 peripheral interfaces.
- Design can be manufactured in fiber and/or copper interface.
- It is designed as a transmitter (TX) encoder device or receiver (RX) decoder device.
- Suitable as a basis for BlueRiver NT1000 designs. Depopulate options such as the DDR.
- Includes the following for the BlueRiver TX Encoder and RX Decoder:
    - Schematics;
    - Layout;
    - and BOM.

2.1.4 Duke

This was the first BlueRiver hardware design implemented for the BlueRiver NT2000.

Note: When starting a new BlueRiver project, it is strongly advised to reference the "Taizi" hardware design, which allows for more flexibility and the use of an external microprocessor (recommended). It is not recommended to base new designs on the Duke reference design.

This BlueRiver reference design utilizes the Kintex-7 160T. It is a ready to manufacture BlueRiver NT2000 reference design that implements auxiliary features available on the BlueRiver platform.

- A single design that can be manufactured in fiber or copper, as well as either a transmitter (TX) encoder or receiver (RX) decoder device through a depopulation option.
- Uses Xilinx Kintex-7 160T in all configurations.
- Includes the following for the BlueRiver TX Encoder and RX Decoder:
    - Schematics;
    - Layout;
    - and BOM

3 BlueRiver Authentication Devices

BlueRiver NT2000 and NT1000 chipset functionality is enabled and licensed using dedicated BlueRiver authentication (security) devices.

- **Without this special authentication device, BlueRiver chipsets do not function.**
- The devices are available only from Semtech AptoVision Products Group or their authorized reseller partners (contact BlueRiver support for more details).
- The BlueRiver Authentication device is custom manufactured by Maxim for Semtech, refer to the DS28E10 datasheet for more details.

The table below lists available security devices along with their unique chip marking and associated chipset functionality.

Table 3: Chipsets and authentication devices

BlueRiver Chipset	Security Device part number	Security device marking
NT2000 fiber	AVBRNT+FITRX01-SD	44+1W22
NT2000 copper	AVBRNT+CUTRX01-SD	44+2W22
NT1000 fiber	AVBRNT1KFITRX01-SD	44+2W22
NT1000 copper	AVBRNT1KCUTRX01-SD	44+3W22

Following items should be noted:

1. The security device for NT2000 fiber can be used for NT2000 copper as well as NT1000 fiber or copper chipsets.
2. While security device for NT2000 copper and NT1000 fiber chipsets have different ordering part numbers, the actual security device is the same.
3. The security device for NT1000 fiber can also be used with NT1000 copper chipset.
4. The BlueRiver encoder or decoder devices can be built as a dual mode product (fiber and copper) using the AQLX107 fiber authentication device AVBRNT+FITRX01-SD. Planned for late spring 2018, the dual mode product will also be able to be built using the AVBRNT1KFITRX01-SD BlueRiver authentication device.

The picture provided below shows how the marking appears on a security device. Example shows values of `44+3W22`.

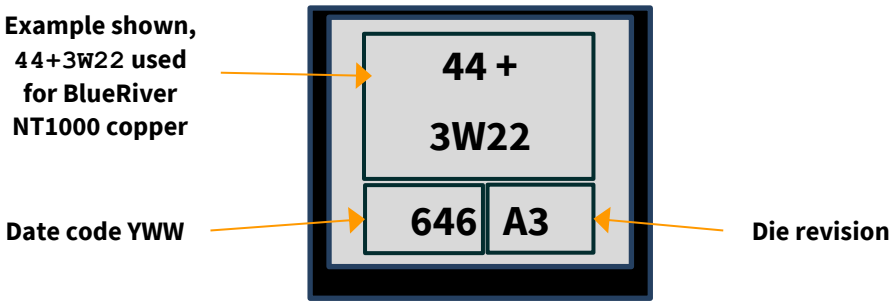


Figure 3: Security device marking

Note: The actual part number is broken up into two lines with '`44+`' shown on the first line and the remaining characters '`3W22`' displayed on the second line.

3.1 BlueRiver Authenticator Maximum Ratings

The table below indicates the absolute maximum ratings for the BlueRiver Authenticator.

- Stresses beyond those outlined in the table below could cause permanent damage to the device.
- These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Chipsets and authentication devices

Component	Maximum rating
IO Voltage to GND	-0.5V, +7V
IO Sink Current	20mA
VCC Voltage to GND	-0.5V, +7V
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

4 Electrical Characteristics

The information below applies to the BlueRiver FPGA chipset only, it outlines the power load in relation to the power rails used by the BlueRiver NT1000/NT2000 chipsets.

Important: Designers must be sure to consider all additional hardware subsystems when designing power delivery for the power rails required in their specific design(s).

4.1 Typical and Maximum Power Load Ratings

There are two sets of tables provided, one for the BlueRiver AQLX107 transmitter (TX) and receiver (RX) designs and a second set for the BlueRiver Kintex-7 160T designs. They illustrate typical and maximum power load related to the BlueRiver NT1000/NT2000 core system.

The tables provided show only power rails used by BlueRiver NT1000 and NT2000 chipsets and critical core components. These specific core components are the AQLX107 or Kintex-7 160T respectively.

Note: Not included in these tables are additional power use related to other design dependent subsystem components, such as HDMI transceiver, Gigabit switch, external PHY, USB, SFP+, etc.

4.1.1 AQLX107 typical and maximum power loads

Table 5: AQLX107 typical and maximum power loads for BlueRiver NT1000/NT2000 Copper designs

Power rail	Typical(2)	Maximum
	Current (mA) (1)	
P0V85	1570 (3)	3830 (4)
P1V0 (NT1000)	3550	3900
P1V0 (NT2000)	3750	4300
P1V2	862	1010
P1V35/P1V5 (NT2000)	297	624
P1V8	200	310
P2V1	340	435
P3V3	35	60
NT1000 AQLX Total Power	7.1 Watts	10.0 Watts
NT2000 AQLX Total Power	7.8 Watts	11.4 Watts

Notes:

(1) Currents and Power values are for the AQLX107 device only, 4K60 4:4:4 w/ high frequency pattern.
(2) Nominal supply voltages, 75°C junction temperature.
(3) 10Gb network with 30-meter CAT 6A cable.
(4) Under maximum supply voltages, 108°C junction temperature, 10Gb network with 100-meter CAT 6A cable.

Table 6: AQLX107 typical and maximum power loads for BlueRiver NT1000/NT2000 Fiber designs

Power rail	Typical(2)	Maximum
	Current (mA) (1)	
P0V85	100 (3)	3830
P1V0 (NT1000)	3550	3900
P1V0 (NT2000)	3750	4300
P1V2	382	1010
P1V35/P1V5 (NT2000)	297	624
P1V8	200	310
P2V1	15	435
P3V3	35	60
NT1000 AQLX Total Power	4.6 Watts	10.0 Watts
NT2000 AQLX Total Power	5.2 Watts	11.4 Watts

Notes:

(1) Currents and Power values are for the AQLX107 device only, 4K60 4:4:4 w/ high frequency pattern.

(2) Nominal supply voltages, 75°C junction temperature.
(3) Current after Copper PHY is disabled.

4.1.2 Kintex-7 160T typical and maximum power loads

Table 7: Kintex-7 160T typical and maximum power loads for BlueRiver NT1000/NT2000 Copper designs

Power rail	Typical[2]	Maximum
	Current (mA) [1]	
P1V0 (NT1000)	3550	3900
P1V0 (NT2000)	3750	4300
P1V2	352	500
P1V35/P1V5 (NT2000)	297	624
P1V8	200	310
P3V3	35	60
NT1000 Kintex-7 Total Power	4.4 Watts	5.3 Watts
NT2000 Kintex-7 Total Power	5.1 Watts	6.6 Watts

Notes:
(1) Currents and Power values are for the Kintex-7 160T device only, 4K60 4:4:4 w/ high frequency pattern.
(2) Nominal supply voltages, 75°C junction temperature.

Table 8: Kintex-7 160T typical and maximum power loads for BlueRiver NT1000/NT2000 Fiber designs

Power rail	Typical[2]	Maximum
	Current (mA)[1]	
P1V0 (NT1000)	3550	3900
P1V0 (NT2000)	3750	4300
P1V2	352	500
P1V35/P1V5 (NT2000)	297	624
P1V8	200	310
P3V3	35	60
NT1000 Kintex-7 Total Power	4.4 Watts	5.3 Watts
NT2000 Kintex-7 Total Power	5.1 Watts	6.6 Watts

Notes:
(1) Currents and Power values are for the Kintex-7 160T device only, 4K60 4:4:4 w/ high frequency pattern.
(2) Nominal supply voltages, 75°C junction temperature.

4.2 External Components

The following table shows the power usage of external components used in the BlueRiver NT1000/NT2000 chipsets.

Table 9: Typical and maximum power load for External parts of BlueRiver NT1000/NT2000 designs

Power rail	External Component	Typical	Maximum
		Current (mA)	
P1V35/P1V5	DDR Memory	1200	1500
P1V0	Silicon Image SiI9777 HDMI IC	1300	1400
P3.3V	10G Fiber SFP+ module	275	297

4.3 Recommended Operating Conditions

The table below outlines the recommended operating conditions.

Comment: For the power rails below that do not have minimum and/or maximum values specified refer to the third-party manufacturer for details.

Table 10: Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Junction Operating Temperature (applies to both Kintex-7 160T and AQLX107)	0.0	--	+85	˚C
P0V85[3]		0.85		
P1V0 (Aquantia)[3]	1.02		1.03	V
P1V0 (Kintex-7)[4]	1.02		1.03	V
P1V2	1.17	1.2	1.23	V
P1V35 (NT2000)	1.283	1.35	1.45	V
P1V5 (NT2000)	1.425	1.5	1.575	V
P1V8	1.75	1.8	1.85	V
P2V1[3]		2.1		V
P3V3	3.135	3.3	3.465	V

Notes:

1. These recommendations are based on the Semtech BlueRiver reference designs. Should the hardware design have been customized to include any replacement or additional components, these changes must be taken into consideration.
2. The junction temperature should be maintained at less than 85°C to ensure that parametric performance is maintained within this specification. The designer should ensure that there is sufficiently low thermal resistance to the circuit board and within the module to maintain this recommended junction temperature.
3. These apply only to designs that are based on the AQLX107 vehicle.
4. This applies only to designs that are based on the Kintex-7 160T vehicle.

4.4 Third Party Electrical Characteristics

Important note: Refer to data sheets of relevant **subsystem components** for additional information and data on elements not included here. This would include, but not be limited to:

- Refer to the Xilinx 7 Series FPGAs GTX/GTH Transceivers User Guide UG476 for more information about the MGTAVCC.
- Refer to the Xilinx 7 Series FPGAs PCB Design Guide UG483 for more information about the VCCINT.
- Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more details regarding the power characteristics.

4.5 Planning power rail usage

Important when implementing BlueRiver NT1000 and BlueRiver NT2000 designs to correctly design all power supplies.

In general, Power Rails do not allow more than 5% variations to their nominal rail. This 5% needs to account for both load variations and temperature variations.

The video nature of this product can produce large dI/dt variations as during blanking not much processing occurs but at the start of active video many transistors start to **simultaneously** toggle.

The following ground rules must be applied:

- Voltage Feedback of DC-DC switcher must be taken as close as possible to the load. This will compensate for resistive loss in the power path.
- Low ESR ceramic capacitors (2.2 uF X5R suggested) must be installed near each Power pin to bypass mid-frequency transients.
- Low ESR bulk capacitors (high-density aluminum poly capacitors with 5 mΩ average ESR are suggested) should be connected within 1 inch (25.4 mm) of the load to filter low-frequency transients.
- On all analog supplies (e.g. P1V0_A1, P1V2_A2 and P2V1) extra care must be taken to avoid coupling between planes. This is especially true for all deterministic noise around the Megahertz area (e.g. switcher noise or flicker noise).
- For example, providing a fill-area of an analog rail if the plane over (or under) it is digital is strongly not recommended. The switching behavior of the digital plane will induce deterministic noise on the analog one.

Refer to section 6 Power Delivery for details on power delivery to the BlueRiver NT1000/NT2000 implementation vehicles and critical subsystems, specifically:

- AQLX107 or Kintex-7 160T
- DDR3 memory
- Silicon Labs SI5341B

Not included in this data sheet are power loads for subsystems that are design dependent, such as but not limited to:

- HDMI transceiver, if other than the Silicon Image SiI9777 HDMI IC is used.
- Ethernet 1GbE switch
- Audio subsystem
- Microcontroller
- USB0
- RS232 and IR

5 Hardware Interface description

In this section, the various I/O interfaces that are connected to the BlueRiver NT1000 and NT2000 chipsets are described.

Majority of interfaces described below are found on both the BlueRiver NT1000 and BlueRiver NT2000 chipsets for both transmitter (TX) and receiver (RX) devices. For this reason, no distinction is made between transmitters and receivers, **except** when the interface in question is applicable only to a BlueRiver NT2000 chipset or a transmitter or receiver device.

The BlueRiver interfaces presented are outlined earlier in Figure 1 BlueRiver NT2000 Chipset and Figure 2 BlueRiver NT1000 Chipset.

5.1 I2C Slave Interface

The BlueRiver NT2000 and NT1000 chipset have one I^2C Slave Bus interface.

- The I^2C slave port is standard mode (100Kbit/s) and full speed (400Kbit/s) capable.
- It supports byte read/write operations in addition to burst read/write operations.

The 7-bit binary address of the I2C slave module is:

- 1001100R (left aligned) where R = 1 sets a read operation while R = 0 sets a write operation.
- Therefore, the I^2C slave port address is 0x98/0x99**.**

Note: Refer to the figures provided below for examples. The first figure outlines the I^2C Byte Read operation and the second the I^2C Byte Write operation.

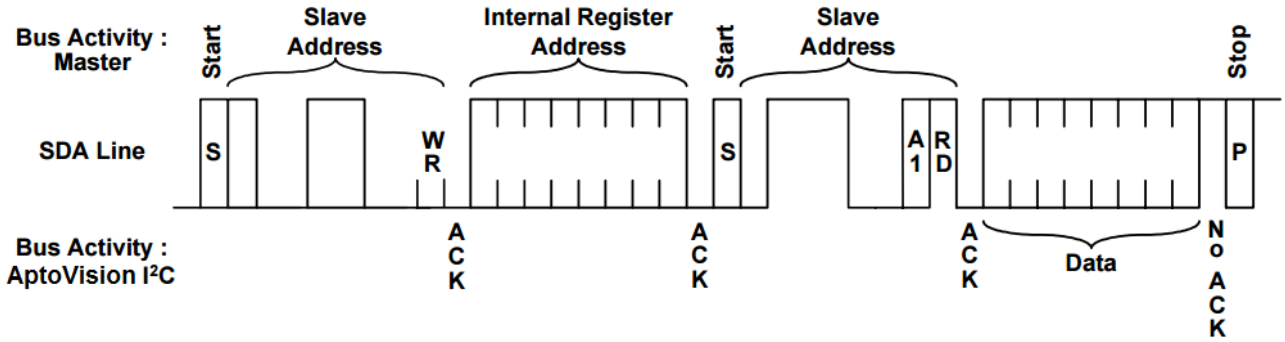


Figure 4: I2C Byte Read

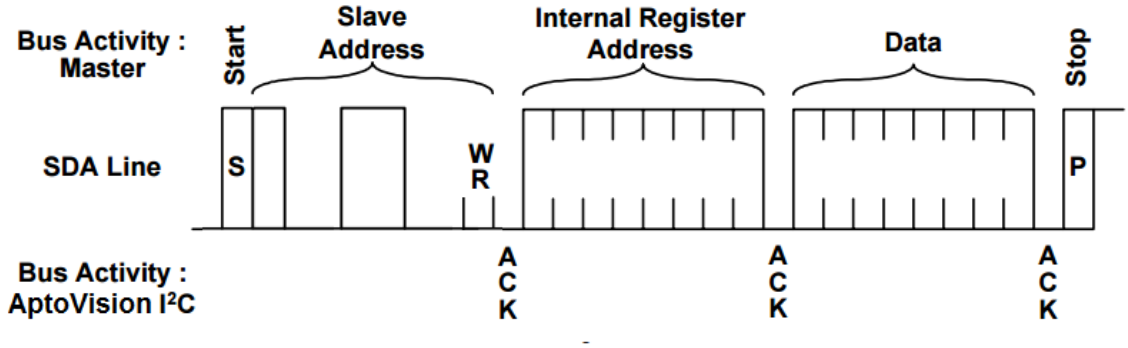


Figure 5: I2C Byte Write

The table below illustrates the BlueRiver NT1000 and NT2000 I2C Registers.

Table 11: NT2000 and NT1000 I2C register table

Address	Register	Type	Field/ Rgty	bit offset	bit width	Range	Default	Comment
0x00	mac_addr_lsb	R	data	0	32	[31:0]	0	MAC address of the FPGA 4 LSB
0x04	mac_addr_msb	R	data	0	16	[15:0]	0	MAC address of the FPGA 2 MSB
0x08	ip_addr	R	data	0	32	[31:0]	0	IP address of the FPGA
0x0c	ip_submask	R	data	0	32	[31:0]	0	Submask of the FPGA
0x10	ip_gateway	R	data	0	32	[31:0]	0	Gateway of the FPGA
0X14	ctrl_0	R	ip_mode	0	1	[0]	0	Control register IP mode: 0=DHCP; 1=Manual
			udp_port	16	16	[31:16]	0	UDP port used by the FPGA
0x18	temp	R	junction	0	12	[11:0]	0	Temperature value for core of the FPGA. Tc = (junction_temp*126-279706) / 1024

Address	Register	Type	Field/ Rgty	bit offset	bit width	Range	Default	Comment
0x1C	hdmi	VOLATILE						HDMI HDCP config/status
		TX chipset: W RX chipset: R	hdcp_en	0	1	[0]	0	HDCP enabled
		TX chipset: W Rx device: R	hdcp_2_2_en	1	1	[1]	0	HDCP 2.2 enabled
		TX chipset: W Rx chipset: R	hdcp_2_2_type	2	1	[2]	0	HDCP 2.2 content stream type: 0 = Type 0 1 = Type 1
		TX chipset: R RX chipset: W	hpd_source	16	1	[16]		HPD source: 0= use external pin 1 = use hpd_value field
		TX chipset: R RX chipset: W	hdp_value	17	1	[17]		HDP value
0x20	event	CLW_BIT						HDMI HDCP config/status event
		TX chipset: N/A RX chipset: RO	hdcp_en	0	1	[0]	0	HDCP enabled event
		TX chipset: N/A RX chipset: RO	hdcp_2_2_en	1	1	[1]	0	HDCP 2.2 enabled event
		TX chipset: N/A RX chipset: RO	hdcp_2_2_type	2	1	[2]	0	HDCP 2.2 content stream type event: 0 = Type 0 1 = Type
		TX chipset: RO RX chipset: N/A	hpd_source	16	1	[16]		HPD source event
		TX chipset: RO RX chipset: N/A	hpd_value	17	1	[17]		HPD value event
0X24	event_mask	RW						HDMI HDCP config/status event mask
		TX chipset: N/A RX chipset:	hdcp_en	0	1	[0]	0	HDCP enabled event mask

Address	Register	Type	Field/ Rgty	bit offset	bit width	Range	Default	Comment
		W						
		TX chipset: N/A RX chipset: W	hdcp_2_2_en	1	1	[1]	0	HDCP 2.2 enabled event mask
		TX chipset: N/A RX chipset: W	hdcp_2_2_type	2	1	[2]	0	HDCP 2.2 content stream type event mask: 0 = Type 0 1 = Type 1
		TX chipset: W RX chipset: N/A	hpd_source	16	1	[16]	0	HPD source event mask
		TX chipset: W RX chipset: N/A	hpd_value	17	1	[17]	0	HPD value event mask
0x60	ctrl_1	R	hdcp_support_type	0	2	[1:0]	0	0x00 : Support HDCP 1.4 & 2.2 0x01 : Support HDCP 1.4 only 0x02 : HDCP disabled
			error_code	8	8	[8:15]		Error code when "error_present" bit is set. For list of errors refer to section 5.18.1 7-Segment Display (Available since version 3.5.0.0)
			error_present	16	1	[16]		Error present bit. This bit set to '1' when error occurs. Refer to “error_code" bits for more information. (Available since version 3.5.0.0)
			boot_image	17	1	[17]	0	This bit provides status on code that is currently running, Multi or Golden. 0 : Booted using Golden image (backup application) 1 : Booted using Multi image

Address	Register	Type	Field/ Rgty	bit offset	bit width	Range	Default	Comment
								(normal application) (Available since version 3.5.0.0)
			10G_interface_is_up	18	1	[18]	0	This bit indicates 10GbE interface connection status: 0 : Down 1 : Up (Available since version 3.4.2.0 and 3.5.0.0)
			P2P_is_active	19	1	[19]	0	This bit indicates the network connection type: 0 : Network switch mode 1 : Point To Point mode (Available since version 3.5.0.0)
0X80	ext_cpu_event	WSET	event	0	32	[31:0]	0	External CPU event. 32 user defined application messages. • This allows external CPU to report events to its application level through BlueRiver API. • Write to set and poll for acknowledge. Write 1: Request to send Read 1: Not yet processed. Read 0: Request completed. (Available since version 3.5.0.0)

5.2 Flash IC

The FLASH IC stores the FPGA firmware code. This includes both the FPGA Multiboot and the Golden firmware.

- Multiboot firmware is the default firmware that is loaded into the device.
- Golden firmware is the 'failsafe' firmware in case the Multiboot firmware becomes corrupted.
- The Flash IC also stores all non-volatile device settings.

A 128-Mbit SPI flash is required.

Semtech AptoVision Products Group has qualified the Winbond W25Q128FVSIG and Winbond W25Q128FVSIGQ.

Warning! An alternate 128 Mbit SPI flash from a different vendor can be used but they need to be qualified by the customer. Contact BlueRiver support for more information.

For details on initial programming and updating of BlueRiver devices, refer to the application note, BlueRiver Programming of Configuration Flash (an_0025).

5.3 MAC EPROM

The purpose of the MAC EPROM IC is to hold a unique MAC address for a BlueRiver NT1000 or NT2000 transmitter or receiver device. This MAC address is used in all Ethernet communication.

The BlueRiver FPGA communicates with this IC via the I2C interface.

- If the communication is not functioning correctly, an error message is displayed on the 7-segments display.

For the MAC EPROM, Semtech recommends the 24AA02E48 from Microchips Technology. This part comes with a unique MAC address already programmed into the EPROM.

To use purchased MAC addresses, any compatible EPROM device can be used. The MAC address **must** be written into EPROM at address **0xFa-0XFF** as shown in the figure below:

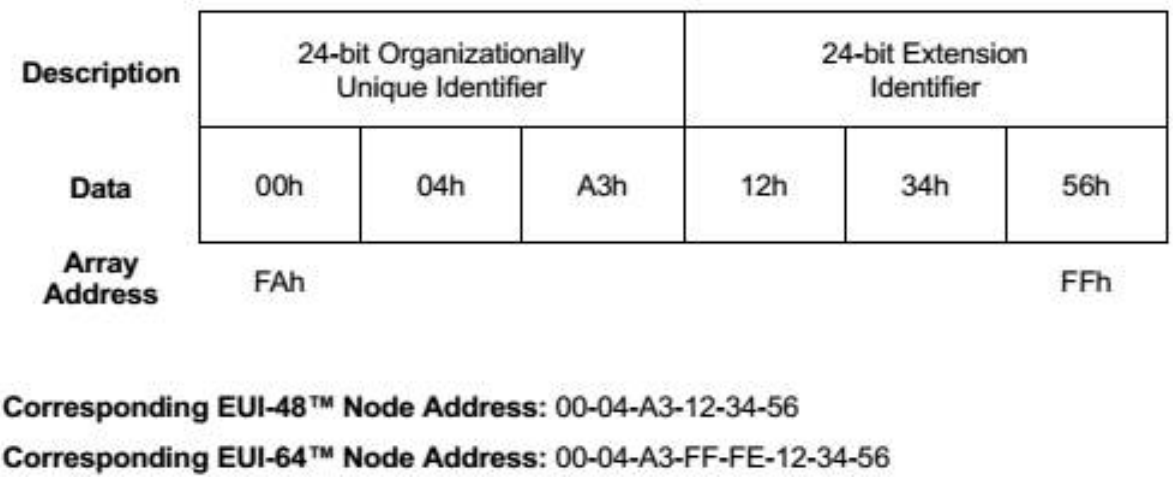


Figure 6: Mandatory Memory Location of MAC address stored in MAC EPROM

5.4 BlueRiver Authentication IC

The BlueRiver Authentication IC is the component that contains the key to unlock BlueRiver functionality. The communication between the FPGA and BlueRiver security chip is fully encrypted and is done over a 1-Wire interface.

The security devices purchased directly from Semtech AptoVision Products Group or from your BlueRiver representative. There are 4 distinct security chips available; two for the BlueRiver NT1000 and two for NT2000. The same chip applies

equally to both transmitter (TX) and receiver (RX) designs.

Table 12: BlueRiver Authentication IC part numbers

Part Number	Design	Description
AVBRNT1KCUTRX01-SD	NT1000	To use with NT1000 copper chipset (TX and RX)
AVBRNT1KFITRX01-SD	NT1000	To use with NT1000 fiber design (TX and RX). Can also be used for the NT1000 copper and NT2000 copper chipsets.
AVBRNT+CUTRX01-SD	NT2000	To use with NT2000 copper design (TX and RX). Can also be used in NT1000 fiber and copper chipsets.
AVBRNT+FITRX01-SD	NT2000	To use with NT2000 fiber design (TX and RX). Can also be used with NT2000 copper and NT1000 fiber or copper chipsets.

5.5 DDR3 Memory (NT2000 only)

External DDR3 memory is only applicable to BlueRiver NT2000 designs.

This memory is used by the BlueRiver AV processing engine, referred to as the BlueRiver AV Processor. This is found only in the BlueRiver NT2000, so therefore not applicable to BlueRiver NT1000 designs.

The DDR3 is used in conjunction with some advanced processing features, such as:

- Video frame buffer
- Video compositing
- Video de-interlacing
- Video frame converting
- Video Chroma resampling and converting

The required DDR3 Memory interface is two integrated circuits of 128Mx16 memory.

The Micron DDR3 Memory interfaces listed in the table below have been qualified by Semtech AptoVision Products Group.

Table 13: DDR3 Memory interfaces qualified by Semtech

Design	MT41K128M16JT-107	MT41J128M16JT-093:K	MT41K128M16JT-125:K
Taizi	x	x	
Duke		x	x

Note: The MT41K128M16JT is recommended for all new designs based on the AQLX107.

IMPORTANT! The DDR3 layout requires proper trace length matching. Semtech AptoVision Products Group requires customers to re-use the DDR3 layout from BlueRiver NT2000 reference design in their own NT2000 designs.

5.6 LED Control

NT1000 and NT2000 includes control of 6 LEDS indicating activity as illustrated in the table here below.

Table 14: LED indicators

LED name	Description
ov_led(1)	Video stable LED. • LED is on if the video signal running through the FPGA is stable. • Stability is established when at least two consecutive video frames have same horizontal and vertical active dimensions.

LED name	Description
ov_led(2)	FPGA Loaded LED. Indicates if FPGA firmware loaded correctly and whether a valid BlueRiver Authenticator detected. **LED Off:** FPGA is not loaded correctly. **LED Blinking:** FPGA loaded correctly but a valid BlueRiver Authenticator NOT detected. **LED ON** FPGA loaded correctly and a valid BlueRiver Authenticator detected.
ov_led(3)	10G TX LED. Indicates if Ethernet packets are being transmitted. **LED Off:** **No p**ackets being transmitted. **LED Blinking:** Packets are being transmitted.
ov_led(4)	10G RX LED. Indicates if Ethernet packets are being received. Also, indicates if FPGA SERDES detects valid signal. **LED Off:** No packets are being received and RX SERDES is NOT linked. **LED Blinking:** Packets are being received and RX SERDES is linked. **LED ON** No packets are being transmitted but RX SERDES is linked.
ov_led(5)	USB Link. Indicates if USB subsystem detected.
ov_led(6)	USB activity. Indicates USB data traffic present.

5.7 Restore Factory Default settings

For the BlueRiver transmitter and receiver devices, if pin is connected in the design pressing and holding `iv_sw(1)` during boot-up resets the device to factory default settings.

To restore factory default settings, perform the following steps:

1. Remove power from device.
2. Hold `iv_sw(1)` and plug power back into the unit.
3. The unit's LEDs will blink (except video), once they stop blinking release the `iv_sw(1)` button.
4. Unit will complete startup process, restoring the factory default settings.

5.8 RGMII 1000BASE-T Interface

The BlueRiver NT1000 and NT2000 devices both have an RGMII interface that is configured to work in 1GbE mode.

The RGMII interface is configured to continuously work in 1GbE (1000 Mbps) mode.

- This means it is configured to always work with 125 MHz clock using a 4-bit DDR bus to transfer data and that auto-negotiation is left to the 1G Switch IC that is connected to the RGMII interface.
- If a device connected to the 1G Switch IC would like to communicate at a lower speed (e.g. 10 or 100 Mbps), the external IC switch manages the speed negotiation and configures itself to desired bandwidth. These packets are then transferred at higher speed over the RGMII interface.

The primary use of this RGMII interface is to connect to a 1GbE switch IC, that is also connected to an external 1GbE Ethernet RJ-45 faceplate connector and possibly to external on-board microcontroller (MCU).

Doing this makes, it is possible to:

- Extend 1GbE data/corporate network over 10GbE network interface between all BlueRiver transmitter and receiver devices.
- Control all BlueRiver transmitter and receiver devices connected to 10GbE network by connecting the control

node (e.g. computer) running the control software to the 1GbE port of a BlueRiver device, thus saving a 10GbE network switch port.

- Connect an external microcontroller (MCU) to 1GbE switch IC, thus connecting the MCU to both the 1GbE Ethernet faceplate connector as well as the 10GbE network link. This is possible only if the 1G switch IC implemented has an unused MII interface.

5.9 RGMII Protocol

The RGMII interface was designed following the RGMII protocol.

Note: Information about the RGMII protocol can be found in the RGMIIv1_3.pdf. A copy of this document may be downloaded from the link provided below:

https://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/903/RGMIIv1_5F00_3.pdf

Should be noted however, that some of the features of this protocol are not supported, including but necessarily limited to the items outlined below:

1. Only 1Gb rate is supported. Transmit and receive always operate at 125 MHz.
2. The following in-band statuses are NOT supported:
    a. Link status
    b. Clock speed status
    c. Duplex status
    d. False Carrier indication
    e. Carrier extend
    f. Carrier Extend Error
    g. Carrier Sense
3. There is no dedicated MDIO interface available.

An assumption is made that the 1G switch interface is to be connected to a collision free domain. This assumption is true when the RGMII interface is either connected to an Ethernet Switch or directly to an endpoint such as a microcontroller (MCU). When in a collision free domain, carrier functionalities do not need to be supported.

Important! Ensure that the BlueRiver RGMII interface is always connected to a collision free domain.

In the BlueRiver NT2000 reference designs Semtech uses Realtek Ethernet switch IC.

- In Duke and Prince designs the Realtek RTL8305H-CG is used.
- In the Taizi design the Realtek RTL8365MB-CG is used.
- For both IC's, they manage all switching activities between their associated interfaces.

The Realtek RTL8305H-CG includes an RGMII interface, a 1GBASE-T interface and an unused MII interface. The latter interface can be used to connect an external microcontroller to network.

In the case of the RTL8365MB-CG, it includes an RGMII interface and a 1GBASE-T interface

Comment: An alternate switch IC that includes only a 1GBASET interface and a RGMII interface can be used instead of the Realtek RTL8305H IC. However, the switch IC will not be controlled by the BlueRiver chipset but instead will need to be controlled by an external microcontroller. For this reason, when using another switch IC several I/O's can potentially be omitted.

The following table lists all the PHY 1G interfaces and how each one should be connected when a different IC is selected.

Table 15: List of IO related to PHY 1G interface

PHY 1G pin	Description and notes
wb_phy_1g_sda **wb_phy_1g_scl**	I2C interface used to configure RTL8305H • should be pulled-up to 3.3V when different IC used
wb_phy_1g_gpio_0 **wb_phy_1g_gpio_2** **wb_phy_1g_gpio_3**	Reserved for RTL8305H • currently not used • should be pulled-up to 3.3V when different IC used
ov_phy_1g_rx_data	RGMII data source • should be connected to RGMII data sink from desired RGMII IC
ob_phy_1g_spdif	Reserved for RTL8305H • currently not used • should be left floating
ob_phy_1g_rx_ctl	RGMII ctl source • should be connected to RGMII ctl sink from desired RGMII IC
ob_phy_1g_rx_clk	RGMII clk source • should be connected to RGMII clk sink. Runs at 125 MHz
ob_phy_1g_rst_n	Used to reset the RTL8305H • should be left floating
ob_phy_1g_crs	Reserved for RTL8305H configured in RMII mode (RMII not supported) • should be left floating
ob_phy_1g_col	Reserved for RTL8305H configured in RMII mode (RMII not supported) • should be left floating
ob_phy_1g_clk	Reserved for RTL8305H • currently not used • should be left floating
iv_phy_1g_tx_data	RGMII data sink • should be connected to RGMII data source from desired RGMII IC
ib_phy_1g_tx_ctl	RGMII ctl sink • should be connect to RGMII ctl source from desired RGMII IC
ib_phy_1g_tx_clk	RGMII clk sink • should be connected to RGMII clk source • runs at 125 MHz

The following block diagram indicates the connections that should be used:

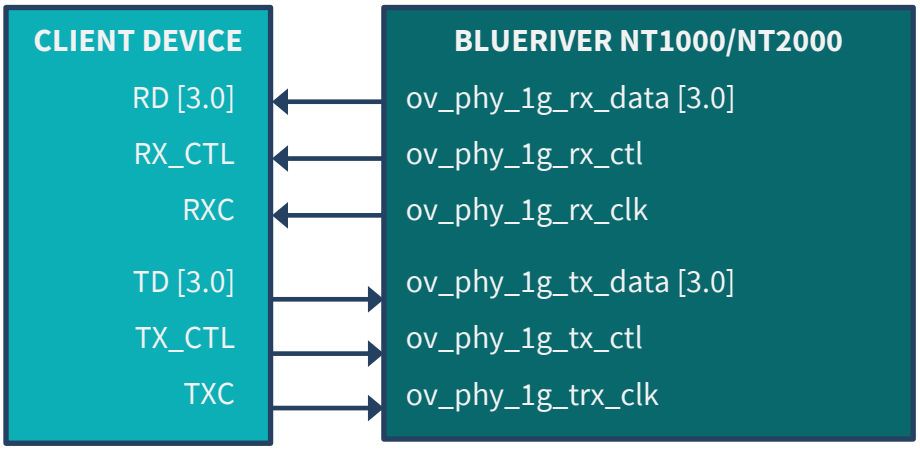


Figure 7 RGMII Connections to use for BlueRiver devices

Note: The figure shown below is for reference only. It shows the phase relationship between RGMII clock and data/control for both the FPGA's RGMII input and the FPGA's RGMII output.

Warning! It is the client's responsibility to ensure that the direction of the "Client Device" pins are consistent with the second example in figure below and if appropriate is adjusted to their meet needs.

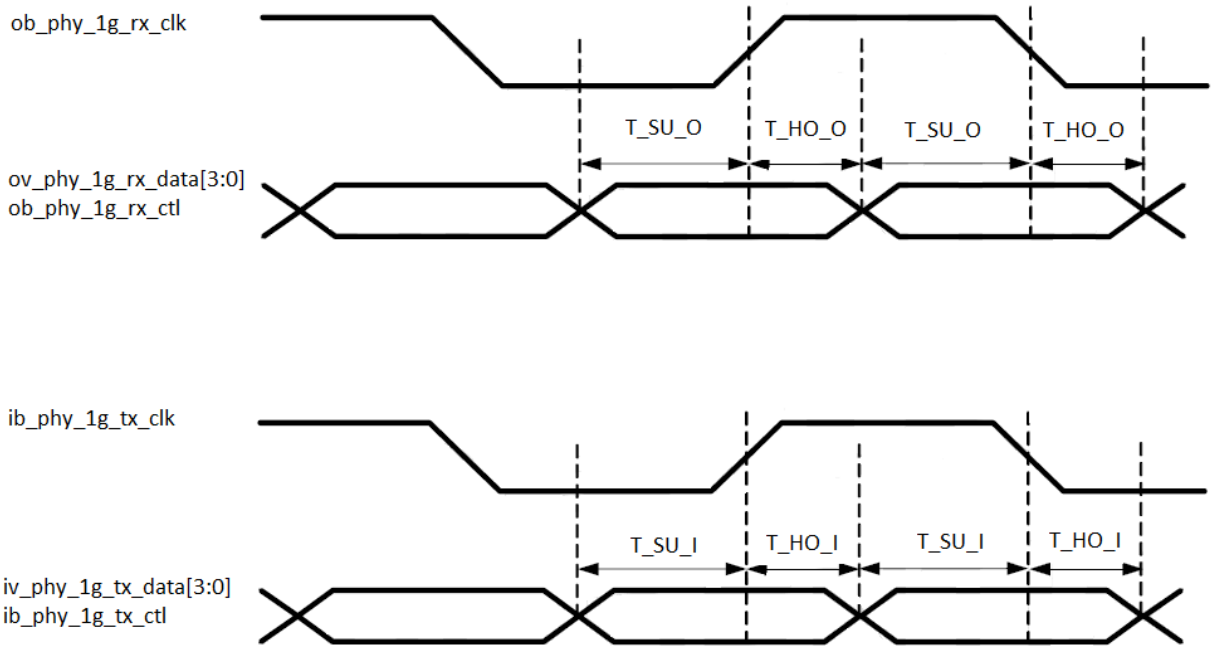


Figure 8 RGMII Relationship of clk, data and ctl for BlueRiver transmitter and receiver

The table provided below lists the interfaces related to the RGMII 1GbE Interface.

Table 16: List of IO related to RGMII 1GbE interface

Timing	Description	Value (min)
T_SU_O	FPGA Output Setup	1 ns
T_HO_O	FPGA Output Hold	1 ns
T_SU_I	FPGA Input Setup	-0.5 ns
T_HO_I	FPGA Input Hold	1 ns

5.10 Quad I2S Interface

Both, the BlueRiver NT1000 and NT2000 chipsets include synchronous multichannel I2S interfaces for extracting and injecting HDMI audio or to transport audio between BlueRiver devices.

- **I2S input** consists of quad (4x) synchronized slave inputs, each carrying 2 audio channels or up to 8-channels.
- **I2S output** consists of quad (4x) synchronized master output, each carrying 2 audio channels or 8-channels.

Note: When auxiliary audio capabilities are being considered, it is advised to implement the Quad I2S interface in all new designs.

The quad I2S inputs and outputs support the following:

- Left justified, MSB first
- 24bits
- Up to 192 kHz sampling rate
- Falling edge aligned data generation.
- Rising edge data sampling.

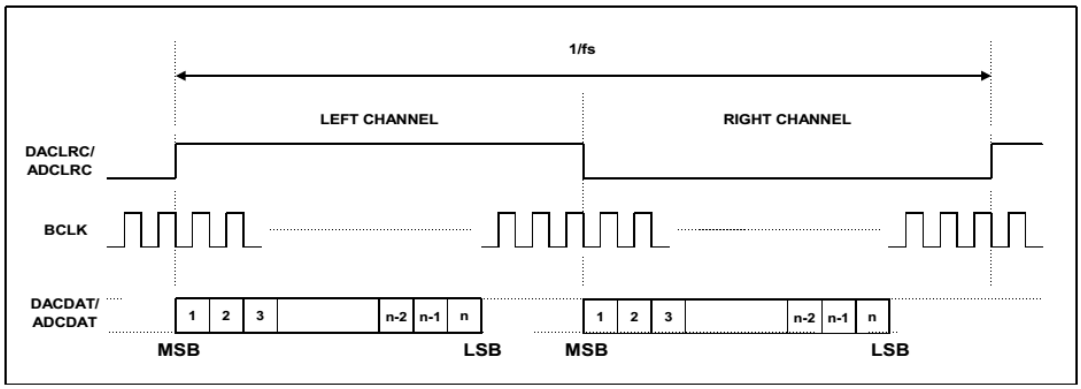


Figure 9 Quad I2S audio interface

5.11 Single I2S audio interface (master)

The purpose of this I2S Master Interface is to transport auxiliary 2-channel audio signals from BlueRiver transmitter devices to BlueRiver receiver devices.

On BlueRiver NT2000 transmitter devices it can also be used to locally extract 2-channel downmixed HDMI PCM audio.

Note: The Single I2S interface was the original audio interface for independent audio. It is now recommended for new designs requiring auxiliary audio to take use of the Quad I2S interface.

This I2S master interface is configured as follows:

- Left justified, MSB first
- LPCM
- 24bits
- 48 KHz
- Falling edge aligned data generation
- Rising edge data sampling

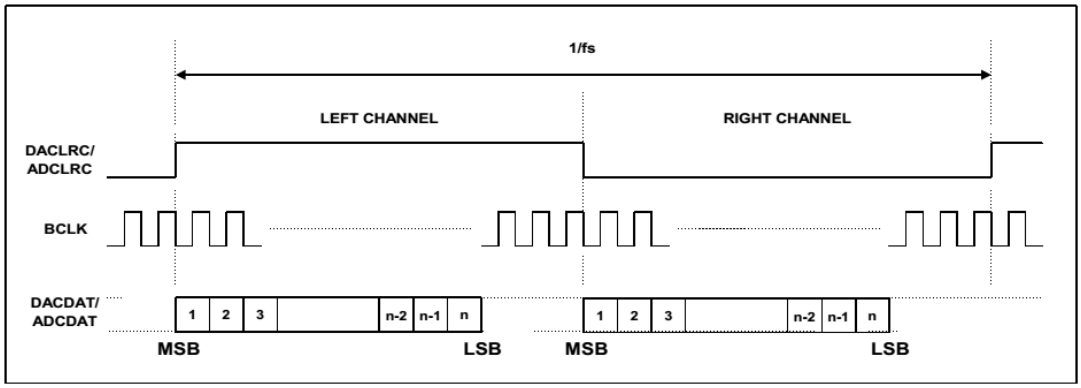


Figure 10 Single I2S audio interface (master)

Comment: In the BlueRiver NT2000 reference designs, this interface is used to implement auxiliary analog audio input or output by connecting an external **Wolfson WM8731SEDS Codec IC** that connects to the external 2-channel analog audio port.

- On the TX side, this interface can be configured as either an input or output.
- On the RX side, this interface is always an output.

5.12 RGMII USB 2.0 interface

This is the RGMII interface that is reserved for use with the Icron ExtremeUSB core to enable USB 2.0 extension functionality for USB devices, such as keyboard, mouse, USB drive and other USB devices.

There are two choices of Icron parts that can be used with the BlueRiver NT1000 and NT2000 chipsets:

- USB 2.0 RG2310A Core SO-DIMM module; or
- USB 2.0 ITC2053A-CB IC

The RGMII interface is configured to work in 1GbE mode, running at 125 MHz.

5.13 10GBASE-T Interface

The 10GBASE-T interface is mutually exclusive with the SFP+ interface (following section, 5.14 SFP+ Interface).

Comment: These interfaces are only exposed when using Kintex-7 160T devices with discrete 10GbE PHY. When using a AQLX107 device, this interface is integrated inside the package.

Hardware can be designed with both a 10GBASE-T and a SFP+ interface but only one of the interfaces can be active at the same time. Also, the depopulation option is required in production to produce either a copper (10GBASE-T) or fiber (SFP+) product.

The interfaces used between the BlueRiver NT1000/NT2000 chipset and the 10GBASE-T PHY are XFI and MDIO.

Note: The XFI connects to the FPGA SERDES interface.

It is the BlueRiver FPGA that is responsible for configuring the 10GBASE-T PHY:

- This is done over the MDIO interface.
- In addition to transferring firmware to the PHY, the MDIO interface is used to check the status of the PHY.

Reminder! The following items are only applicable when using the discreet Kintex-7 160T FPGA. They do not apply to the AQLX107.

The XFI interface has some important characteristics to keep in mind:

- It is a high-speed interface running at 10.3125 Gbps. Each BlueRiver transmitter (TX) and receiver (RX) interface shall be routed differentially keeping a differential impedance of 100 Ohms.
- Special care needs to be taken when routing this interface. No VIA should be used while routing these lines.

It is the PHY that converts the XFI interface to 10GBASE-T interface. When using Kintex-7 160T, BlueRiver supports the Broadcom BCM84851 PHY.

Note.: Because these are very high-speed interfaces, Semtech AptoVision Products Group recommends designers to reuse design layouts from the BlueRiver NT2000 reference design.

5.14 SFP+ Interface

As mentioned in previous section, it's important to note that the SFP+ interface is mutually exclusive with the 10GBASE-T interface (previous section, 5.13 10GBASE-T Interface).

Hardware can be designed with both interfaces but only one can be active at the same time. Also, the depopulation option should be used in production to produce either a copper (10GBASE-T) or fiber (SFP+) product.

The interfaces used between BlueRiver NT2000/NT1000 and SFP+ is XFI.

Note: The XFI connects to the FPGA SERDES interface.

The XFI interface has some important characteristics:

- This is a high-speed interface running at 10.3125 Gbps. Each of TX and RX interface shall be routed differentially keeping a differential impedance of 100 Ohms.
- Special care shall be taken while routing this interface. No VIA should be used while routing those lines.

Note: Because these are very high-speed interfaces, Semtech AptoVision Products Group recommends designers to reuse design layouts from the BlueRiver reference design(s).

5.15 SI5341B

All BlueRiver NT2000/NT2000 **receiver** (RX) devices require the Silicon Labs Sl5341B clock generation IC on board.

Note: Clock generation IC is not required for BlueRiver transmitter (TX) devices.

Important: This IC is important and a replacement IC cannot be used. It is used by BlueRiver receiver devices to regenerate the TMDS clock.

TIPS:

i. Pay special attention to both power delivery and signal routing, especially for the routing of clock pairs TMDS_CLK_RAW and REC_CLK.
ii. These sensitive clocks are used as differential clock signal to drive SERDES reference clock of the FPGA and HDMI transceiver.
iii. Refer to the BlueRiver receiver (RX) design for details on the clock buffer circuit and PCB layout.
iv. Refer to the Silicon Labs Si5341B datasheet for more information about the SI5341B IC.

Note: When ordering this IC, use the part number Si5341B-B05239-GM number to guarantee availability, price and

support from Silicon Labs.

5.16 156.25 MHz XTAL

All BlueRiver NT1000/NT1000 devices, transmitters and receivers, require 156.25 crystal. The crystal provides a reference clock to the high-speed SERDES.

Important: The crystal used must be a 3rd overtone device. Semtech AptoVision Products Group has qualified and recommends the TXC Crystals and Oscillators, BF-156.250MBE-T for BlueRiver NT1000/NT2000 chipsets.

5.17 HDMI Transceiver

The HDMI Transceiver Interface uses the FPGA SERDES to connect the FPGA to the HDMI signal.

It is composed of three different TMDS lines that each run at a maximum speed of 6 Gbps and a TMDS clock that runs at a maximum speed of 340 MHz.

Each TMDS line shall be routed differentially keeping a differential impedance of 100 Ohms.

Comment: The TMDS clock is normally equivalent to the TMDS serial clock divided by ten (HDMI 1.4); however, it is divided by forty when the TMDS serial clock is higher than 3.4 GHz (HDMI 2.0).

Each BlueRiver endpoint has an HDMI transceiver chip between the HDMI connector and the BlueRiver NT1000/NT2000 HDMI interface. It is configured as an input on transmitter (TX) devices and as an output on receiver (RX) devices.

The HDMI chip has 2 tasks:

1. Convert the 3.3V DC coupled TMDS interface to AC coupled interface supported by the BlueRiver NT1000/NT2000 chipsets.
2. Contains a valid HDCP key.

Note: Semtech AptoVision Products Group use the Silicon Image SiI9777 HDMI transceiver in all reference designs.

5.18 GPIO & 7-Segment Display

Both the BlueRiver NT1000/NT2000 include a set of 12 pins for general purpose I/O.

5.18.1 7-Segment Display

These GPIO pins can drive a three-character 7-segment display:

- For the 7-segment, GPIO used are [10:8] and [6:0].
- Only one character is displayed and the three characters are multiplexed.

If implemented the 7-segment display provides the following:

1. Displays the last octet of the multicast IP address (channel) used for the primary video stream.
   a. BlueRiver transmitter devices show the channel on which it transmits the video.
   b. BlueRiver receiver device shows the last three octets of the IP of the channel on which it receives video.
   Warning: This feature is useful for debugging purposes only. If using extended Multicast IP range keep in mind the first part of the IP address is not visible.
   c. This makes it possible to identify which two devices are connected just by looking at the 7-segment display.
   d. The code “P2P” indicates that the device is connected directly to another device without passing through an Ethernet switch, a Point-to-Point configuration.

2. Displays the booting sequence:
   a. FAST turning circle -- indicates that BlueRiver firmware is loading.
   b. SLOW turning circle -- indicates that 10GBASE-T PHY firmware is loading.
3. Displays error codes.

5.18.1.1.1 Error codes

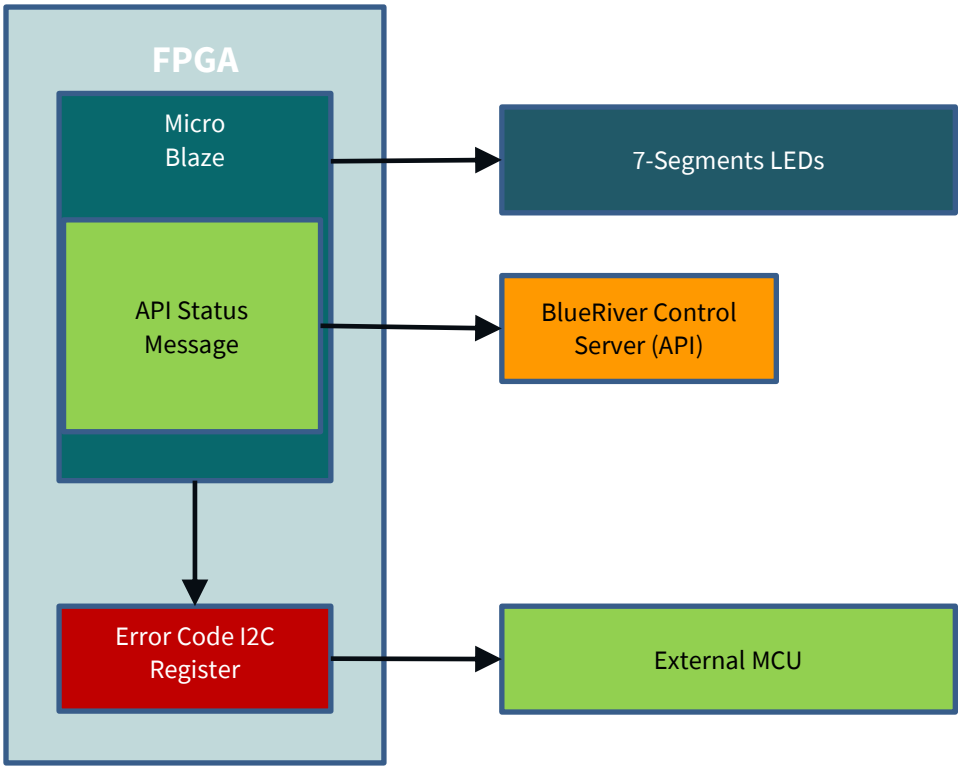
Possible error codes are listed in the table below:

Table 17: Error codes possible on 7-segment display

Code Number	Description
E00	BlueRiver device is being reset back to factory settings.
E01	Device is running from golden firmware image.
E02	Error occurred in subroutine.
E03	Error occurred in subroutine.
E04	Error writing into SPI flash memory.
E05	Error occurred in dynamic memory allocation.
E06	Error occurred in pbuf data.
E10	Pericom IC failed to initialize. (legacy error).
E11	Communication error with Pericom IC. (legacy error).
E12	ICRON USB chip did not initialize correctly.
E20	HDMI IC did not initialize correctly.
E21- E24	Read error occurred. Not able to communicate with HDMI IC (read).
E25-E28	Write error occurred. Not able to communicate with HDMI IC (write).
E29	Not able to Flash HDMI IC.
E30	10G PHY IC did not initialize correctly.
E31-E34	Errors occurred when accessing the 10G PHY.
E35	10G PHY IC not detected.
E36	10G PHY IC not running.
E40	EDID's checksum doesn't match the calculated checksum.
E50	Not possible to initialize MAC IC.
E51	MAC is busy.
E52	Not able to communicate with MAC IC (write).
E53	Not able to communicate with MAC IC (read).
E60	SFP+ did not initialize correctly.
E61	Not able to communicate with SFP+.
E62	Not able to communicate with Realtek RTL8305.
E70	Error Initializing the default settings.
E71	Error initializing RS-232.
E72	Error initializing HDMI 2.0
E80-E81	Error reading EDID.
E82-E83	Error writing EDID.
E84	Silicon Labs SI5341B clock generator out of range.
E85	Silicon Labs SI5341B clock generator not detected.
E90	Error occurred in subroutine.
E91	Error occurred in subroutine.
E96	Error with matrix, too many transitions.

Although it is possible to retrieve BlueRiver error codes from the LED display of the 7-Segment, when in production this is not typically possible as many designs do not include the 7-Segment LED display. The ability to retrieve error codes

through the BlueRiver Control server or thru external MCU I2C register is therefore possible. Figure below shows the path of the BlueRiver errors listed in the table above.



RED = FPGA section
GREEN = Firmware section
ORANGE = API/GUI section

Figure 11: BlueRiver error codes

5.18.2 GPIO pins

The GPIO pins are available for custom use.

- By default, all GPIO are tristate (set as inputs).
- If the 7-Segment hardware bit is present in the board definition (managed through the BlueRiver Production Assistant), then the GPIO pins [10:8] and [6:0] are no longer GPIO but instead are connected to the 7-segment controller.

Note: GPIO changes (from the BlueRiver Control Server (API) requests) are volatile, after power up they return to tristate (inputs) and 7-segment (if applicable).

As example for potential use of GPIO's, the BlueRiver hardware reference designs illustrate how these pins can be used to connect with an external microcontroller:

- GPIO [7] is connected to the external microcontroller reset pin.
- GPIO [11] is connected to the external microcontroller BOOT0.
- For updating of the external microprocessor firmware, these two pins are controlled by the BlueRiver Control Server (API).

5.19 Infrared

BlueRiver NT2000 series includes Infrared (IR) I/O operating at 3.3 volts.

- In the BlueRiver NT2000 reference designs, the NT2000 output connects to an output circuitry that amplifies the 3.3V signal to 5V.
- Similarly, the 3.3V NT2000 input is connected to a clamping circuit to drop 12V input voltage down to 3.3V.

5.20 RS-232

Both the BlueRiver NT1000 and NT2000 chipsets support 4 x UART interfaces:

- Typically, one of these is normally used to implement the RS-232 faceplate interface.
- The additional UART interfaces are available to for example, add another RS-232 interface to the external faceplate or communicate with other onboard systems such as external microcontroller.
- All 4 UART ports support baud rates ranging from 2 400 bauds up to 115 200 bauds.

Comment: Although the BlueRiver chipset supports baud rates up to 115 200, it is important to note that only a baud rate up to 19 200 is sustained over a long period of uninterrupted traffic. This means that short bursts of data are successfully sent/received but if continuous data is sent above 19 200 without breaks, some data will be lost. This limitation applies only to RS-232 data sent between BlueRiver devices.

5.21 External Microcontroller

External microcontroller unit (MCU) is used to control external subsystem components to the core functionality of the BlueRiver chipset. This includes:

- HDMI transceiver
- 1GbE Ethernet
- Custom subsystems. These could include, audio processing subsystems or additional types of video interfaces besides HDMI such as DisplayPort, VGA, or SDI.

Subsystems that are controlled exclusively by the BlueRiver NT1000 and NT2000 chipsets are:

- Silicon Labs SI5341B clock generator (BlueRiver receiver devices only)
- 10G PHY
- Icron Extreme USB 2.0 core

Comment: In all current BlueRiver hardware designs an external microprocessor is used, important to note that this is the recommended solution.

BlueRiver can provide a remote connection to the external microcontroller:

1. Connect BlueRiver chipset UART to the external microcontroller. Control and communicate with the microcontroller using RS-232 commands and data through the BlueRiver API. Refer to Figure 12: Connecting external MCU to RS-232.
2. Connect the external microcontroller to the internal 1GbE Switch that is also connected to the BlueRiver RGMII. This allows for the microcontroller to be remotely controlled (from software) using Ethernet packets and custom protocol. Refer to Figure 13: Connecting external MCU to 1GbE Ethernet.

In both cases, the microcontroller should also be connected to the BlueRiver NT2000/NT1000 I2C slave interface port to access local parameters and status registers.

Important! When using an external microcontroller to control the HDMI transceiver, connecting to the NT1000/NT2000 I2C slave interface is mandatory for HDCP support.

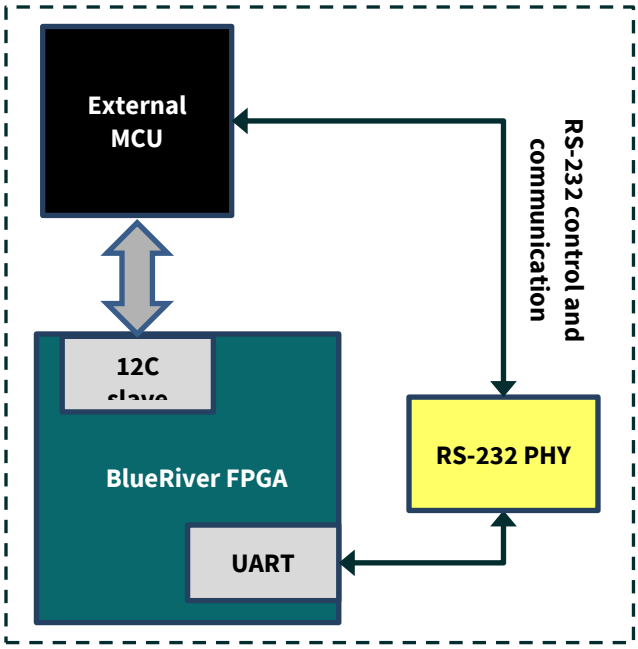


Figure 12: Connecting external MCU to RS-232

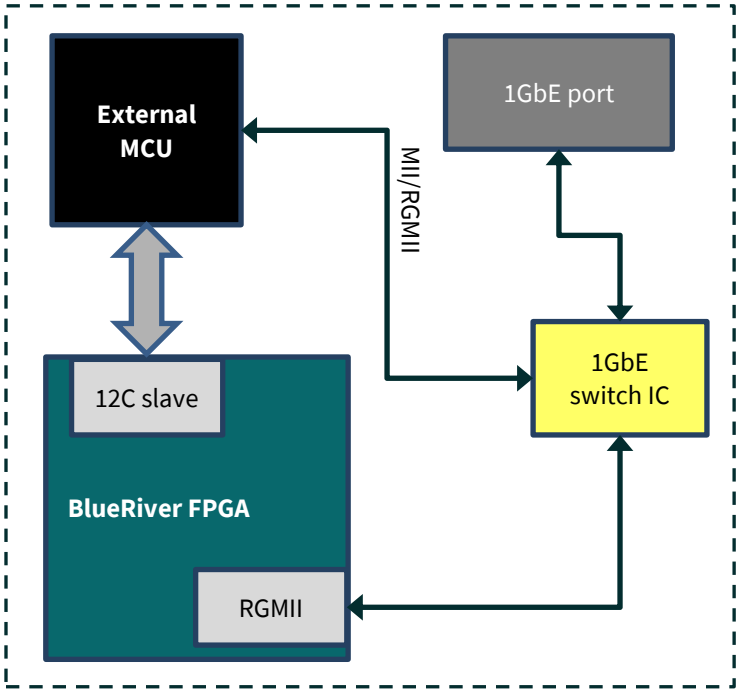


Figure 13: Connecting external MCU to 1GbE Ethernet

6 Power Delivery

6.1 1.0V supply (P1V0) – (P1V0_A1)

The 1.0v supply (P1V0) is a very important supply, as well challenging to design.

P1V0 rail supplies the CORE of the BlueRiver NT1000 and NT2000 logic (FPGA section of AQLX107 or Kintex-7 160T FPGA).

This 1V rail needs to be delivered through a full power plane and the maximum drop under full load should be less than 50 mV.

6.1.1 Purpose

The main purpose of the 1V is to supply the BlueRiver NT1000/NT2000 chipset logic (FPGA section of the AQLX107 or Kintex-7 160T FPGA).

It is separated in two sections:

1. MGTAVCC
2. VCCINT

MGTAVCC supplies the section related to the FPGA's SERDES; this includes the 10GbE link and HDMI interface.

VCCINT is used to supply the core logic of the FPGA.

6.1.2 Specifications

Refer to the Xilinx 7 Series FPGAs GTX/GTH Transceivers User Guide UG476 for more information about the MGTAVCC.

Refer to the Xilinx 7 Series FPGAs PCB Design Guide UG483 for more information about the VCCINT.

Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for details regarding the power characteristics.

6.1.3 Recommendation for 1.0V

1. Selected DC/DC should have a minimum efficiency of at least 90% for the total current required to drive FPGA and other subsystem IC's that also make use of the P1V0 power rail.
2. MGTAVCC is the analog for the internal analog circuit of the FPGA's SERDES.
    a. This includes the analog circuits for the PLLs, transmitters and receivers.
    b. It is critical that this supply be well filtered.
    c. Xilinx recommends that the noise at MGTAVCC pins be less than 10 mV over the band from 10 kHz to 80 Mhz. For this reason, multiple capacitor values are used in the decoupling.
3. VCCINT is the digital supply to internal Kintex-7 160T and AQLX107 FPGA gate logic.
    a. High frequency decoupling capacitors are included in these packages.

Recommendation: Semtech AptoVision Product Group suggests 1.03V instead of 1.0V on FPGA core supply.

Note: If SiI9777 HDMI transceiver is used, this rail is also used to supply CORE voltage to SiI9777 and similar decoupling approach should be used.

- Silicon Image suggests 1.05V for their core supply.
- Semtech AptoVision Products Group suggests 1.03V for core supply to both the FPGA and SiI9777.

6.2 0.85V supply (P0V85)

The 0.85V supply (P0V85) power rail is used by the Aquantia AQLX107.

6.2.1 Purpose

Purpose of this rail is to supply the core (digital) voltage for the Aquantia's 10GBASE-T PHY IC inside of the Aquantia AQLX107 package.

6.2.2 Specifications

Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more detailed information regarding the power characteristics.

6.2.3 Recommendations for 0.85V

1. Selected DC/DC should have a minimum efficiency of at least 90%.
2. Special care should be taken on VDD_SRDS since this is supplying high frequency analog section of the chip.

6.3 1.2V supply (P1V2))

The 1.2V power rail is used by both the Aquantia AQLX107 and Kintex-7 160T.

6.3.1 Purpose

The 1.2 V is the second most important voltage on the board (next to the 1.0V) in the sense that it is used to supply multiple high frequency analog sections related to the high speed SERDES.

6.3.2 Specifications

Refer to the Xilinx 7 Series FPGAs GTX/GTH Transceivers User Guide UG476 for more information about MGTAVTT.

Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more detailed information about the power characteristics.

6.3.3 Recommendations for 1.2V

1. Selected DC/DC should have a minimum efficiency of at least 90%.
2. Special care should be taken when routing the voltage feedback. It should be routed in such a way as to minimize the noise.
3. Special care shall also be taken when routing P1V2_A2.
    a. This power nets shall be distributed using a solid power plane.
    b. Also, the resulting planes should be placed on a layer that is immediately over a ground plane layer.
    c. Finally, no signal should be routed over the P1V2_A2 on the plane immediately adjacent to the power plane.
    d. If this is not possible, a layer that contains a ground plane should be used in-between the power plane and the routing plane.
4. MGTAVTT is the supply of the internal analog termination circuit of the FPGA's SERDES.
    a. It is critical that this supply is well filtered.
    b. Xilinx recommends that the noise at MGTAVTT pins shall be less than 10 mV over the band from 10 kHz to 80 Mhz.
    c. For this reason, multiple capacitor values are used in the decoupling.

6.4 1.5V supply (P1V5) / 1.35 supply (P1V5)

This power rail supplies the DDR3 memory.

DDR3 memory is only used by BlueRiver NT2000 chipset for the built-in BlueRiver AV Processing Engine.

The NT1000 does not include this engine, so does not require DDR3 memory.

6.4.1 Purpose

The purpose of 1.5V power rail, is to supply the DDR3 memory and the AQLX107/Kintex-7 160T banks that are connected to this memory.

- In the BlueRiver NT2000 reference designs, the higher speed DDR3 memory running at 1.5V is used.
- Exception is that in the Duke NT2000 reference design the DDR memory uses 1.35V.

6.4.2 Specifications

Refer to Xilinx 7 Series FPGAs PCB Design Guide UG483 for further information about VCCO.

Refer to Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more detailed information about the power characteristics.

Refer to MT41K128M16JT-125:K (1.35V) and MT41J128M16JT-093:K (1.5V) specifications from Micron for more information about the VDD and VDDQ.

6.4.3 Recommendations for 1.35/1.5V

1. Selected DC/DC should have a minimum efficiency of at least 90%.
2. Kintex-7 160T and AQLX107 devices include high frequency decoupling capacitors in the package.

6.5 1.8V supply (P1V8)

6.5.1 Purpose

The purpose of the 1.8 V power rail is general.

P1V8 power rails are used to:

- Supply the oscillator needed to generate the TMDS clock.
- Supply both MGTVCCAUX and VCCAUX on the Kintex-7 160T and AQLX107.

Note: Some HDMI transceivers make use of this voltage level.

6.5.2 Specifications

Refer to the Xilinx 7 Series FPGAs PCB Design Guide UG483 for more information about VCCAUX.

Refer to the Xilinx 7 Series FPGAs GTX/GTH Transceivers User Guide UG476 for more information about MGTVCCAUX.

Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more detailed information about the power characteristics.

Refer to the Silicon Labs Si5341B datasheet for more information about VDDOA and VDDOB.

6.5.3 Recommendation for 1.8V

1. Selected DC/DC should have a minimum efficiency of at least 90%.
2. Kintex-7 and AQLX107 include high frequency decoupling capacitors within the package.
3. MGTVCCAUX supply the internal QPLL circuit of the FPGA's SERDES.
   - It is critical that this supply is well filtered.
   - Xilinx recommends that the noise at MGTVCCAUX pins shall be less than 10 mV over the band from 10 kHz to 80 Mhz.
   - For this reason, multiple capacitor values are used in the decoupling.

6.6 2.1V supply (P2V1)

The P2V1 power rail is used with Aquantia AQLX107.

Warning! When using Aquantia AQLX107, the P2V1 power rail is the most susceptible power rail for noise. Be sure to avoid any deterministic noise coupling from possible aggressors.

6.6.1 Purpose

The 2.1V power rail is an important power rail on the board and needs to be very clean. It supplies power to multiple high frequency analog sections related to 10G PHY.

6.6.2 Specification

Refer to the Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more detailed information about the power characteristics.

6.6.3 Recommendation for 2.1V

1. Selected DC/DC should have an efficiency of at least 90%.
2. Special care shall be taken when routing P2V1.
   - This power net shall be distributed using a solid power plane.
   - The resulting plane should be placed on a layer that's immediately over a ground plane layer.
   - Finally, no signal should be routed over the P2V1 on the plane immediately adjacent to the power plane.
   - If this not possible, a layer that contains a ground plane should be used in-between the power plane and the interfering routing plane.

6.7 3.3V supply (P3V3)

6.7.1 Purpose

The purpose of 3.3 V is general.

In the case of the SI5351B, it serves as a clock output supply.

Note: The section related to the SI5351B is only necessary on the BlueRiver receiver (RX) board. It is not required on the BlueRiver transmitter (TX) board.

The P3.3 is used to:

- Supply the oscillator needed to generate the 10GbE SERDES clock.
- Supply multiple IO banks on the FPGA.

This power rail is used by many other subsystems, must be designed accordingly.

6.7.2 Specification

Refer to the Xilinx 7 Series FPGAs PCB Design Guide UG483 for more information about VCCO.

Refer to Aquantia AQLX107 AQcite FPGA Programmable Multi-Gigabit BASE-T PHY datasheet for more information about the power characteristics.

6.7.3 Recommendation for 3.3V

1. Selected DC/DC should have a minimum efficiency of at least 90%.
2. Kintex-7 and AQLX107 devices include high frequency decoupling capacitor in the package.

7 PCB recommendations

In this section, general but important PCB design recommendations are outlined based on Semtech AptoVision Products Group's experience with our own BlueRiver reference designs.

Important: Hardware designers need to not only be aware of these recommendations but also to any manufacturer recommendations for the various subsystems used in the BlueRiver NT1000/NT2000 designs.

7.1 PCB Physical Characteristics

Here are some recommendations about the PCB itself:

1. Heat dissipation is important.
   - Fully populated BlueRiver NT2000 reference design includes a PCB that is approximately 120mm x 170mm (4.72 inches x 6.69 inches). Smaller footprint is not recommended.
   - For Taizi refer to the BlueRiver hardware reference design for more details.
   - A smaller footprint would require a large amount of effort on developing an efficient active heat dissipation design.
2. Recommend 1.5 oz. per square foot of copper (457.73 grams per square meter) clad thickness for power and ground planes.

7.2 Power Distribution

It is important to minimize resistance in the power distribution paths.

This is especially true for power delivery for the more demanding parts of the designs, such as the SERDES, FPGA, 10G copper PHY and the HDMI transceiver.

- Whenever possible use a solid copper plane.
- Use as much VIA as possible when doing the transition from power plane to TOP or BOTTOM plane. Six to nine VIAs is not too many.
- To minimize the voltage drop, use Low DC resistance ferrite bead.
- NO thermal relief on VIAs and BGA pads should be present.

7.3 Routing and Layout

7.3.1 Aquantia AQLX107 (10G Copper PHY)

For all new BlueRiver NT1000/NT2000 designs, Semtech AptoVision Products Group strongly recommends using the Aquantia AQLX107 for 10G copper PHY.

Only if customers have an existing BlueRiver NT design, should they consider using Broadcom BCM84851 instead.

Also, it is recommended to copy the routing and layout of the AQLX107 from the appropriate BlueRiver NT1000 /NT2000 reference design. If this is not a viable option, then follow the recommendations below:

1. The 50 MHz oscillator used to clock the AQLX107 should be routed differentially and the lines need to be well balanced (equal length and constant distance).
2. The 50 MHz oscillator should be placed as close to the AQLX107 as possible.
3. Bandgap resistor (AQLX107 PIN D21) should be placed as close to the AQLX107 as possible. In addition, the trace used to connect it shall be as wide as possible.
4. Refer to the power recommendations described elsewhere in this document. The outlined recommendations should be applied to ensure that best results possible are achieved.
5. Nothing should be routed either under or near the 10GBASE-T RJ45 connector. Also, a ground cut-out should be added.
6. Differential lines between the AQLX107 and 10GBASE-T RJ45 connector should be routed differentially and the lines should be well balanced, (equal length and constant distance).
7. No VIA should be used on the differential lines between the AQLX107 and the 10GBASE-T connector RJ45.
8. Ground should be used to separate differential lines between the AQLX107 and the 10GBASE-T RJ45 connector.

7.3.2 Silicon Image SiI9777 (HDMI transceiver)

BlueRiver reference designs use the Silicon Image SiI9777.

- If SiI9777 is used in a new BlueRiver NT1000/NT2000 design, recommended to copy the routing and layout of the SiI9777 section from the appropriate BlueRiver reference design.
- To minimize capacitive discontinuity, serial components on TMDS lines, like decoupling capacitor on HDMI differential lines between SiI9777 and AQLX107K7-B0000-S-C or Kintex-7 160T, recommended to include a cutout of the same pad size underneath the associated ground plane return path.

7.3.3 DDR3 Memory Interface (NT2000 only)

Semtech AptoVision Products Group makes it mandatory to reuse the DDR3 layout and routing used in the BlueRiver NT2000 reference designs. Customers are strongly advised to use the DDR3 block "**as is**".

7.3.4 All differential clock lines

Reference clocks from crystals and output clocks to/from clock IC's should be routed differentially and free of potential noise aggressors.

7.4 Other recommendations

1. Be sure the P2V1 plane is perfectly clean.
    - Away from MagJack RJ45, GND plane above and GND plane below.

- Nearby ceramic decoupling capacitors need to connect directly on this plane.

2. Ensure High speed serial lanes are routed on top layer without VIA's.
    - The intra-pair skew of these pairs must be reduced to less than 5 mils.
    - Also, the skew compensation need to be close to the mismatching (like shown below).

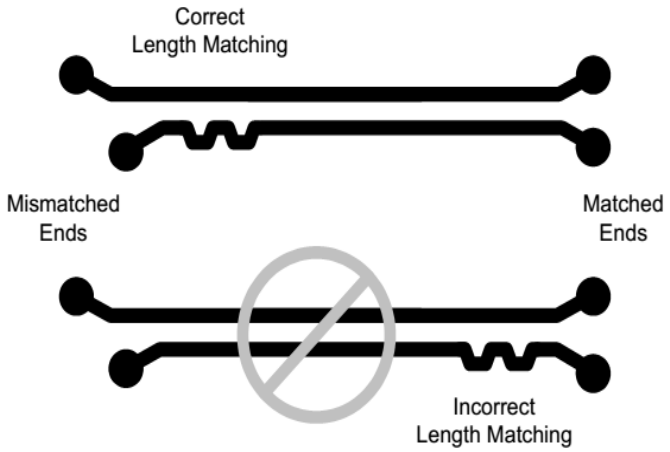


Figure 14: Correct and Incorrect Length Matching

1. Ensure there are no traces in the MagJack (RJ45 10GbE) area.
2. Even if you do not choose to install the LED 7-segments for mass-production, recommended to install it for prototyping as it can be valuable tool during debugging.
3. Ensure that the DDR traces are routed as they are shown in the BlueRiver NT2000 layout. It is required to reuse the entire BlueRiver DDR layout section.
4. Confirm that you are using a 156.25 MHz crystal that is a 3rd overtone.
5. Confirm that the RJ45 with built-in magnetics that is being implemented is approved for use in the 10GBASE-T standard.

Contact Information

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