CSC258 – Memory and datapaths

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上周review

- ALU
- Shifter, Rotator
- Booth Algorithm

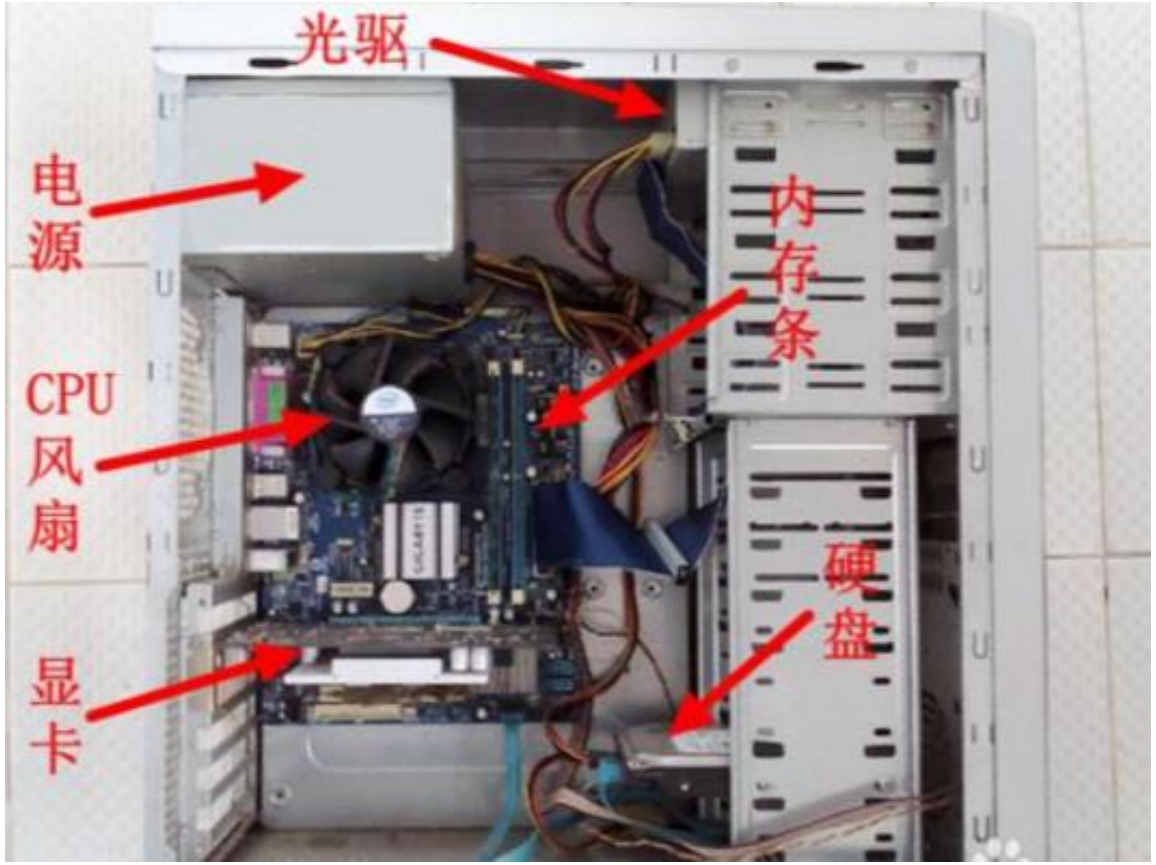
Storage (*)

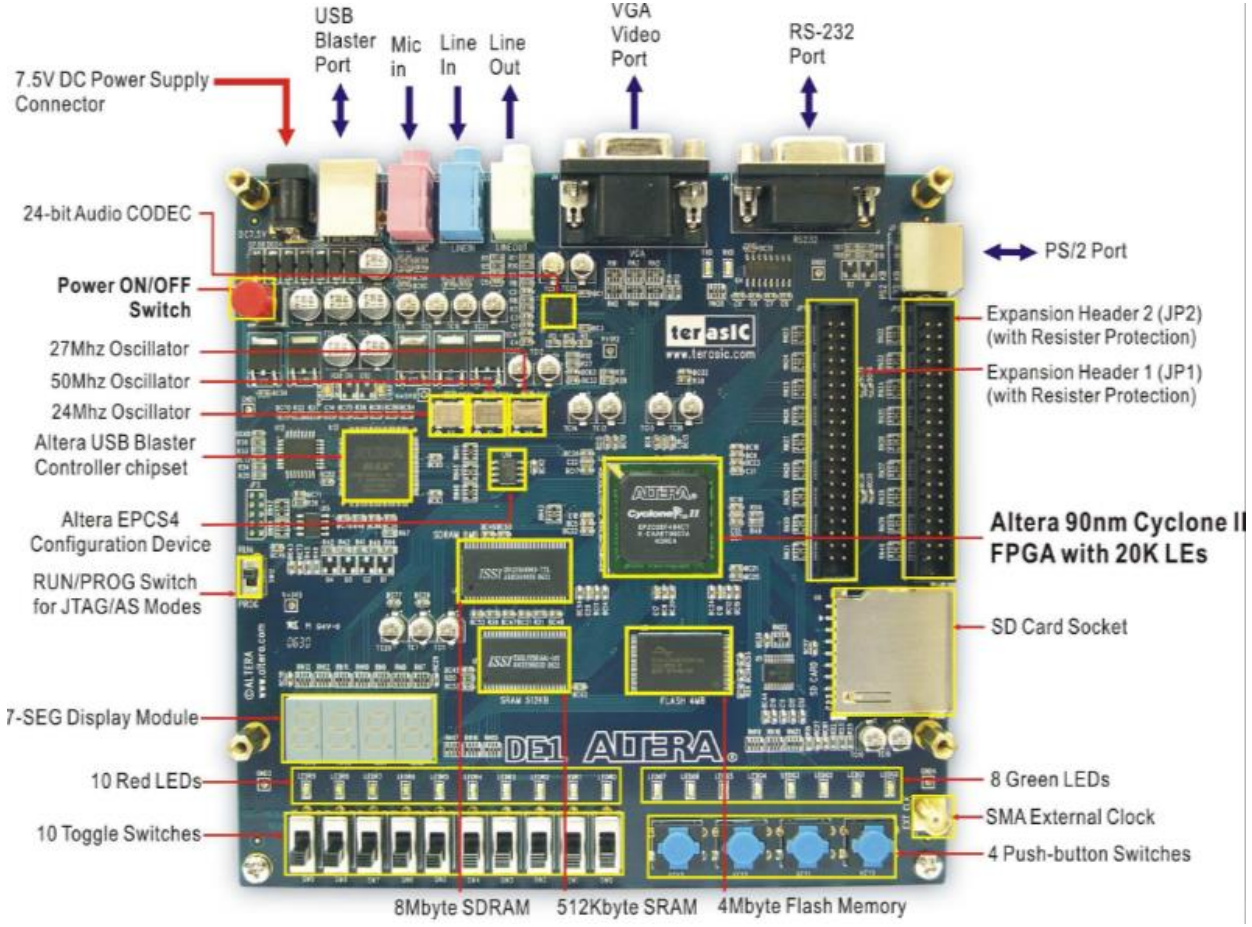
- In terms of access speed:
  - Register = The plate in front of you (We have learned shift register and load register)
  - Cache = The fridge in the kitchen
  - Memory (RAM) = The corner grocery store 内存
  - Hard Disk = The farm in the prairies
  - Network = The farm in another country

- In terms of how they store bits in the bit cell.:

1. *random access memory* (*RAM*)
   ① *volatile*, meaning that it loses its data when the power is turned off

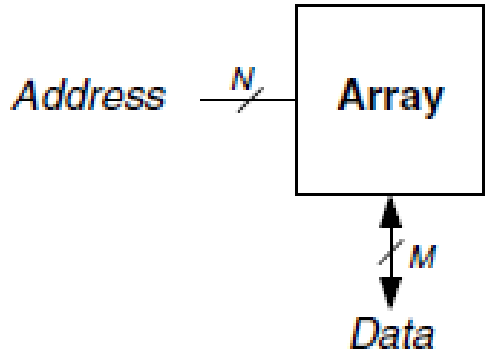
2. *Read only memory* (*ROM*)
   ① *ROM is nonvolatile*, meaning that it retains its data indefinitely, even without a power source.



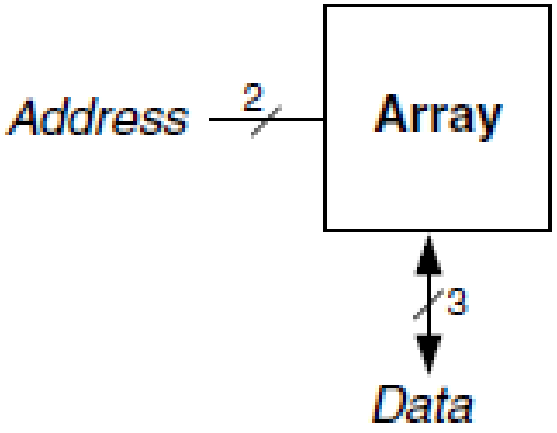


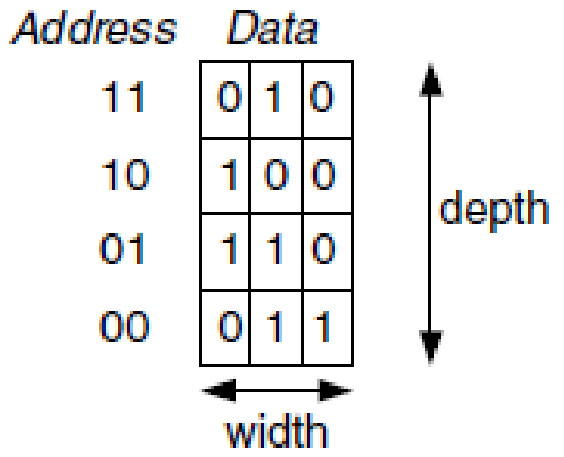
思考题：从电路的角度来看速度，解释为什么会有速度的差别？

MEMORY ARRAYS (basic ideas)



- To store information, we need
  - The value of the information : **Data;**
  - To tell where do we put the data: **Address.**
  - **思考：该用什么器件处理N bit address to data?**
- Reflect to dictionary concept in Python
  - An array with **N-bit addresses** and ***M*-bit data** has ***2^N rows*** and ***M columns***. Each row of data is called a *word.* Thus, the array contains ***2^N 个 M-bit*** words.





考点

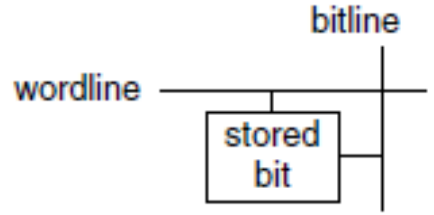
- 长方形求面积、求长、求宽
- 3缺1
- （2012Fall - 1）How many instructions could fit into a 256 byte memory unit, given a 32-bit architecture? **(2 marks)**
- **A. 256　　B. 64　　C. 32　　D. 8**

Example

- (2012F - 2) How many address bits are needed to specify each byte in a 512 byte memory unit?

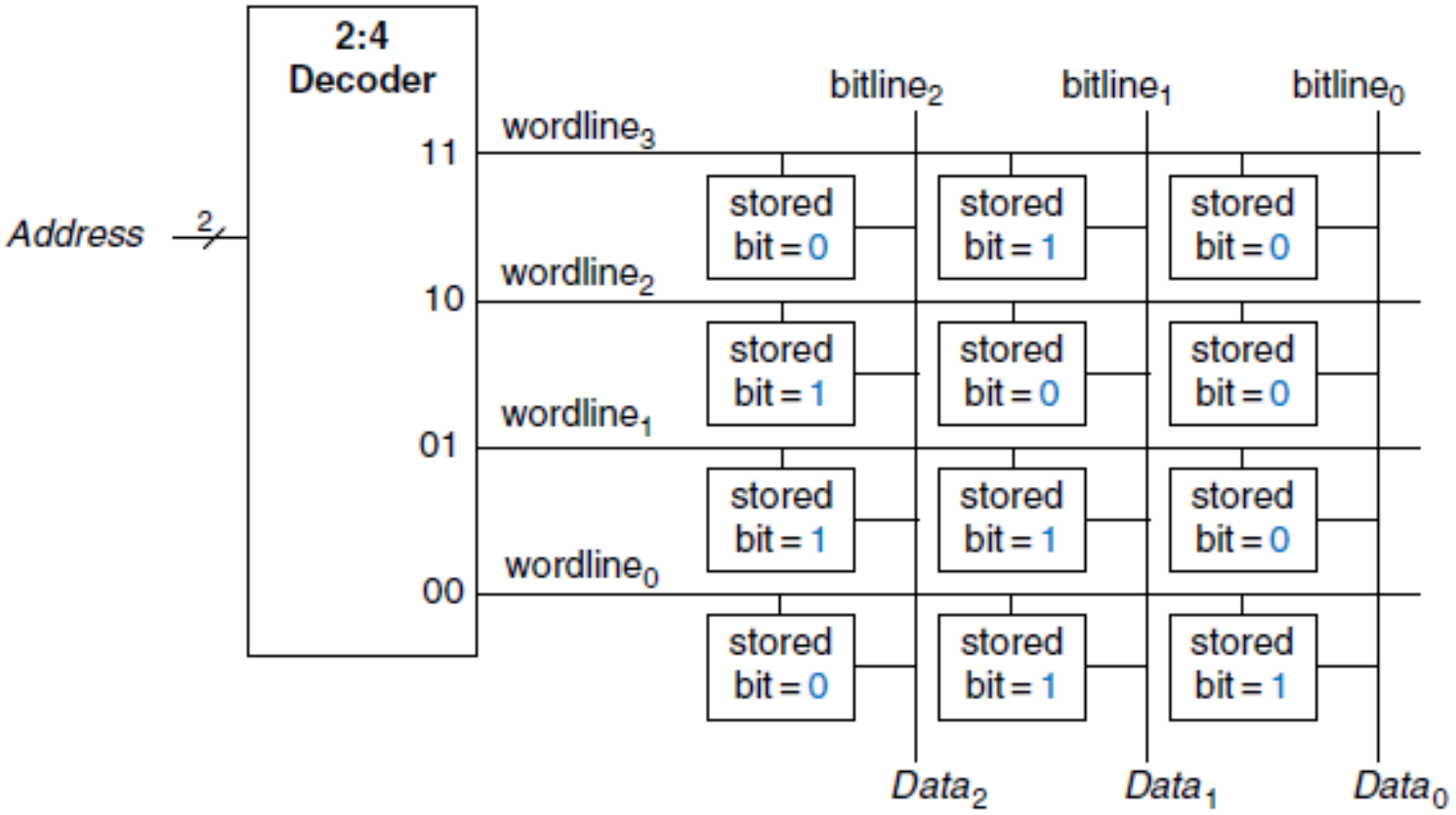
A. 512 B. 8 C. 32 D. 9

MEMORY ARRAYS (basic ideas)(*)



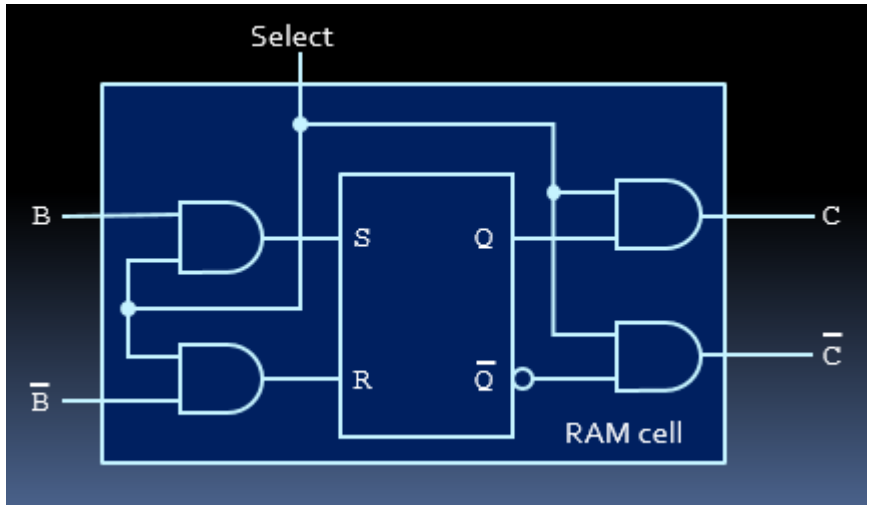
- Bit cell:

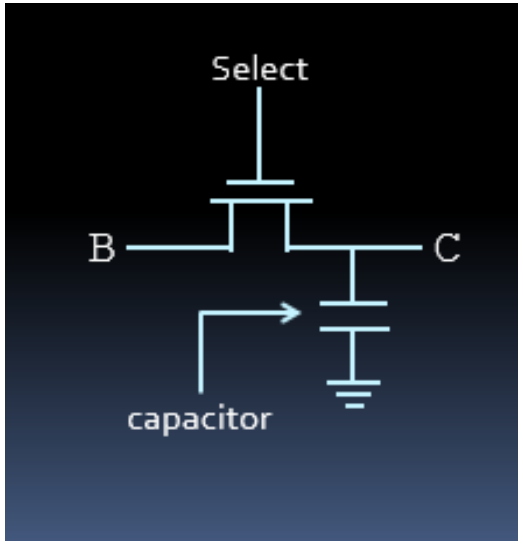
Memory arrays are built as an array of *bit cells*, each of which stores 1 bit of data.



Storage cells (*)

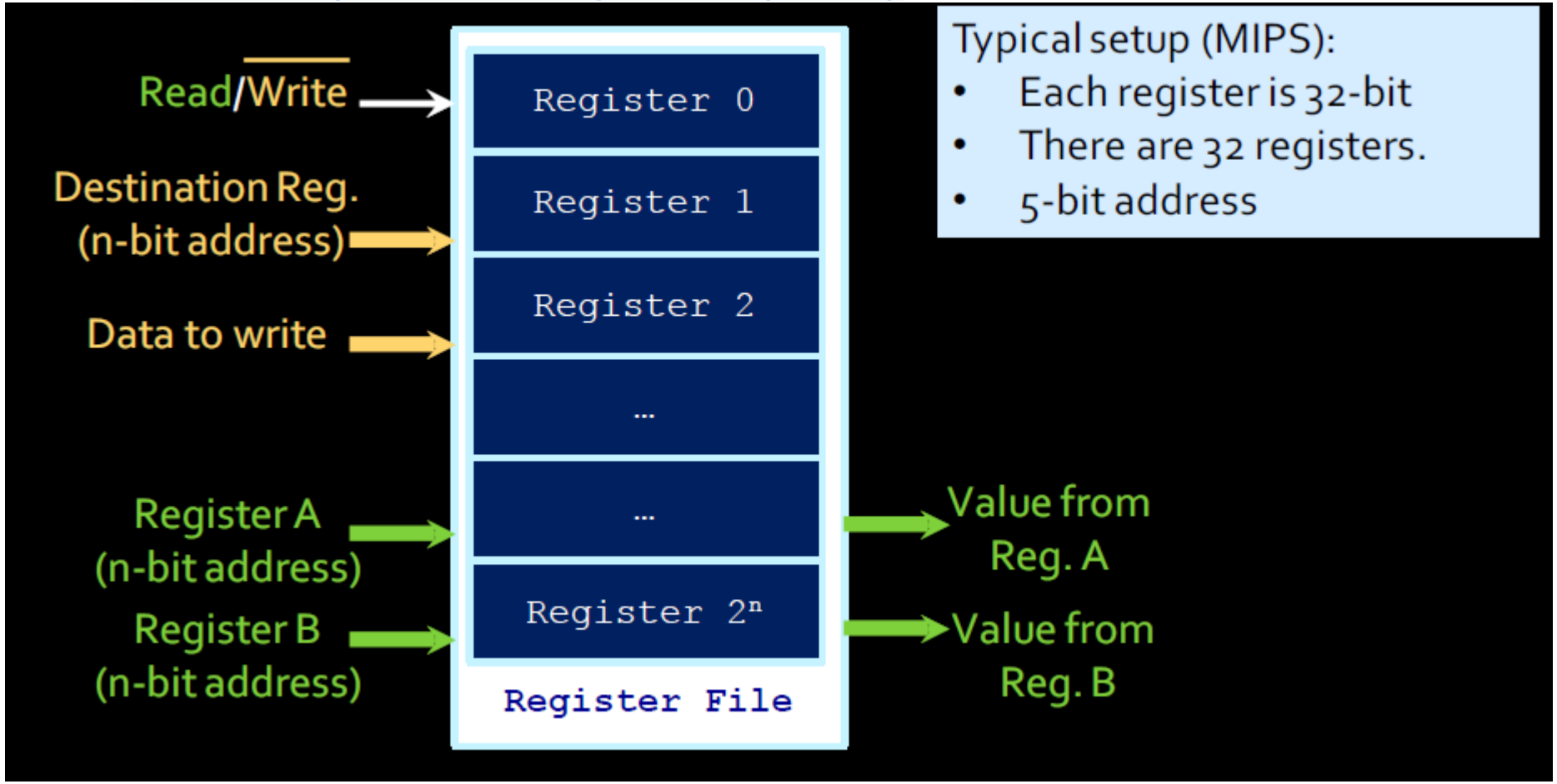
- Multiple ways of representing these cells.
  - e.g. RAM cell: DRAM IC cell:





Register File

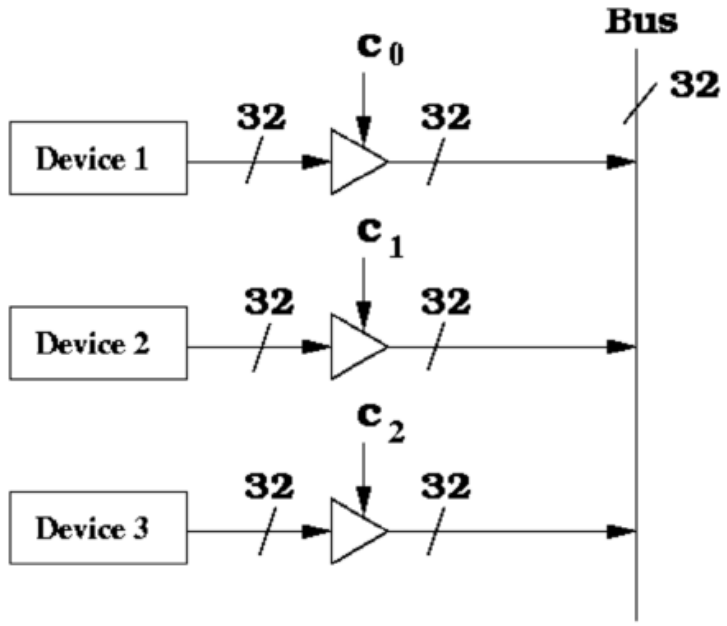
- A **register file** is an array of processor registers in a central processing unit (CPU).



DATA BUS and Tri-State Buffer

- BUS (总线): We have group of wires to carry information in order to communicate different parts of our computer system
- Tri-state Buffer
  - WE = 1 connected Y = A
  - WE= 0 disconnected Y = High Z

WE	A	Y
0	X	Z
1	0	0
1	1	1



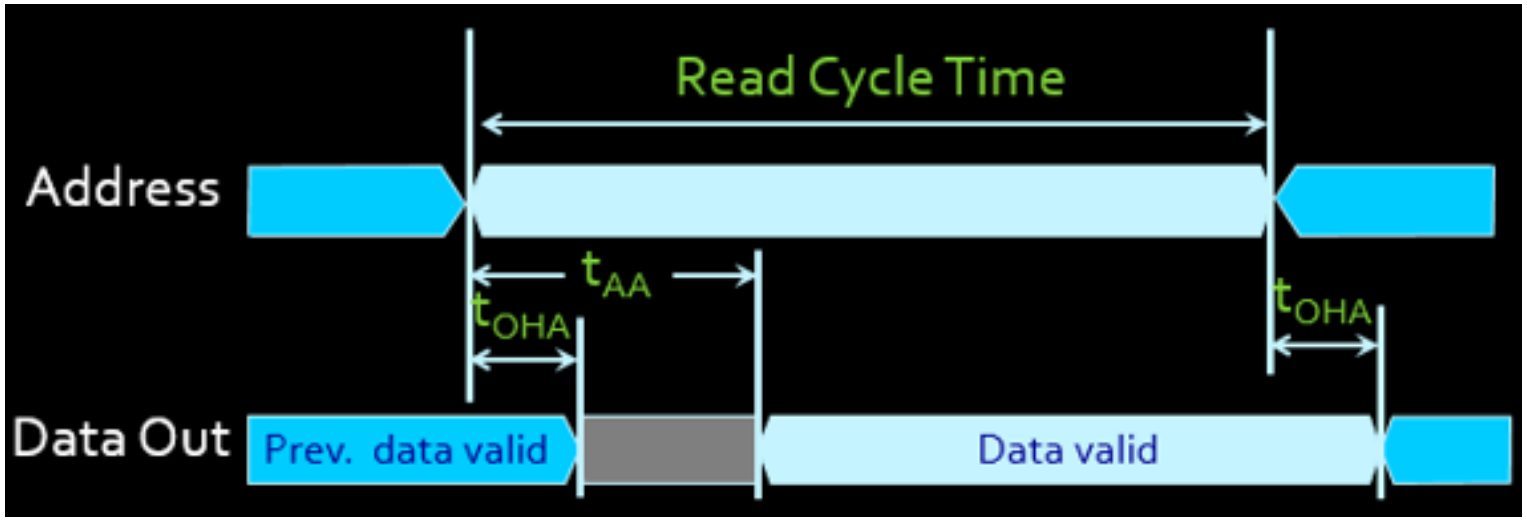
SRAM

- Input: Address, CE'(chip enable), Read/Write', OE'(Output Enable)
- Output: Data

Chip Enable' (CE')	Read/Write'	Output Enable' (OE')	Behavior
0	0	0	Write
0	1	0	Read
1	X	X	Not Enabled

考点（time types）

- 纯概念
- Read
  - t_AA: Address Access Time, time needed for address to be stable before reading data
  - t_OHA: Output Hold Time, time output data is held after change of address

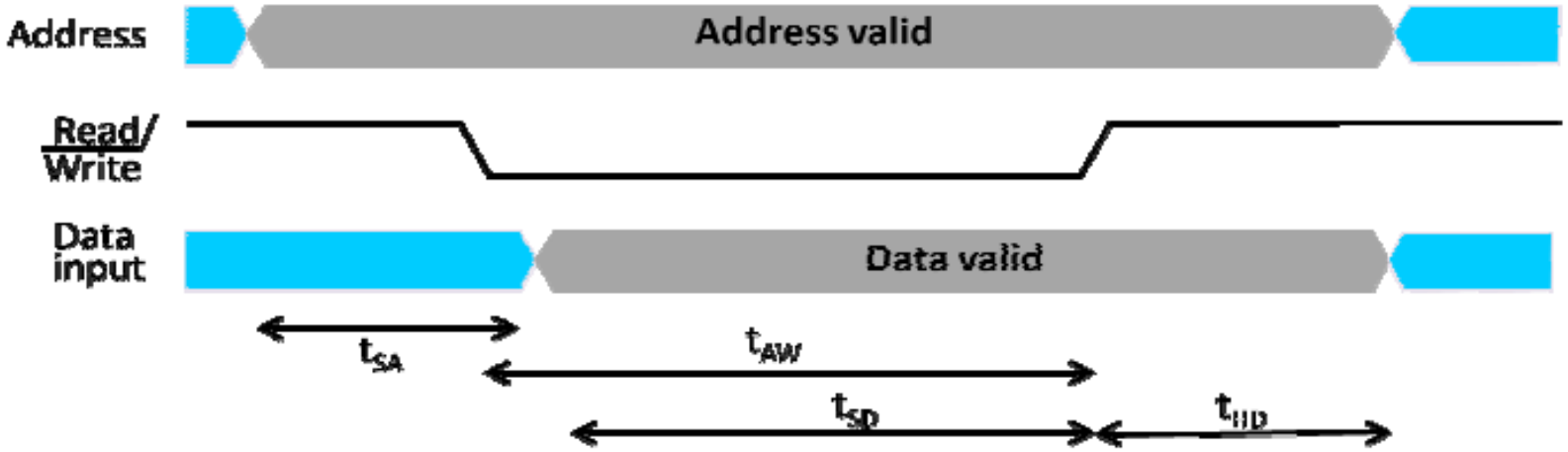


考点

- Write:
  - t_SA: Address set up time, time for address to be stable before enabling write signal
  - t_AW: Address width time
  - t_SD: Data Setup time to Write end, time for data-in value to be set up at desination
  - t_HD: data hold from write end, time for the data in value should stay unchanged after write signal changes.

Example

2. For the following write signal diagram, describe what each labeled time segment is called, and the purpose of each segment during a memory write operation. **(8 marks)**



t_{SA}: _____

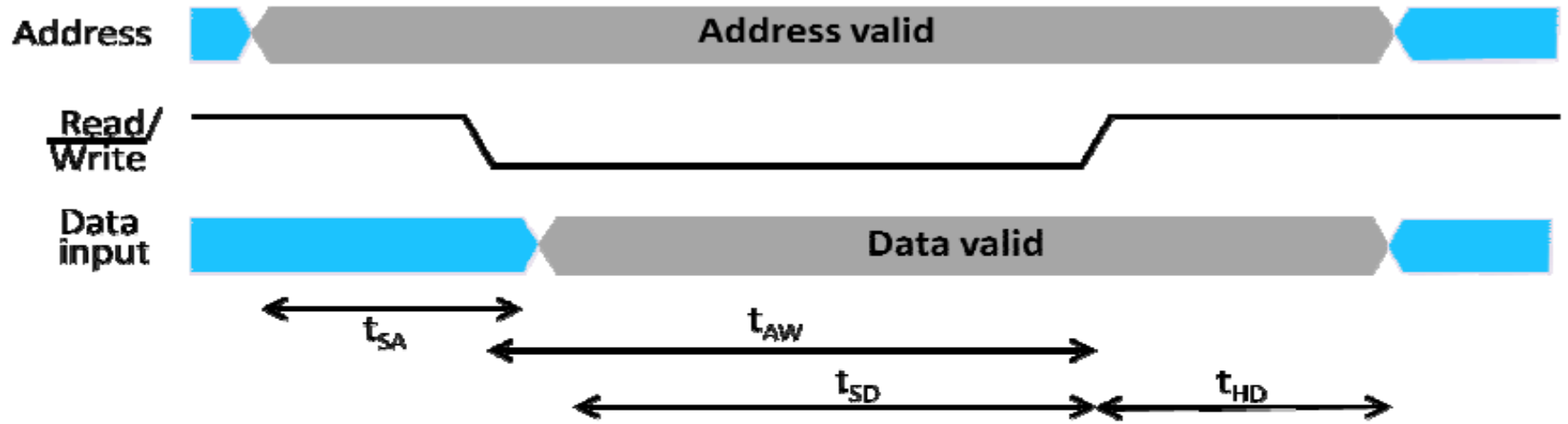
t_{AW}: _____

t_{SD}: _____

t_{HD}: _____

Answer

2. For the following write signal diagram, describe what each labeled time segment is called, and the purpose of each segment during a memory write operation. **(8 marks)**



t_{SA}: **Setup address time: Time needed for address to be stable before writing.**

t_{AW}: **Address width time: Time that write signal is high.**

t_{SD}: **Setup data time: Time needed for data values to be set up for write.**

t_{HD}: **Hold data time: Time needed to maintain data values after write signal falls.**

Review Question

- Q1 : A word-addressable RAM unit has 10 address bits going into it. How many bytes is the RAM unit able to store? (A word is 4 bytes, Word-addressable means each word has a unique address.)

- Solution: Each 4 bytes has a unique address. There are 2^10 = 1K unique addresses. So total size = 4 byte x 1K = 4KB
- Q2 : When reading from RAM, what are the values for CE' and OE' ?

- CE' = 0 , OE' = 0

CPU Control Unit (preview)

- The Control Unit controls how data flows in the **data path**.

- The **datapath** of a processor is a description/illustration of how the data flows between processor components during the execution of an operation.
  - Example:
    - Performing C = A+B is a different execution, aka, different datapath comparing with C = A->1 etc.

Lab 7