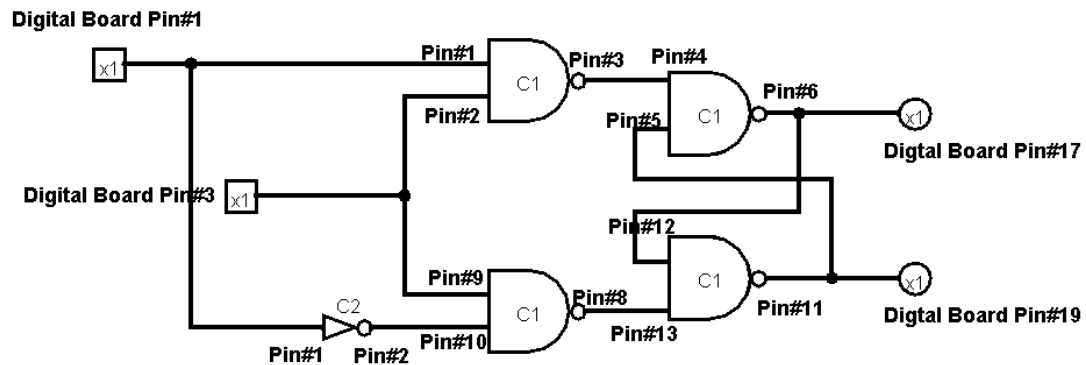


## CSC258 --- Lab4 Prelab

### Part1:

#### 1. Schematic of D Latch:



#### Chips used:

1. C1: 74LS00/03 2-input NAND
2. C2: 74LS 04/05 NOT

#### Connected to all chips:

Pin#7 – Gnd

Pin#14 – Vcc

4. the Clk should not be 0 for the first test. Since if the Clk is 0, the outputs remain. If at the first test, Clk set to be 0, the outputs will be undefined. After the first test, the outputs are defined, we can set the Clk to be 0 now.

```
vlib work
vlog -timescale 1ns/1ns lab4part2.v
vsim ALU
log {/*}
add wave {/*}
```

```
#7-seg decoder
```

```
#0: 1000000
```

```
#1: 1111001
```

```
#2: 0100100
```

```
#3: 0110000
```

```
#4: 0011001
```

```
#5: 0010010
```

```
#6: 0000010
```

```
#7: 1111000
```

```
#8: 0000000
```

```
#9: 0010000
```

```
#A: 0001000
```

```
#b: 0000011
```

```
#C: 1000110
```

```
#d: 0100001
```

```
#E: 0000110
```

```
#F: 0001110
```

```
# testing case 000 (keep reset unactive high)
```

```
# expect output: 02, 04, 10.
```

```
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[1]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[2]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50 -r 60
```

```
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50 -r 60
```

```
force {SW[9]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50 -r 60
```

```
force {SW[7]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
```

```
force {SW[6]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
```

```
force {SW[5]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
```

```
run 60ns
```

```
# testing case 001
```

```
# expect output: 00, 0F 1E
```

```
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[1]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[2]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[3]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
```

```

force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50 -r 60
force {SW[7]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
force {SW[6]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
force {SW[5]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50 -r 60
run 60ns

```

#testing case 010

```

# expect output:    00,          0F          1E
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[1]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[2]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[3]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50 -r 60
force {SW[7]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
force {SW[6]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[5]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
run 60ns

```

#testing case 011

```

#expect output:reset ot 00,      33,          FF
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 0 40, 0 50 -r 60
force {SW[1]} 0 0, 0 10, 1 20, 1 30, 0 40, 0 50 -r 60
force {SW[2]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50 -r 60
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50 -r 60
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50 -r 60
force {SW[7]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50 -r 60
force {SW[6]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50 -r 60
force {SW[5]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50 -r 60
run 60ns

```

#testing case 100

```

#expect output: reset,          00,          01,          01
force {SW[0]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50, 0 60, 0 70 -r 80
force {SW[1]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[2]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50, 0 60, 1 70 -r 80
force {SW[7]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[6]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[5]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
run 80ns

```

#testing case 101

```
#expect output: reset,          02,          08,          00
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 0 40, 0 50, 1 60, 1 70 -r 80
force {SW[1]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50, 0 60, 0 70 -r 80
force {SW[2]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50, 0 60, 1 70 -r 80
force {SW[7]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[6]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[5]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
run 80ns
```

#testing case 110

```
#expect output: reset,          06,          03,          00
force {SW[0]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[1]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 1 60, 1 70 -r 80
force {SW[2]} 0 0, 0 10, 1 20, 1 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
force {SW[9]} 0 0, 0 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50, 0 60, 1 70 -r 80
force {SW[7]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[6]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[5]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 0 60, 0 70 -r 80
run 80ns
```

#testing case 111

```
#expect output: 00,          03,          0F,          E1
force {SW[0]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[1]} 0 0, 0 10, 1 20, 1 30, 0 40, 0 50, 1 60, 1 70 -r 80
force {SW[2]} 0 0, 0 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[3]} 0 0, 0 10, 0 20, 0 30, 0 40, 0 50, 1 60, 1 70 -r 80
force {SW[9]} 1 0, 1 10, 1 20, 1 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {KEY[0]} 0 0, 1 10, 0 20, 1 30, 0 40, 1 50, 0 60, 1 70 -r 80
force {SW[7]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[6]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
force {SW[5]} 1 0, 1 10, 0 20, 0 30, 1 40, 1 50, 1 60, 1 70 -r 80
run 80ns
```