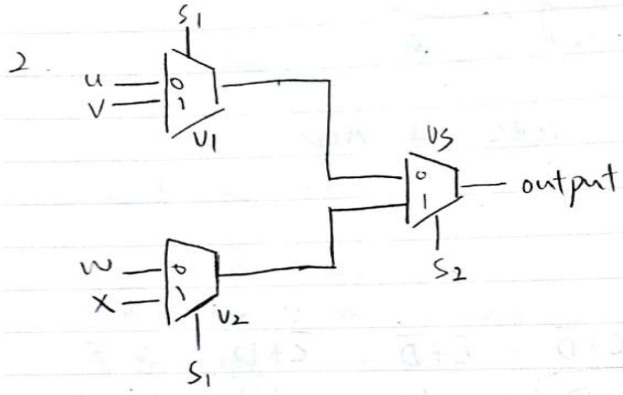
CSC258 Lab#2
Xin Luo/ Ruijie Sun 1003069706/

Part A (pre-lab)
Ruijie Sun:

Lab 2 Prelab

Part II
1. 2 rows for full

2.



Part III
1. ① HEX[0] high = 1, 4, b, d ⇔ 0001, 0100, 1011, 1101

low: 亮
high: 熄

X_3	X_2	X_1	X_0	HEX[0]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1

Y_3	Y_2	Y_1	Y_0	HEX[0]
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

	$\bar{X}_1\bar{X}_0$	$\bar{Y}_1X_0$	X_1X_0	$Y_1\bar{X}_0$
$\bar{Y}_3\bar{Y}_2$	0	(1)	0	0
X_3X_2	(1)	0	0	0
Y_3Y_2	0	(1)	0	0
$X_3\bar{X}_2$	0	0	(1)	0

$$HEX[0] = \bar{X}_3\bar{X}_2\bar{X}_1X_0 + \bar{X}_3X_2\bar{Y}_1\bar{X}_0 + Y_3Y_2\bar{Y}_1X_0 + Y_3\bar{X}_2X_1X_0$$

② HEX[1] high = 3, b, b, C, E, F ⇔ 0101, 0110, 1011, 1100, 1111, 1110

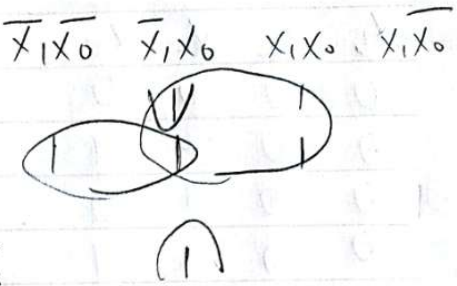
u	v	w	x	
Y_3	Y_2	Y_1	Y_0	HEX[1]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1 ($\bar{Y}_3Y_2\bar{Y}_1Y_0$)
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1 ($X_3\bar{X}_2X_1X_0$)
1	1	0	0	1 ($Y_3Y_2\bar{Y}_1\bar{Y}_0$)
1	1	0	1	0
1	1	1	0	1 ($Y_3Y_1X_1\bar{Y}_0$)
1	1	1	1	1

	$\bar{Y}_1\bar{Y}_0$	$\bar{Y}_1X_0$	X_1X_0	$Y_1\bar{Y}_0$
$\bar{Y}_3\bar{Y}_2$	0	0	0	0
$\bar{Y}_3Y_2$	0	(1)	1	(1)
Y_3Y_2	(1)	0	(1)	(1)
$Y_3\bar{Y}_2$	0	0	(1)	0

$$HEX[1] = Y_3X_1\bar{Y}_0 + \bar{Y}_3X_2\bar{X}_1X_0 + Y_3X_1Y_0 + Y_2X_1\bar{Y}_0$$

HEX[4] high: 1, 3, 4, 5, 7, 9 ⇔ 0001, 0011, 0100, 0101, 0111, 1001

X_3	X_2	X_1	X_0	HEX[4]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



$HEX[4] = X_0\bar{X}_3 + \bar{X}_1X_0\bar{X}_2 + \bar{X}_3X_2\bar{X}_1$

③ HEX[2] high = 2 C E F ∈ 0010, 1100, 1110, 1111

u X_3	v X_2	w Y_1	x X_0	HEX[2]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	0	0	0	0
$\bar{X}_3X_2$	0	0	0	0
X_3X_2	1	0	1	1
$X_3\bar{X}_2$	0	0	0	0

$HEX[2] = \bar{Y}_3Y_2X_1\bar{Y}_0 + X_1Y_2Y_3 + \bar{X}_0Y_2Y_3$

④ HEX[3] high = 1 4 7 9 A F ∈ 0001, 0100, 0111, 1001, 1011, 1111

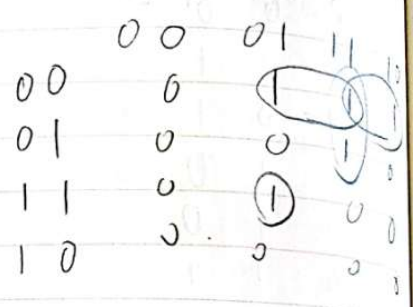
Y_3	Y_2	Y_1	X_0	HEX[3]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	$X_1\bar{X}_0$	X_1X_0
$\bar{Y}_3\bar{Y}_2$	0	1	0	0
$\bar{Y}_3Y_2$	1	0	0	0
Y_3Y_2	0	0	1	0
$Y_3\bar{Y}_2$	0	1	0	1

$HEX[3] = \bar{Y}_3Y_2\bar{Y}_1\bar{X}_0 + \bar{Y}_2\bar{Y}_1X_0 + Y_2Y_1X_0 + Y_3\bar{Y}_2X_1\bar{X}_0$

HEX[5] high: 1 2 3 7 d ⇐ 0001, 0010, 0011, 0111, 1101

X_3	X_2	X_1	X_0	HEX[5]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



$HEX[5] = X_3X_2\bar{X}_1X_0 + \bar{X}_3\bar{Y}_2X_0 + \bar{Y}_3\bar{Y}_2X_1 + \bar{X}_3X_1Y_0$

✓

HEX[6] high: 0 1 7 ($\equiv$ 0000, 0001, 0111, 1100)

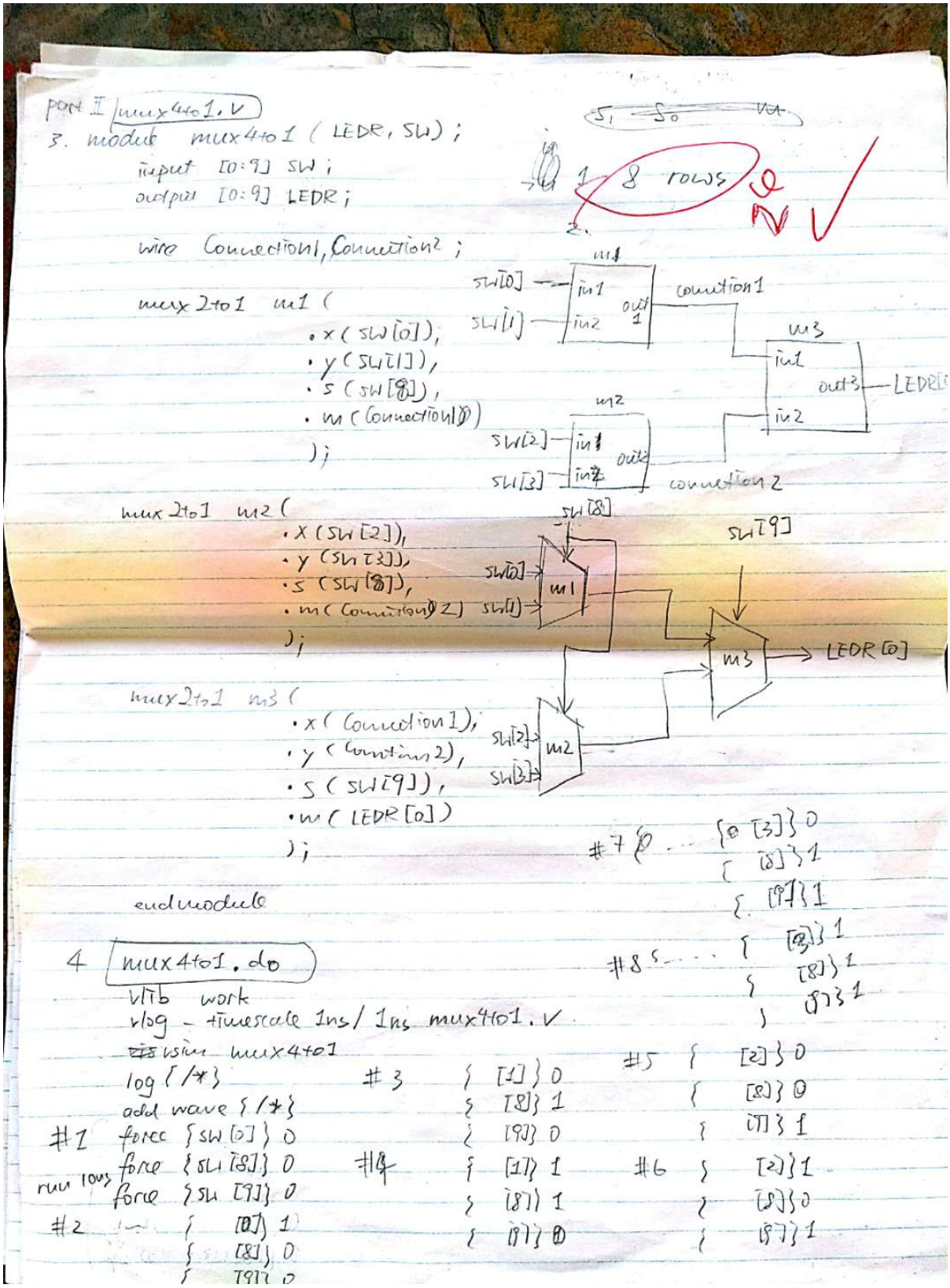
X_3	X_2	X_1	X_0	HEX[6]
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	1	1	0	0
$\bar{X}_3X_2$	0	0	1	0
X_3X_2	1	0	0	0
$X_3\bar{X}_2$	0	0	0	0

$HEX[6] = \bar{X}_3\bar{X}_2\bar{X}_1 + \bar{X}_3X_2X_1X_0 + X_3X_2\bar{X}_1\bar{X}_0$

✓

Xin Luo:


part II mux4to1.v
3. module mux4to1 (LEDR, SW);
input [0:9] SW;
output [0:9] LEDR;
wire Connection1, Connection2;
mux 2to1 u1 (
.x (SW[0]),
.y (SW[1]),
.s (SW[8]),
.m (Connection1)
);
mux 2to1 u2 (
.x (SW[2]),
.y (SW[3]),
.s (SW[8]),
.m (Connection2)
);
mux 2to1 u3 (
.x (Connection1),
.y (Connection2),
.s (SW[9]),
.m (LEDR[0])
);
endmodule
4 mux4to1.do
vlib work
vlog -timescale 1ns/1ns mux4to1.v
vsim mux4to1
log {/*}
add wave {/*}
#1 force {SW[0]} 0
force {SW[8]} 0
run 10ns
force {SW[9]} 0
#2 {[0]} 1
{[8]} 0
{[9]} 0
#3 {[1]} 0
{[8]} 1
{[9]} 0
#4 {[1]} 1
{[8]} 1
{[9]} 0
#5 {[2]} 0
{[8]} 0
{[9]} 1
#6 {[2]} 1
{[8]} 0
{[9]} 1
#7 {[3]} 0
{[8]} 1
{[9]} 1
#8 {[3]} 1
{[8]} 1
{[9]} 1
1 8 rows
u1
u2
u3
in1
in2
out
connection1
connection2
LEDR[0]
SW[8]
SW[9]

Part 三.

1. HEX[0] high. = 1, 4, b, d ⇒ 0001, 0100, 1011, 1101

X_3	X_2	X_1	X_0	HEX[0]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	0	(1)	0	0
$\bar{X}_3X_2$	(1)	0	0	0
X_3X_2	0	(1)	0	0
$X_3\bar{X}_2$	0	0	(1)	0

$HEX[0] = \bar{X}_3\bar{X}_2\bar{X}_1X_0 + \bar{X}_3X_2\bar{X}_1\bar{X}_0 + \bar{X}_3X_2\bar{X}_1X_0 + X_2\bar{X}_2X_1X_0$

✓

HEX[1] high = 5, 6, b, C, E, F ⇒ 0101, 0110, 1011, 1100,

X_3	X_2	X_1	X_0	HEX[1]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	0	0	0	0
$\bar{X}_3X_2$	0	(1)	0	(1)
X_3X_2	(1)	0	(1)	(1)
$X_3\bar{X}_2$	0	0	(1)	

$HEX[1] = X_3X_2\bar{X}_1\bar{X}_0 + \bar{X}_3X_2\bar{X}_1X_0 + X_3X_1X_0 + X_2X_1\bar{X}_0$

✓

HEX[2] high : 2 C E F ⇒ 0010, 1100, 1110, 1111

X_3	X_2	X_1	X_0	HEX[2]
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	0	0	0	1
$\bar{X}_3X_2$	0	0	0	0
X_3X_2	1	0	1	1
$X_3\bar{X}_2$	0	0	0	0

$$HEX[2] = \bar{X}_3\bar{X}_2X_1\bar{X}_0 + X_3X_2X_1 + X_3X_2\bar{X}_0$$

HEX[3] high : 1 4 7 9 A F ⇒ 0001, 0100, 0111, 1001, 1010, 1111

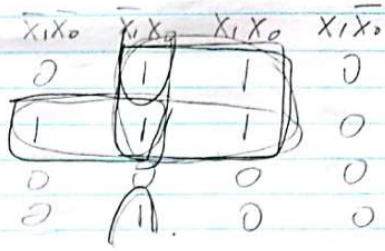
X_3	X_2	X_1	X_0	HEX[3]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	0	1	0	0
$\bar{X}_3X_2$	1	0	1	0
X_3X_2	0	0	1	0
$X_3\bar{X}_2$	0	1	0	1

$$HEX[3] = \bar{X}_3X_2\bar{X}_1\bar{X}_0 + \bar{X}_2\bar{X}_1X_0 + X_2X_1X_0 + X_3\bar{X}_2\bar{X}_1\bar{X}_0$$

HEX[4] high = 1 3 4 5 7 9 ⇒ 0001, 0011, 0100, 0101, 0111

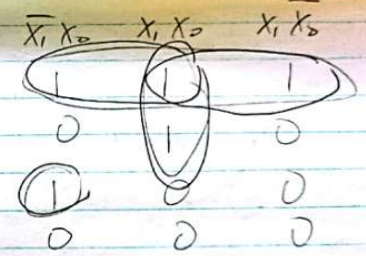
x_3	x_2	x_1	x_0	HEX[4]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



$$HEX[4] = \bar{x}_3 x_0 + \bar{x}_3 x_2 \bar{x}_1 + \bar{x}_2 \bar{x}_1 x_0$$

HEX[5] high = 1 2 3 7 d ⇒ 0001, 0010, 0011, 0111, 1101

x_3	x_2	x_1	x_0	HEX[5]
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



$$HEX[5] = \bar{x}_3 x_1 x_0 + \bar{x}_3\bar{x}_2 x_0 + \bar{x}_3\bar{x}_2 x_1 + x_3 x_2 \bar{x}_1 x_0$$

HEX[6] high: 0 1 7 C ⇒ 0000, 0001, 0111, 1100

X_3	X_2	X_1	X_0	HEX[6]
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

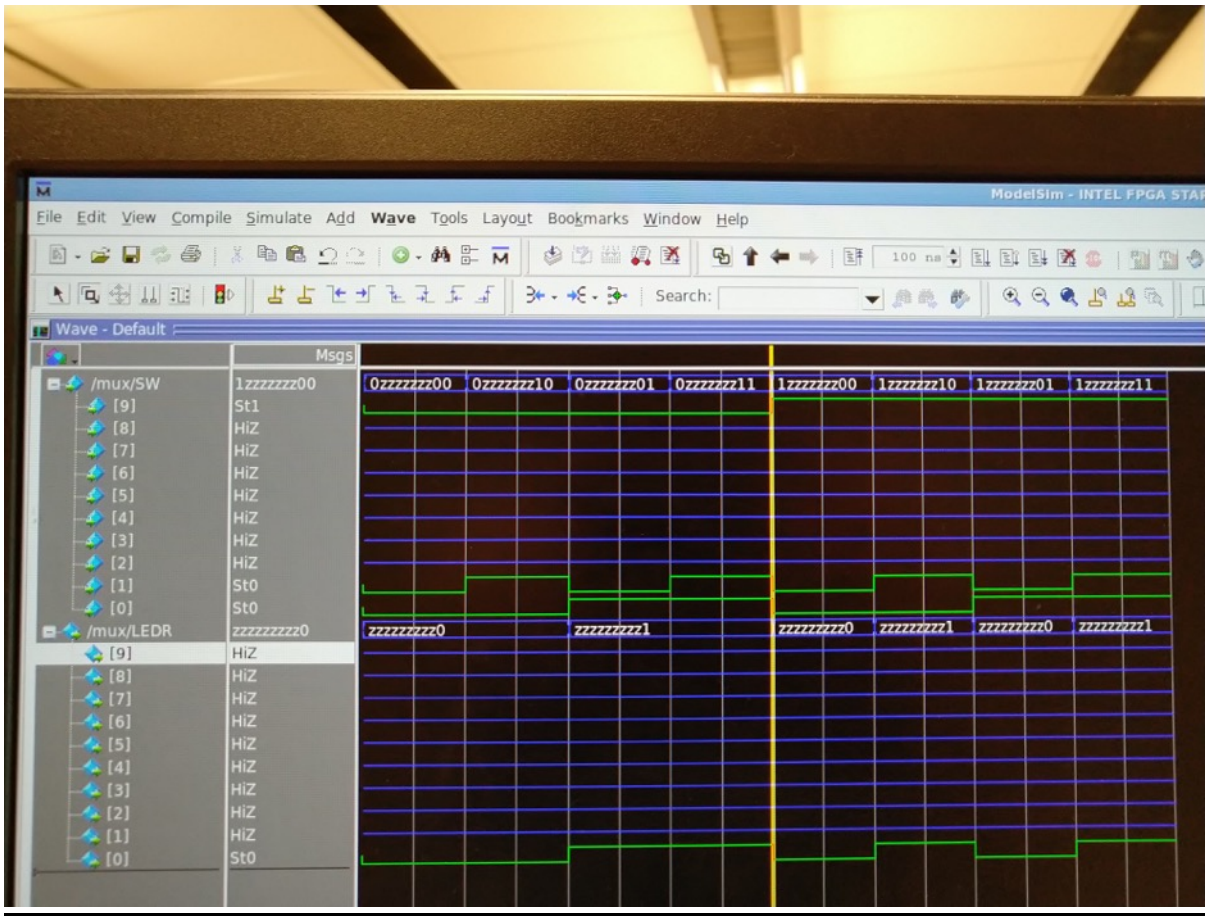
	$\bar{X}_1\bar{X}_0$	$\bar{X}_1X_0$	X_1X_0	$X_1\bar{X}_0$
$\bar{X}_3\bar{X}_2$	1	1	0	0
$\bar{X}_3X_2$	0	0	0	0
X_3X_2	1	0	0	0
$X_3\bar{X}_2$	0	0	0	0

$HEX(6) = \bar{X}_3\bar{X}_2\bar{X}_1 + X_3X_2\bar{X}_1\bar{X}_0 + \bar{X}_3X_2X_1$

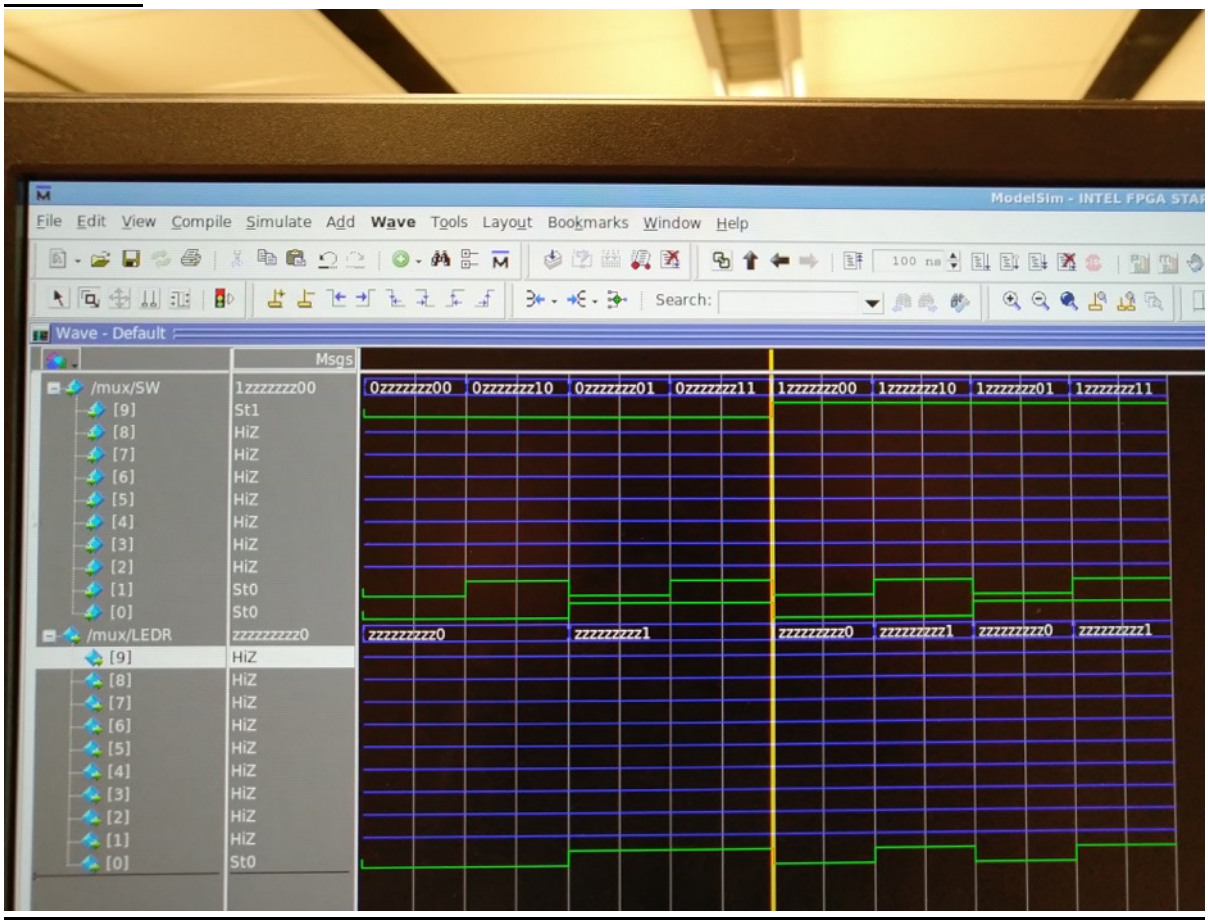
```
module 7_segment_decoder( C3, C2, C1, C0, h6, h5, h4, h3, h2, h1, h0 );
  input C3, C2, C1, C0;
  output h6, h5, h4, h3, h2, h1, h0;
  assign h0 = (~C3 & ~C2 & ~C1 & C0 | ~C3 & C2 & ~C1 & ~C0 |
               ~S[3] & ~S[2] & ~S[1] & S[0] | S[3] & ~S[2] & S[1] & S[0] )
  assign HEX[1] = (S[3] & S[2] & ~S[1] & ~S[0] | ~S[3] & S[2] & ~S[1] & S[0]
                 | S[3] & S[1] & S[0] | S[2] & S[1] & ~S[0] )
  assign HEX[2] = (~S[3] & ~S[2] & S[1] & ~S[0] | S[3] & S[2] & S[1] |
                   S[3] & S[2] & ~S[0])
  assign HEX[3] = (~S[3] & S[2] & ~S[1] & ~S[0] | ~S[2] & ~S[1] & S[0] |
                   S[2] & S[1] & S[0] | S[3] & ~S[2] & S[1] & ~S[0] )
  assign HEX[4] = (~S[3] & S[0] | ~S[3] & S[2] & ~S[1] | ~S[2] & S[1] & S[0])
  assign HEX[5] = (~S[3] & S[1] & S[0] | ~S[3] & ~S[2] & S[1] |
                   ~S[3] & ~S[2] & S[0] | S[3] & S[2] & ~S[1] & S[0])
  assign HEX[6] = (~S[3] & ~S[2] & S[1] | S[3] & S[2] & ~S[1] & ~S[0] |
                   ~S[3] & S[2] & S[1] & S[0])
end module
```

Part B (simulation for part1):

Ruijie Sun:



Xin Luo:



Short answer 3:

The output on the FPGA chip matches the the simulation .

Short answer 4:

The time we need to compile the verilog file and test the results on the FPGA chip is much longer then we directly simulate the result on the ModelSim using .do file.

Part C (Verilog code for Part2)

Ruijie Sun:

```
module mux4to1(u,v,w,x,s1,s2,m);
   input u; //selected when s1 is 0 and s2 is 0
   input v; //selected when s1 is 0 and s2 is 1
        input w; //selected when s1 is 1 and s2 is 0
   input x; //selected when s1 is 1 and s2 is 1
   input s1; //select signal # 1
        input s2; //select signal # 2
        wire A;
        wire B;
        output m; //output

        mux2to1 m1(
          .x(u),
                    .y(v),
                    .s(s1),
                    .m(A)
        );
        mux2to1 m2(
          .x(w),
                    .y(x),
                    .s(s1),
                    .m(B)
        );
        mux2to1 m3(
          .x(A),
                    .y(B),
                    .s(s2),
                    .m(m)
        );
```

```
endmodule

module mux2to1(x, y, s, m);
    input x; //selected when s is 0
    input y; //selected when s is 1
    input s; //select signal
    output m; //output

    assign m = s & y | ~s & x;
    // OR
    // assign m = s ? y : x;

endmodule
```

Xin Luo:

part II mux4to1.v

```
3. module  mux4to1 ( LEDR, SW) ;
        input  [0:9] SW ;
        output [0:9] LEDR ;

        wire Connection1, Connection2 ;

        mux 2to1  m1 (
                        .x ( SW[0]),
                        .y ( SW[1]),
                        .s ( SW[8]),
                        .m ( Connection1)
                        );

        mux 2to1  m2 (
                        .x (SW[2]),
                        .y (SW[3]),
                        .s (SW[8]),
                        .m ( Connection2)
                        );

        mux 2to1  m3 (
                        .x ( Connection1),
                        .y ( Connection2),
                        .s ( SW[9]),
                        .m ( LEDR[0])
                        );

        endmodule
```

PartD: (Verilog code for part3):

Ruijie Sun:

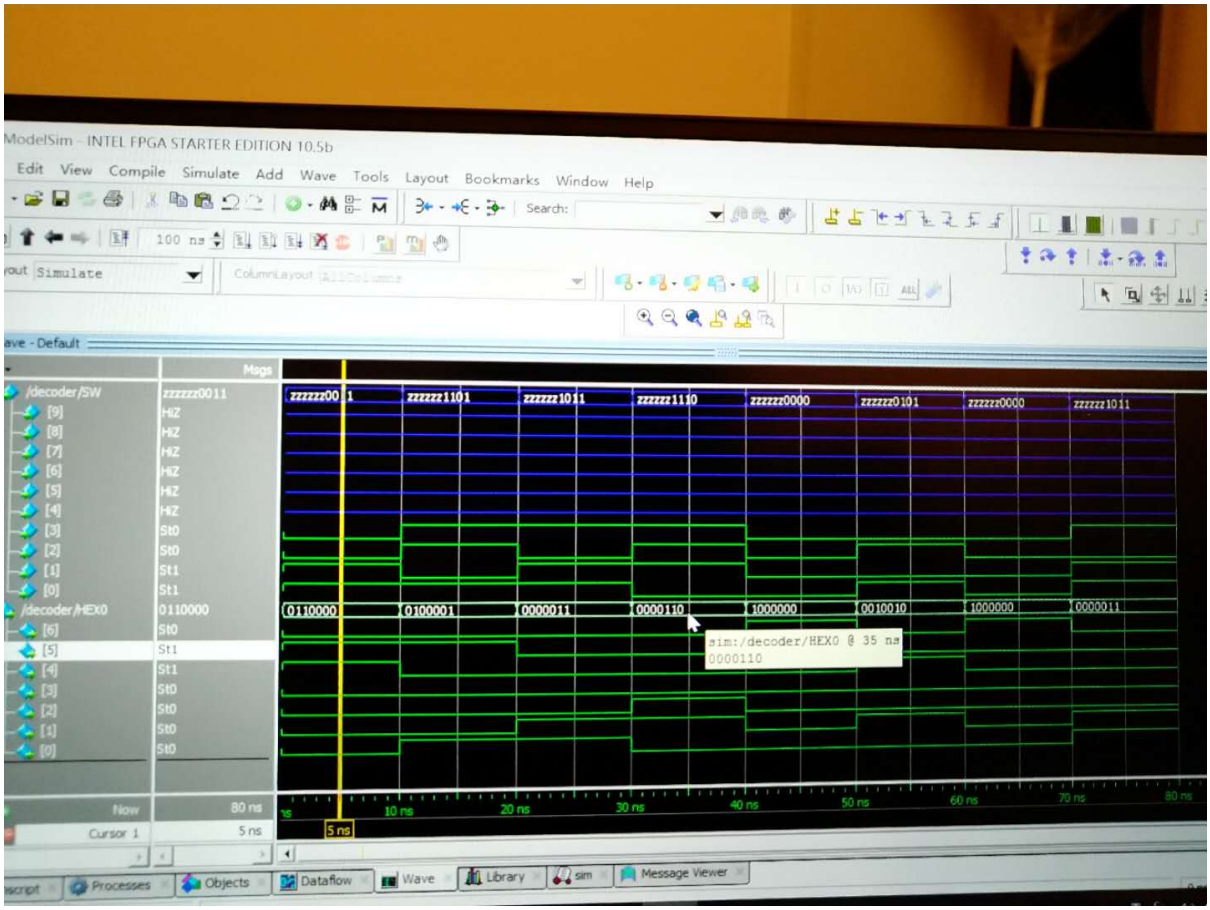
```
module decoder(HEX0, SW);
   input [9:0] SW;
   output [6:0] HEX0;

   decoderr u0(
      .u(SW[0]),
      .v(SW[1]),
      .w(SW[2]),
      .x(SW[3]),
      .HEX00(HEX0[0]),
                .HEX01(HEX0[1]),
                .HEX02(HEX0[2]),
                .HEX03(HEX0[3]),
                .HEX04(HEX0[4]),
                .HEX05(HEX0[5]),
                .HEX06(HEX0[6])
      );
endmodule


module
decoderr(u,v,w,x,HEX00,HEX01,HEX02,HEX03,HEX04,HEX05,HEX06);
   input u;
   input v;
        input w;
   input x;
        output HEX00;
        output HEX01;
        output HEX02;
        output HEX03;
```

```
        output HEX04;
        output HEX05;
        output HEX06;
   assign HEX00 = ~u & ~v & ~w &x | ~u & v & ~w & ~x| u & ~v & w & x | u & v & ~w & x ;
        assign HEX01 = ~u & v & ~w & x | u & w & x | u & v & ~x | v & w & ~x ;
        assign HEX02 = u & v & ~x | ~v & w & ~x;
        assign HEX03 = ~u & v & ~w & ~x | ~v & ~w & x | v & w & x | u & ~v & w & ~x ;
        assign HEX04 = ~u & v & ~w | ~v & ~w & x | ~u & x ;
        assign HEX05 = ~u & ~v & x | ~u & ~v & w | ~u & w & x | u & v & ~w & x ;
        assign HEX06 = ~u & ~v & ~w | ~u & v & w & x | u & v & ~w & ~x ;

endmodule
```



Xin Luo:

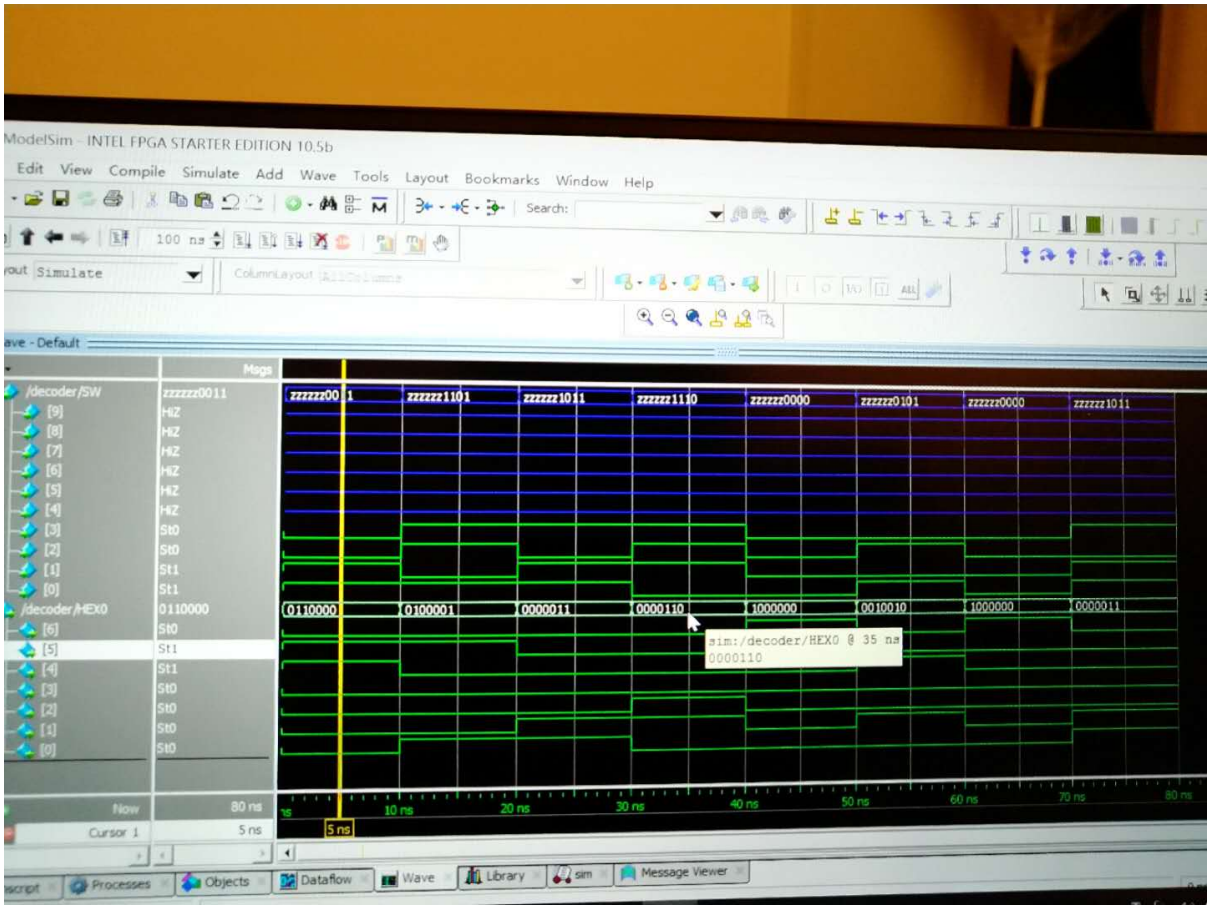
```
module 7_segment_decoder( C3, C2, C1, C0, h6, h5, h4, h3, h2, h1, h
    input C3, C2, C1, C0;
    output h6, h5, h4, h3, h2, h1, h0;
    assign h0 = (~C3 & ~C2 & ~C1 & C0 | ~C3 & C2 & ~C
        ~S[3] & ~S[2] & ~S[1] & S[0] | S[3] & ~S[2] & S[1] & S[0] )
    assign HEX[1] = ( S[3] & S[2] & ~S[1] & ~S[0] | ~S[3] & S[2] & ~S[1] & S[0]
        | S[3] & S[1] & S[0] | S[2] & S[1] & ~S[0] )
    assign HEX[2] = ( ~S[3] & ~S[2] & S[1] & ~S[0] | S[3] & S[2] & S[1] |
        S[3] & S[2] & ~S[0])
    assign HEX[3] = ( ~S[3] & S[2] & ~S[1] & ~S[0] | ~S[2] & ~S[1] & S[0] |
        S[2] & ~S[1] & S[0] | S[3] & ~S[2] & S[1] & ~S[0])
    assign HEX[4] = ( ~S[3] & S[0] | ~S[3] & S[2] & ~S[1] | ~S[2] & S[1] & S[0])
    assign HEX[5] = ( ~S[3] & S[1] & S[0] | ~S[3] & ~S[2] & S[1] |
        ~S[3] & S[2] & ~S[1] & S[0])
    assign HEX[6] = ( ~S[3] & ~S[2] & S[1] | S[3] & S[2] & ~S[1] & ~S[0] |
        ~S[3] & S[2] & S[1] & S[0])
endmodule
```

```
module 7_seg_decoder( SW, HEX0 );
    input [3:0] SW;
    output [6:0] HEX0;

    7_segment_decoder S1 (
        .C3 (SW[3]),
        .C2 (SW[2]),
        .C1 (SW[1]),
        .C0 (SW[0]),
        .h6 (HEX0[6]),
        .h5 (HEX0[5]),
        .h4 (HEX0[4]),
        .h3 (HEX0[3]),
        .h2 (HEX0[2]),
        .h1 (HEX0[1]),
        .h0 (HEX0[0])
        );
endmodule
```

4-bit input

6-bit output



Part E:

1. We can be familiar with the process of handling the FPGA chip and understand how the circuit work.
2. The most interesting part of this lab is to do it by our self instead of learn from book.
3. If there can be more TAs in the lab to check our work, the lab time will be much shorter because most people finish their work but TA don't have time to check, we always need to wait for a longer time than we actually need.