UNIVERSITY OF TORONTO

Solutions

Fall 2014 Midterm

Solutions

CSC258: Computer Organization

Duration: 2 hours

October 23rd, 2014

Last Name: _____

First Name: _____

Student Number: _____

Instructor: Steve Engels

Instructions:

- **Write your name on the back of this exam paper.**
- **Do not open this exam until you hear the signal to start.**
- Have your student ID on your desk.
- No aids permitted other than writing tools. Keep all bags and notes far from your desk before the exam begins.
- There are 4 questions on 8 pages. When you hear the signal to start, make sure that your exam is complete before you begin.
- Read over the entire exam before starting.
- If you use any space for rough work or have to user the overflow page, clearly indicate the section(s) that you want marked.

Mark Breakdown

Part A:	**/ 19**
Part B:	**/ 24**
Part C:	**/ 9**
Part D:	**/ 14**
Bonus:	**/ 1**
Total:	**/ 66**

Part A: Short Answer (19 marks)

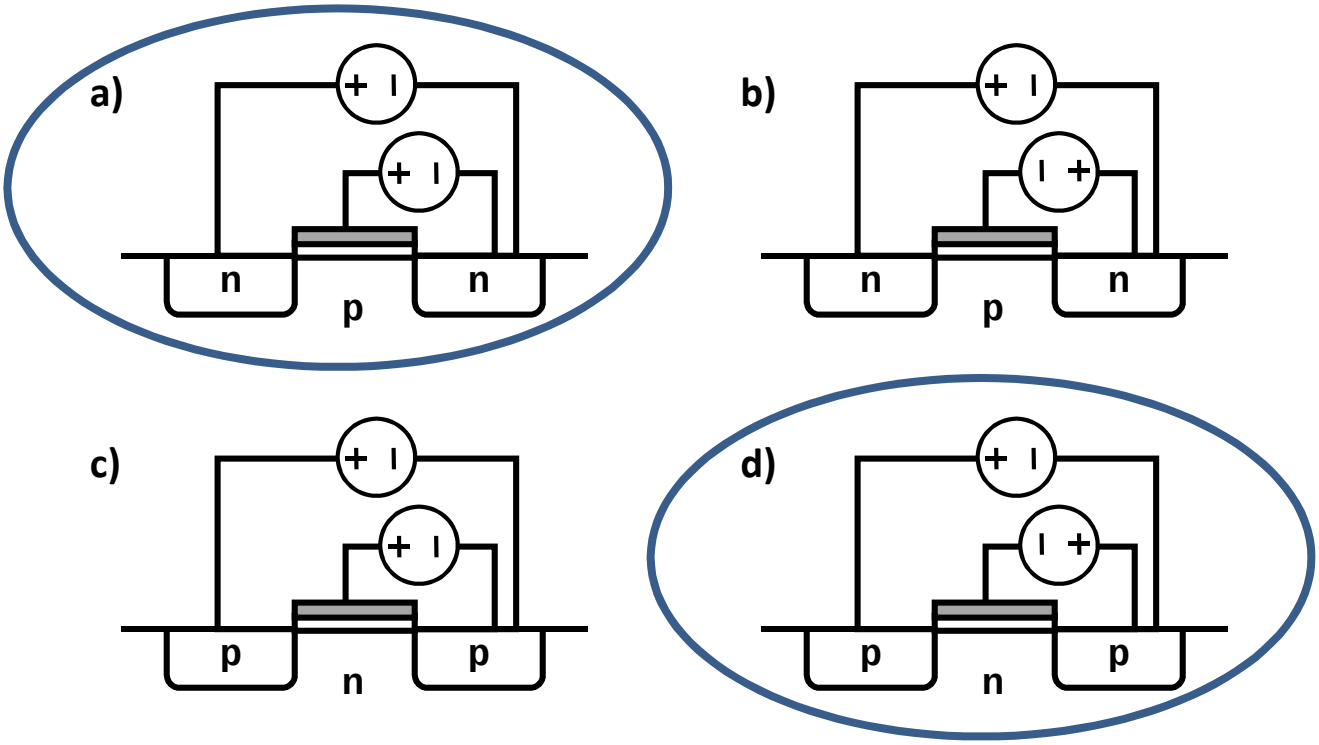
Answer the following questions in the space provided. When providing a written answer, write **as clearly and legibly as possible**. Marks will not be awarded to unreadable answers.

1. In the spaces below, write the lowest possible values for signed and unsigned 8-bit binary numbers. Also provide the equivalent decimal value for each binary number. **(2 marks)**

Signed binary value: 10000000 **Decimal value:** -128

Unsigned binary value: 00000000 **Decimal value:** 0

2. Which of the following MOSFET configurations would cause current to flow between the source and the drain? Circle all that apply. **(2 marks)**



3. When phosphorus atoms are added to silicon, which of the following statements is true about the resulting material? Circle all the answers that apply. **(2 marks)**

a) The resulting material has an overall positive charge.

b) The resulting material has an overall negative charge.

c) The resulting material has a higher number of holes.

d) The resulting material has a higher number of electrons.

4. Assume that Y, A and B are all 1-bit binary values. Which of the following Verilog statements set output Y high when inputs A and B have different values? Circle all that apply. **(2 marks)**

a) `and(Y, A, B);`

b) `xor(Y, A, B);`

c) `or(Y, A, B);`

d) `nand(Y, A, B);`

e) `nor(Y, A, B);`

5. Given binary inputs A, B, C and D, which of the following are valid minterms? Circle all that apply. **(3 marks)**

a) $A \cdot B + C \cdot D$

b) $A+B+C+D$

c) $A \cdot B \cdot C$

d) $D \cdot C \cdot B \cdot A$

e) $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

f) $A+B \cdot C$

6. For each description below, fill in the blank with the correct transistor term. **(5 marks)**

The region caused by electrons and holes cancelling each other out. depletion layer

The addition of impurities such as phosphorus or boron to silicon. doping

The application of a voltage that causes junction current to stop flowing. reverse bias

The material between the gate and the main silicon layer. oxide

The charge carriers in a p-type material. holes

7. How many flip-flops are needed to implement a 100-state finite state machine? **(1 mark)**

$$\lceil \log_2 100 \rceil = 7$$

8. What values on R and S are considered to be the "forbidden state" of inputs on an RS flip-flop? **(1 mark)**

R: 1 **S:** 1

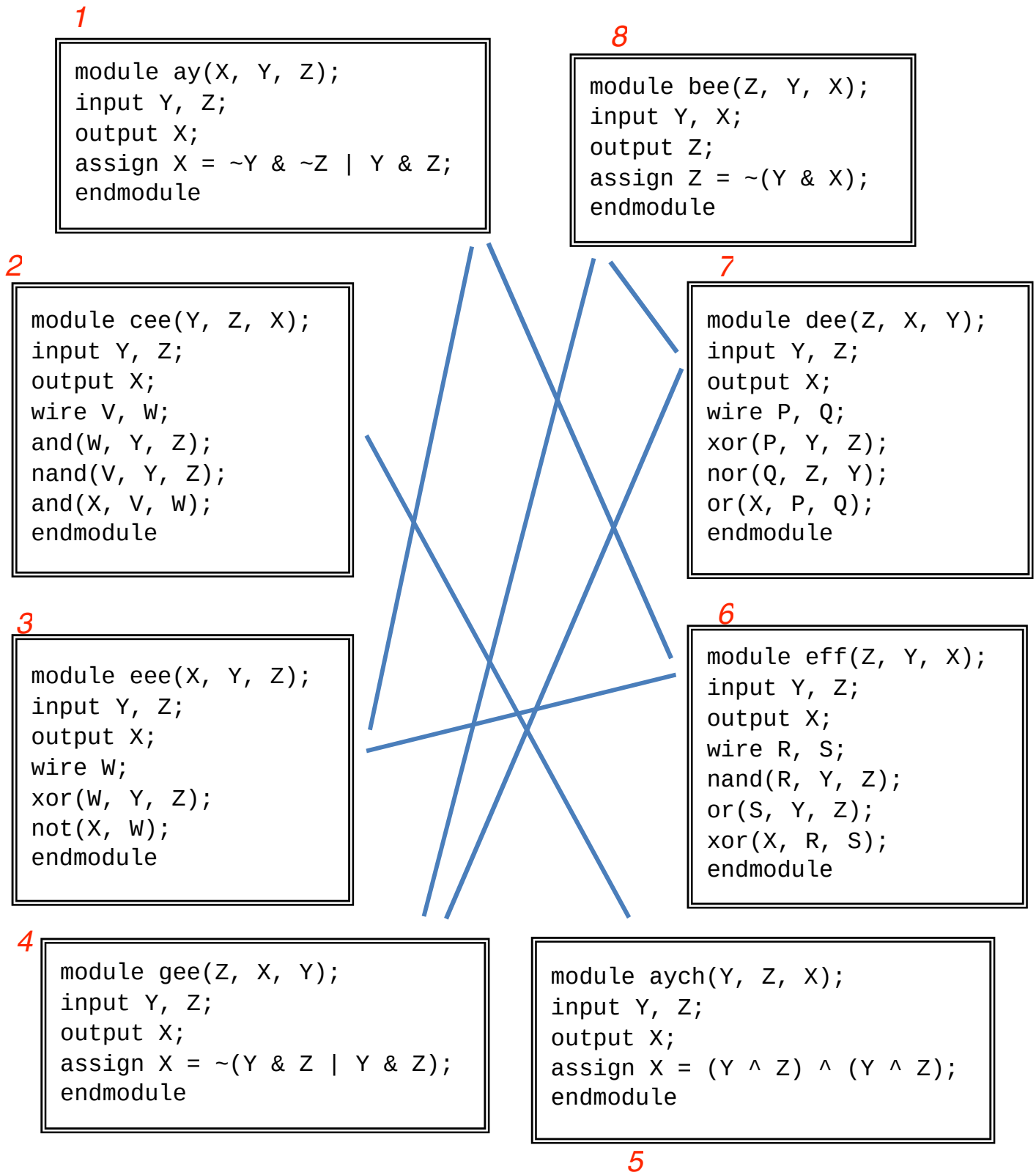
9. What do the letters MOS stand for in the term MOSFET? **(1 mark)**

Metal oxide semiconductor

Part B: Slightly Longer Answer (24 marks)

Answer the following questions in the space provided. The final answer is all that is necessary, but showing your work can help if your final answer isn't correct. Again, make sure to write legibly here.

1. Draw lines to connect the Verilog modules that have equivalent behaviour. **(16 marks)**



1

```
module ay(X, Y, Z);
input Y, Z;
output X;
assign X = ~Y & ~Z | Y & Z;
endmodule
```

8

```
module bee(Z, Y, X);
input Y, X;
output Z;
assign Z = ~(Y & X);
endmodule
```

2

```
module cee(Y, Z, X);
input Y, Z;
output X;
wire V, W;
and(W, Y, Z);
nand(V, Y, Z);
and(X, V, W);
endmodule
```

7

```
module dee(Z, X, Y);
input Y, Z;
output X;
wire P, Q;
xor(P, Y, Z);
nor(Q, Z, Y);
or(X, P, Q);
endmodule
```

3

```
module eee(X, Y, Z);
input Y, Z;
output X;
wire W;
xor(W, Y, Z);
not(X, W);
endmodule
```

6

```
module eff(Z, Y, X);
input Y, Z;
output X;
wire R, S;
nand(R, Y, Z);
or(S, Y, Z);
xor(X, R, S);
endmodule
```

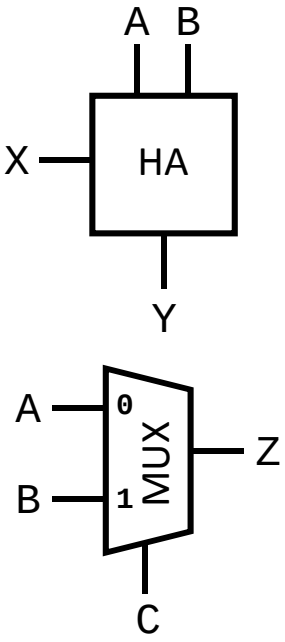
4

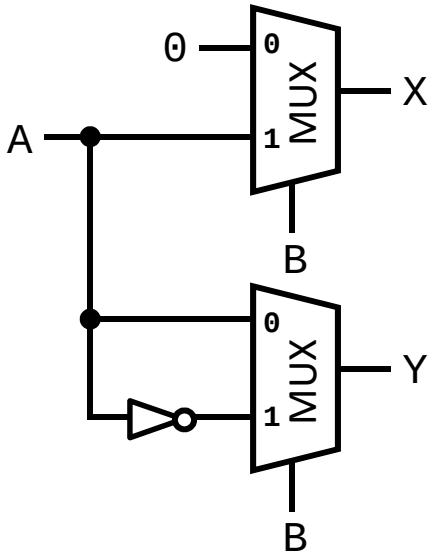
```
module gee(Z, X, Y);
input Y, Z;
output X;
assign X = ~(Y & Z | Y & Z);
endmodule
```

```
module aych(Y, Z, X);
input Y, Z;
output X;
assign X = (Y ^ Z) ^ (Y ^ Z);
endmodule
```

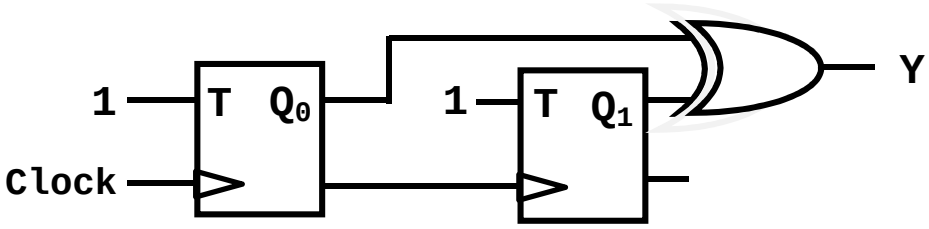
5

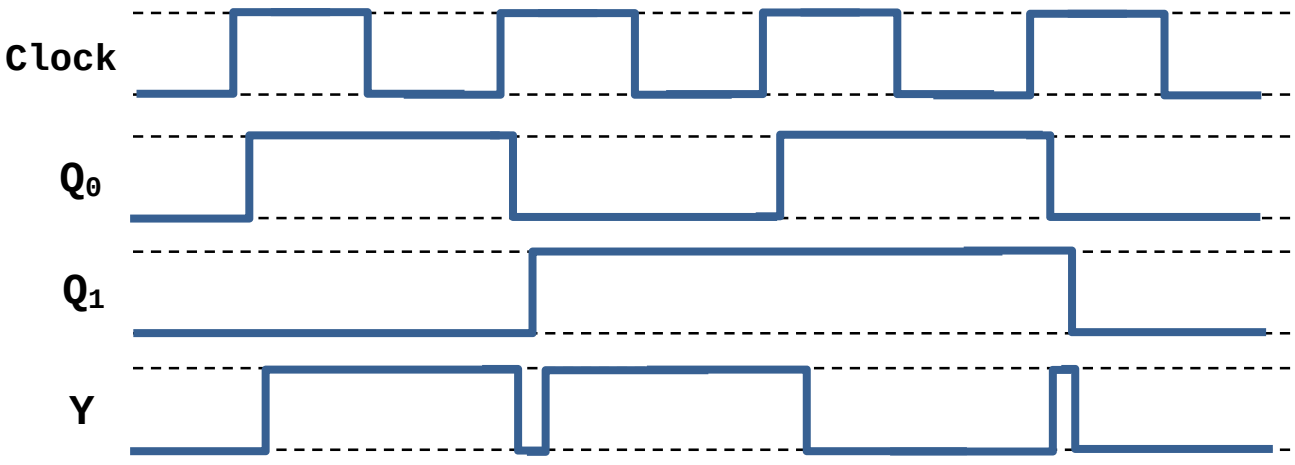
2. Consider the half adder and the multiplexer on the right. In the space below, draw a diagram that implements the half adder device using only multiplexers and NOT gates. For full marks, use the fewest muxes possible. **(4 marks)**





3. In the waveform diagram below, show what the waveform looks like for the signals in the flip-flop circuit below. Assume that Q_0 and Q_1 each start with initial values of 0. **(4 marks)**





Part C: Circuit Design and Analysis (9 marks)

1. Consider the Karnaugh map below. On the right-hand side, list the minterms that cause high output behaviour in the circuit, using the minterm notation shown in class. **(3 marks)**

	$\overline{C}\cdot\overline{D}$	$\overline{C}\cdot D$	$C\cdot D$	$C\cdot\overline{D}$
$\overline{A}\cdot\overline{B}$	1	0	X	1
$\overline{A}\cdot B$	0	X	0	X
$A\cdot B$	1	X	0	0
$A\cdot\overline{B}$	1	1	X	1

Minterms:

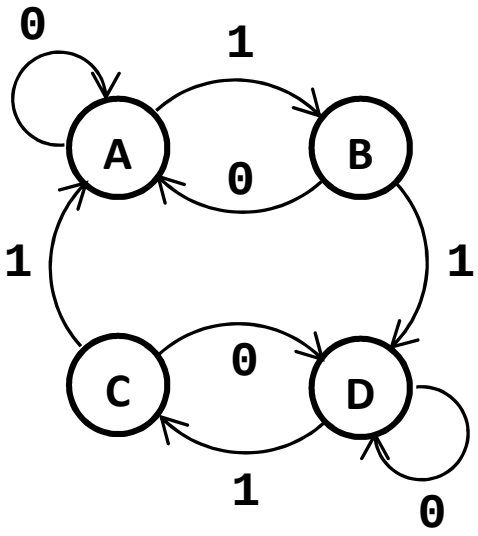
$$m_0 + m_2 + m_8 + m_9 + m_{10} + m_{12}$$

2. Group terms in the Karnaugh map above that will result in a circuit with the lowest gate cost. Write the most reduced equivalent boolean expression in the space below. **(4 marks)**

$$\overline{B}\cdot\overline{D} + A\cdot\overline{C}$$

3. Consider the state diagram on the right. Given this diagram, which of the following flip-flop assignments on the left provide safe state transitions? Circle all that qualify. **(2 marks)**

	State			
	A	**B**	**C**	**D**
Assignment #1	00	01	10	11
Assignment #2	00	01	11	10
Assignment #3	00	11	10	01
Assignment #4	00	10	10	11



Part D: Verilog (14 marks)

Consider the piece of Verilog code on the right.

```
module midterm (a, b, c, d, e);
  input [1:0] a;
  input [1:0] b;
  output c, d, e;

  wire x;

  assign x = a[1] & b[1];
  assign c = a[1] & ~b[1] |
                x & a[0] & ~b[0];
  assign d = a[0] & b[0] &
                a[1] & b[1];
  assign e = ~a[1] & b[1] |
                x & ~a[0] & b[0];

endmodule
```

1. What does this piece of code do? **(4 marks)**

A comparator circuit
(minus a case)

2. What functions do the output signals c , d and e perform here? **(2 marks)**

C: a > b

D: a = b

E: a < b

3. In the space below, provide Verilog code that implements a 32-bit parallel load register. For full marks, this register should update its output on the **positive clock edge**, and have an **asynchronous negative clear**. For full marks, you ***must*** use an `always` block to implement the main functionality of your design. The module has been started for you below. **(8 marks total)**

```
module 32bit_register (data, enable, q, clock, clear);

   input enable, clock, clear;
   input [31:0] data;
   output reg [31:0] q;

   always @ (posedge clock or negedge clear)
      if (~clear)
         q <= 0;
      else if (enable)
         q <= data;
   endmodule
```

Bonus Question: ***What are the names of the TAs in your lab?***
(1 mark)

_____

_____

The rest of this page is left blank intentionally for answer overflows.

Please enter your first and last name in the space below. Do NOT write your student number here.

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