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STUDENT NUMBER: 1003326046

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EXAM REPRODUCTION

UNIVERSITY OF TORONTO
Faculty of Arts & Science

DECEMBER 2018 EXAMINATIONS

CSC258H1F

Duration: 3 hours

Aids Allowed: 1 ruler, 1 highlighter

Exam Reminders:

- Fill out your name and student number on the top of this page and at the bottom of subsequent pages.
- Do not begin writing the actual exam until the announcements have ended and the Exam Facilitator has started the exam.
- As a student, you help create a fair and inclusive writing environment. If you possess an unauthorized aid during an exam, you may be charged with an academic offence.
- Turn off and place all cell phones, smart watches, electronic devices, and unauthorized study materials in your bag under your desk. If it is left in your pocket, it may be an academic offence.
- When you are done your exam, raise your hand for someone to come and collect your exam. Do not collect your bag and jacket before your exam is handed in.
- If you are feeling ill and unable to finish your exam, please bring it to the attention of an Exam Facilitator so it can be recorded before leaving the exam hall.
- In the event of a fire alarm, do not check your cell phone when escorted outside.

Special Instructions:

- There are 6 questions on 14 pages, plus a bonus question. When you hear the signal to start, make sure that your exam is complete before you begin.
- Read over the entire exam before starting.
- If you use any space for rough work or have to user the overflow page, clearly indicate the section(s) that you want marked.

Exam Format and Grading Scheme:

Part A: 35 / 19	Part B: 5 / 25	Part C: 19 / 22	Part D: 34 / 39
Part E: 6 / 14	Part F: 14 / 24	Bonus: 1 / 1	Total: 92.5 / 143

Students must hand in all examination materials at the end

Part A: Short Answer (19 marks)

Answer the following questions in the space provided. When providing a written answer, write **as clearly and legibly as possible**. Marks will not be awarded to unreadable answers.

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1. How many bytes can be stored in a memory unit that uses 8 address bits and a 32-bit architecture? **(2 marks)**

B 2

$2^8 \times 4 = 2^{10}$

a) 256 **b)** 1024

c) 2048 **d)** 8192

2. How many address bits are needed to specify the location of an integer in a 1024 bit memory unit, given a 64-bit architecture? **(2 marks)**

A 2 8

$2^x \cdot 2^3 = 2^{7}$ bytes

a) 4 **b)** 8

c) 10 **d)** 16

3. Which of the following are inputs to the VGA adapter in Lab 7? **(2 marks)**

ABC 0.5

a) colour **b)** CLOCK_50

c) write **d)** resetn

4. True or False? Multiplication with Booth's Algorithm uses the same number of clock cycles as multiplication with an accumulator circuit. **(1 mark)**

False 0

True **False**

5. Which of the following assembly instructions use the processor's sign extend unit? Circle all that apply. **(2 marks)**

BCD 2

I

~~**a)** jal~~ **b)** bne

c) lb **d)** xori

6. If the Verilog statement {C, A} = A * B performs multiplication on the binary numbers A, B and C without losing any bits, which of the following must be true? **(2 marks)**

D 2

a) C has more bits than B **b)** C has fewer bits than B

c) C has the same number of bits as B **d)** More than one of the above

8.5

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7. Which of the following is the FPGA that we use in the DE1 labs? **(1 mark)**

C 0

a) Cyclone II
b) Cyclone III
c) Cyclone IV
d) Cyclone V

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8. Which is the chip that is used for this FPGA in the labs? **(1 mark)**

D 1

a) 5CSEMA6F31C6
~~b) 5CSEMA6F31C5~~
~~c) 5CSEMA5F31C5~~
d) 5CSEMA5F31C6

9. True or False? Interrupts are polled on a MIPS architecture. **(1 mark)**

1

True **False**

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10. Rank the following interrupts, from 1 (highest priority) to 4 (lowest priority). **(2 marks)**

0

Arithmetic overflow exception ___2___ **External interrupt** ___3___

Address error exception ___1___ **Breakpoint exception** ___4___

11. What is the maximum distance that a program counter can traverse in memory, as a result of a jump instruction? **(1 mark)**

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1 D

a) 2^{16} bytes
b) 2^{18} bytes
c) 2^{26} bytes
d) 2^{28} bytes

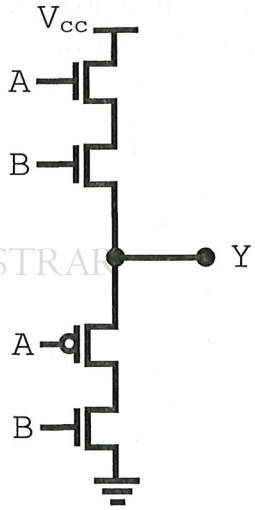
$2^{26} \cdot 4$

R
I
J

12. What is the gate that is implemented by the transistor diagram below? **(2 marks)**

tri – buffer

2



5

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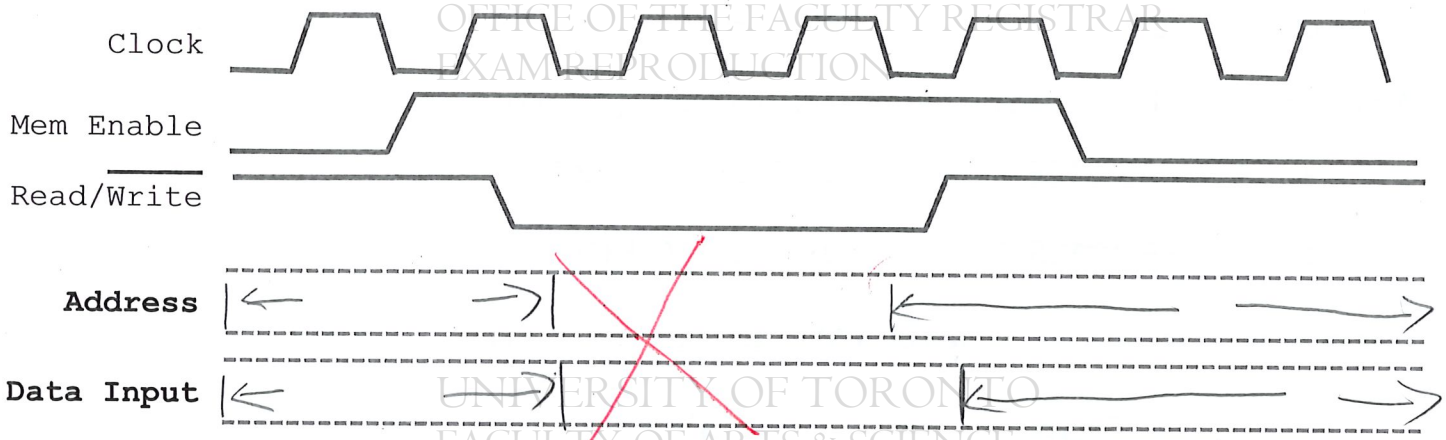
5/25 2 Tsu Tsd Thd T_{AW}

Part B: Design and Analysis (25 marks)

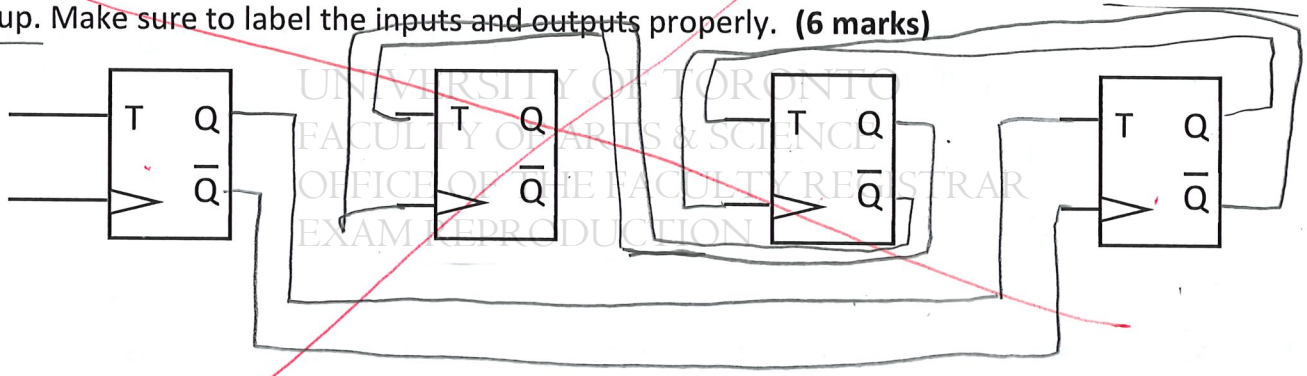
1. In the memory write diagram below, label the regions in the address and data input where those signals have valid values **(4 marks)**. On the same diagram, label the Setup Address Time and the Hold Data Time, and describe the reasons for these delays in the spaces provided. **(4 marks)**



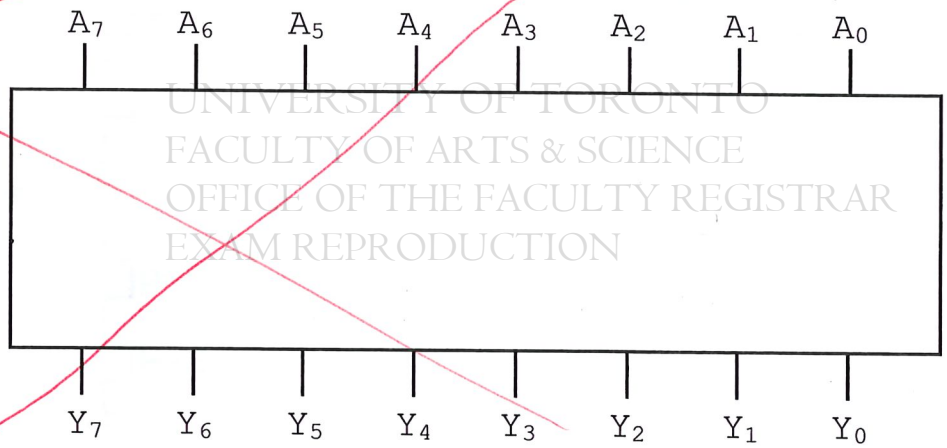
2

Label these on diagram & describe		
	Setup Address Time	exist time to setup address before write
	Hold Data Time	exist time to hold data high after write ends

2. Using the flip-flops shown below, design a ripple counter diagram that counts down instead of up. Make sure to label the inputs and outputs properly. **(6 marks)**



3. In the diagram below, fill in the circuitry for an 8-bit shift-by-two circuit, like those found in the processor datapath. For full marks, use the fewest gates possible. **(3 marks)**



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(continued)

$(\neg B \wedge \neg C) \vee (\neg C \wedge B)$ 3/8

4. For each of the circuits below, circle the ones that will compile without errors. **(4 marks)**
For circuits that do compile, draw lines between the ones with the same behaviour. **(4 marks)**

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```
module final(A, B, C);
input [1:0] B, C;
output [1:0] A;
assign A = ~B & ~C | ~C & B;
endmodule
```

B	C	A
0	0	0
0	1	1
1	0	0
1	1	0

```
module final(A, B, C);
input [1:0] B, C;
output [1:0] A;
assign A = B ^ C;
endmodule
```

```
module final(A, B, C);
input [1:0] B, [1:0] C;
output [1:0] A;
wire W;
xor(W, B, C);
not(A, W);
endmodule
```

B	C	A
0	0	1
0	1	0

−4

```
module final(A, B, C);
input B[1:0], A[1:0];
output C[1:0];
wire R, S;
nand(R, B, A);
or(S, B, A);
xor(C, R, S);
endmodule
```

A	B	C
0	0	1
0	1	0
1	0	0

```
module final(A, B, C);
input [1:0] B, A;
output [1:0] C;
wire R, S;
nand(R, B, A);
or(S, B, A);
xor(C, R, S);
endmodule
```

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

```
module final(A, B, C);
input [1:0] B, C;
output [1:0] A;
reg W;
xor(W, B, C);
not(A, W);
endmodule
```

−0.5

B	C	A
0	0	0
0	1	0
1	0	0
1	1	1

```
module final(A, B, C);
input [1:0] B, C;
output [1:0] A;
assign A = B & ~C | ~B & C;
endmodule
```

$(B \wedge \neg C) \vee (\neg B \wedge C)$

B	C	A
0	0	0
0	1	1
1	0	1
1	1	0

```
module final(A, B, C);
input [1:0] B, C;
output [1:0] A;
A <= B ^ C;
endmodule
```

−0.5

B	C	A
0	0	0
0	1	1
1	0	1
1	1	1

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(continued)

10/10 A = 1011 B = 1001 → 0110 → 0111 0100 → 0101 → -5

Part C: Processors (22 marks)

$2^3+2^1+2^0 = 4+2+1 = 7$

1. When Booth's Algorithm is performed on the binary inputs ~~A=1101~~ and ~~B=1011~~, the values for A and P change at each step of the algorithm. The framework is provided below, with a few values filled in for you. Fill in the rest, according to the steps shown in class. **(10 marks)** -7 35

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Initial Values: A= 10110 B= 1001 -B= 0111 1

Step #1:

A = 10110 **Initial P value =** 0000 0000

New P value = 0111 0000

1
P 0000 0000
-B 0111
P 0111 0000
A = 11011
P = 0011 1000

Step #2:

A = 11011 **Initial P value =** 0011 1000

New P value = 0011 1000

2 do nothing
A = 11101
P = 0001 1100
5

Step #3:

A = 11101 **Initial P value =** 0001 1100

New P value = 1010 1100

3
P 0001 1100
+B 1001
P 1010 1100
A = 11110
P = 1101 0110

Step #4:

A = 11110 **Initial P value =** 1101 0110

New P value = 0100 0110

4
P 1101 0110
-B 0111
P 0100 0110
P = 0010 0011
$2^5+2^1+2^0 = 32+2+1$

Final P value (binary) = 0010 0011 **Final P value (decimal) =** 35 2

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(continued)

R | opcode | rs | rt | rd | shamt | funct | I | op | rs | rt | imm... | J | op | label |

2. Consider the datapaths below. For each of the following operations, highlight the path that the data needs to take from start to finish. **(12 marks)**

9

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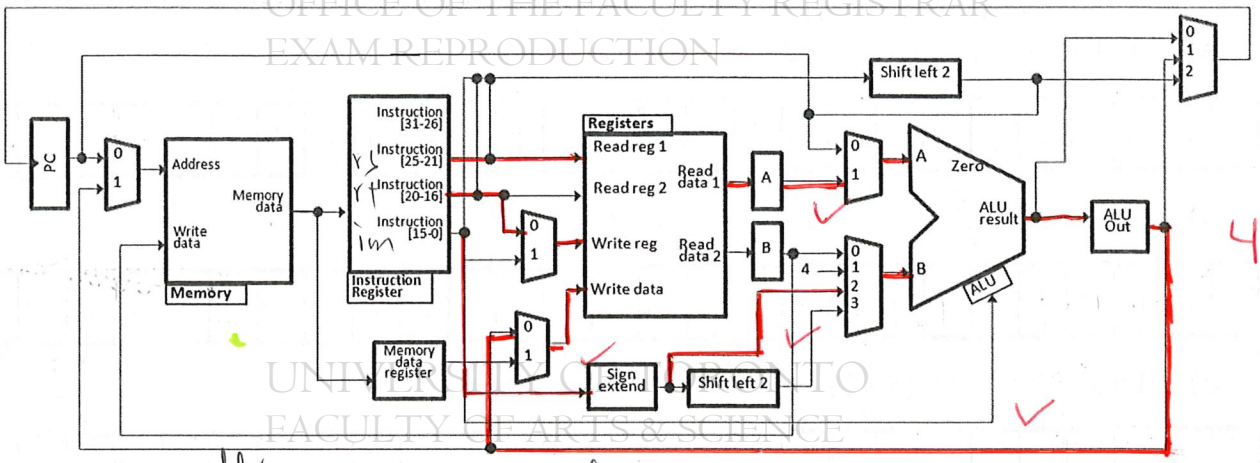
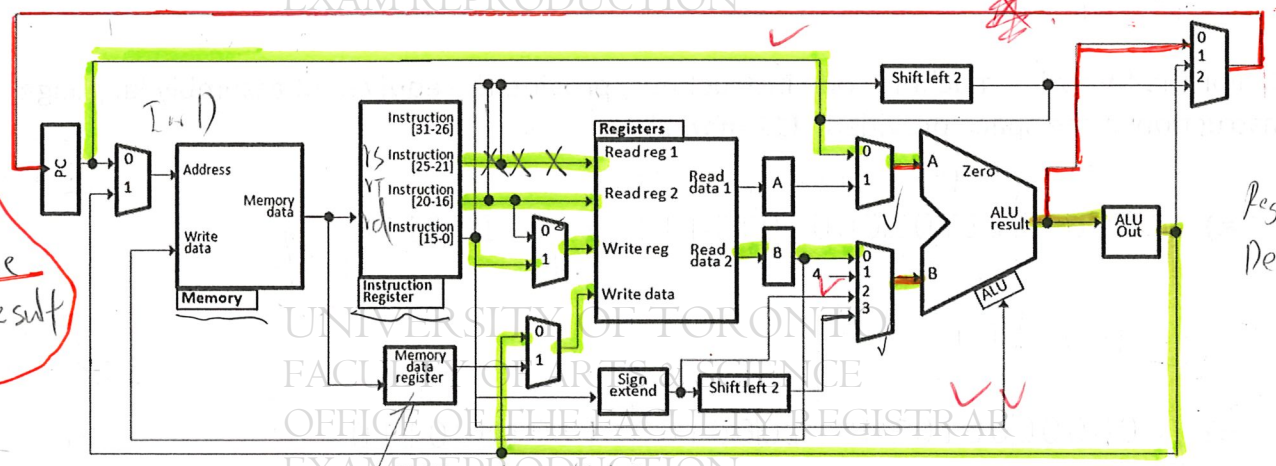
a) Set register $t0 to 100 addi $t $s i ← 100 rt = rs + i



4

b) Store the program counter in $ra addr add $ra $zero

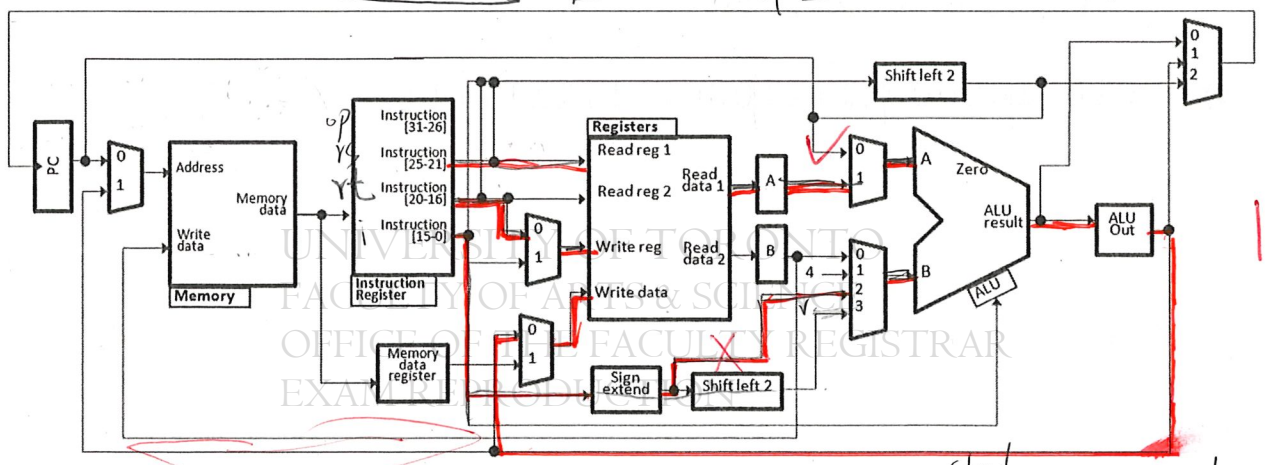


4

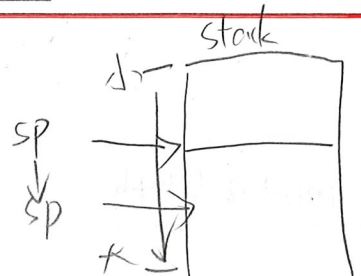
Register Destination

#please ignore red line
#green line is final result

c) Pop the top element from the stack and store it in $a0 I rt = i($sp)



1



pop : lw
sp = sp+4

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(continued)

Part D: Processor Instructions (39 marks)

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1. For the following assembly language instructions, write the equivalent machine code instruction in the space provided. You might find the reference information in the appendix helpful for this question. Fill in the space with an X if the value doesn't matter. **(12 marks)**

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01000 01001 01010

a) `sllv $t0, $t1, $t2` R | opcode | rs | rt | rd | shamt | funct | 4

d t s

0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0	0	X	X	X	X	X	0	0	0	1	0	0

6 5 5 5 5 6

b) `jr $ra` R syntax $s 3

0	0	0	0	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0

c) `lhu $t0, 15($s0)` I | opcode | rs | rt | im | 4

t s

1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

10000 $2^4 = 16$

2. For the following machine code instructions, provide the equivalent assembly language instruction in the space provided. **(12 marks)**

op rs rt im

a) 100011|11101|00010|1111111111111111 4

29 2 −1

lw $v0, −1($sp)

$2^3+2^2+2^1+2^0$
$8+4+2+1 = 15$

rs rt rd shamt funct

b) 000000|00101|00110|00100|11101|000110 4

$2^4+2^3+2^1+2^1$
$16+8+4+2 = 30$

srlv $a0, $a2, $a1

0 31 12 10 9 8 7 6 5 4 3 2 1

c) 001001|00000|11111|0001011111111111 2

op rs rt im

addiu $ra, $zero, $2^{12}+2^{10}+2^9+2^8+2^7+2^6+2^5+2^4+2^3+2^2+2^1$

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(continued)

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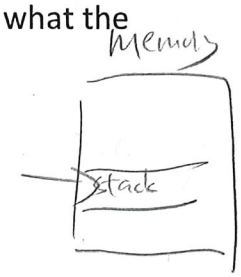
3. For each of the processor tasks below, indicate what the values of the following control unit signals will be by filling in the boxes next to each signal with the signal values. **(15 marks)**

- If a control signal doesn't affect the operation, fill in its value with an X.
- For ALUOp, full marks will only be given for binary values. If you don't know what the values are, just write what kind of operation is taking place instead.



sp address addr

Add 100 to the stack pointer address. 4

PCWrite	0	PCWriteCond	0	IorD	X	MemRead	0	MemWrite	0
MemToReg	0	IRWrite	0	PCSource	X	ALUOp	001		
ALUSrcA	1	ALUSrcB	11	RegWrite	1	RegDst	1		

addr ra

Store the address of the current instruction in the return address register. 4.5

PCWrite	0	PCWriteCond	0	IorD	X	MemRead	0	MemWrite	0
MemToReg	0	IRWrite	0	PCSource	X	ALUOp	001		
ALUSrcA	0	ALUSrcB	00	RegWrite	1	RegDst	1		

sw t, i(s) I opcode rs rt i 4.5

Jump to the newly-calculated $ra (from previous part) if $t0 is equal to zero.

PCWrite	0	PCWriteCond	1	IorD	X	MemRead	0	MemWrite	0
MemToReg	X	IRWrite	0	PCSource	00	ALUOp	010		
ALUSrcA	1	ALUSrcB	00	RegWrite	0	RegDst	X		

I beq rs rt label

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Part E: Verilog (14 marks)

Consider the piece of Verilog code on the right.

```
module final (A, B, M, Clock);

input [31:0] m;
input w;
output reg [5:0] o;
output reg [4:0] s, t, d;
output reg [15:0] i;
reg [31:0] c;

always @ (*)
  begin
    if (w)  c <= m;
    o <= c[31:26];
    s <= c[25:21];
    t <= c[20:16];
    d <= c[15:11];
    i <= c[15:0];
  end
endmodule
```

1. In a sentence or less, describe what operation this code performs. **(4 marks)**

write to Instruction Register

2. Based on your answer above, what do the `i` and `o` reg values represent? **(2 marks)**

i: immediate

o: opcode

3. In the space below, complete the short Verilog module called `register_unit`, that implements the **register unit** from the processor datapath. **(8 marks)**

```
module register_unit (reg_write, read_reg1, read_reg2,
        write_reg, write_data, read_data1, read_data2);
input reg_write
end module
```

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Part F: Assembly Language (24 marks)

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1. In the spaces provided below, write the assembly language instruction(s) that perform the following tasks. Full marks will only be given for one-instruction answers. **(12 marks total)**

a) Set the value stored in `$s0` to one eighth of its original value. **(3 marks)**

~~sr~~ $s0, $s0, 3

sra

3
+ 3.5
6.5

b) Invert all the bits of the value stored in `$a0`. **(3 marks)**

nor

nor $a0, $a0, $zero

c) Pop a character off the stack and store it in `$t0`. **(3 marks)**

~~lb~~ $t0, 0($sp)

lbu

d) Set the program counter to zero. **(3 marks)**

~~lw~~ $pc, 0($zero)

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2. In the space provided, describe the overall result of each assembly program. **(12 marks)**

```
            .data
len:        .word     5
list:       .word     -4, -1, 0, 1, 4
            .text
main:       la ~~addi~~ $s0, ~~$zero,~~ list
            la ~~add~~ $s1, ~~$zero,~~ len
            lw $t1, 0($s1)
top:        lw $t0, 0($s0)
            add $t0, $t0, $t0
            sw $t0, 0($s0)
            addi $t1, $t1, -1
            addi $s0, $s0, 4
            bne $t1, $zero, top
end:        jr $ra
```

double the element value in list

```
            .data
len:        .word     5
list:       .word     -4, -1, 0, 1, 4
            .text
main:       la ~~addi~~ $s0, $zero, list
            la ~~add~~ $s1, $zero, len
            lw $t1, 0($s1)
top:        lw $t0, 0($s0)
            sub $t0, $t0, $t0
            sw $t0, 0($s0)
            addi $t1, $t1, -1
            addi $s0, $s0, 4
            bne $t0, $zero, top
end:        jr $ra
```

set first element as 0

```
            .data
len:        .word     5
list:       .word     -4, -1, 0, 1, 4
            .text
main:       la ~~addi~~ $s0, $zero, list
            la ~~add~~ $s1, $zero, len
            lw $t1, 0($s1)
top:        lw $t0, 0($s0)
            addi $t1, $t1, -1
            addi $s0, $s0, 4
            add $t0, $t0, $t0
            sw $t0, 0($s0)
            bne $t1, $zero, top
end:        jr $ra
```

set the list to [-4, -8, -16, -32, -64, -128]

```
            .data
len:        .word     5
list:       .word     -4, -1, 0, 1, 4
            .text
main:       la ~~addi~~ $s0, $zero, list
            la ~~add~~ $s1, $zero, len
            lw $t1, 0($s1)
            lw $t0, 0($s0)
top:        addi $t1, $t1, -1
            add $t0, $t0, $t1
            bne $t1, $zero, top
            addi $s0, $s0, 4
            sw $t0, 0($s0)
end:        jr $zero
```

set second element in list to 6

-1.5

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(continued)

Reference Information

ALU Arithmetic Input Table:

Select		Input	Operation	
S_1	S_0	Y	C_{in}=0	C_{in}=1
0	0	All 0s	G=A	G=A+1
0	1	B	G=A+B	G=A+B+1
1	0	B	G=A-B-1	G=A-B
1	1	All 1s	G=A-1	G=A

Register assignments:

Register values : Processor role

- Register 0 ($zero): reserved value.
- Register 1 ($at): reserved for the assembler.
- Registers 2-3 ($v0, $v1): return values
- Registers 4-7 ($a0-$a3): function arguments
- Registers 8-15, 24-25 ($t0-$t9): temporaries
- Registers 16-23 ($s0-$s7): saved temporaries
- Registers 28-31 ($gp, $sp, $fp, $ra)

Bonus Question:

If CSC258 was a holiday dessert, what would it look like? Draw your answer in the space provided below. **(1 mark)**

ice cream which always keep me calm

Assembly Instruction Table:

Instruction	Type	Op/Func	Syntax
add	R	100000	$d, $s, $t
addu	R	100001	$d, $s, $t
addi	I	001000	$t, $s, i
addiu	I	001001	$t, $s, i
div	R	011010	$s, $t
divu	R	011011	$s, $t
mult	R	011000	$s, $t
multu	R	011001	$s, $t
sub	R	100010	$d, $s, $t
subu	R	100011	$d, $s, $t
and	R	100100	$d, $s, $t
andi	I	001100	$t, $s, i
nor	R	100111	$d, $s, $t
or	R	100101	$d, $s, $t
ori	I	001101	$t, $s, i
xor	R	100110	$d, $s, $t
xori	I	001110	$t, $s, i
sll	R	000000	$d, $t, a
sllv	R	000100	$d, $t, $s
sra	R	000011	$d, $t, a
srav	R	000111	$d, $t, $s
srl	R	000010	$d, $t, a
srlv	R	000110	$d, $t, $s
beq	I	000100	$s, $t, label
bgtz	I	000111	$s, label
blez	I	000110	$s, label
bne	I	000101	$s, $t, label
j	J	000010	label
jal	J	000011	label
jalr	R	001001	$s
jr	R	001000	$s
lb	I	100000	$t, i ($s)
lbu	I	100100	$t, i ($s)
lh	I	100001	$t, i ($s)
lhu	I	100101	$t, i ($s)
lw	I	100011	$t, i ($s)
sb	I	101000	$t, i ($s)
sh	I	101001	$t, i ($s)
sw	I	101011	$t, i ($s)
slt	R	101010	$d, $s, $t
sltu	R	101001	$d, $s, $t
slti	I	001010	$t, $s, i
sltiu	I	001011	$t, $s, i
mfhi	R	010000	$d
mflo	R	010010	$d
trap	I	001100	i

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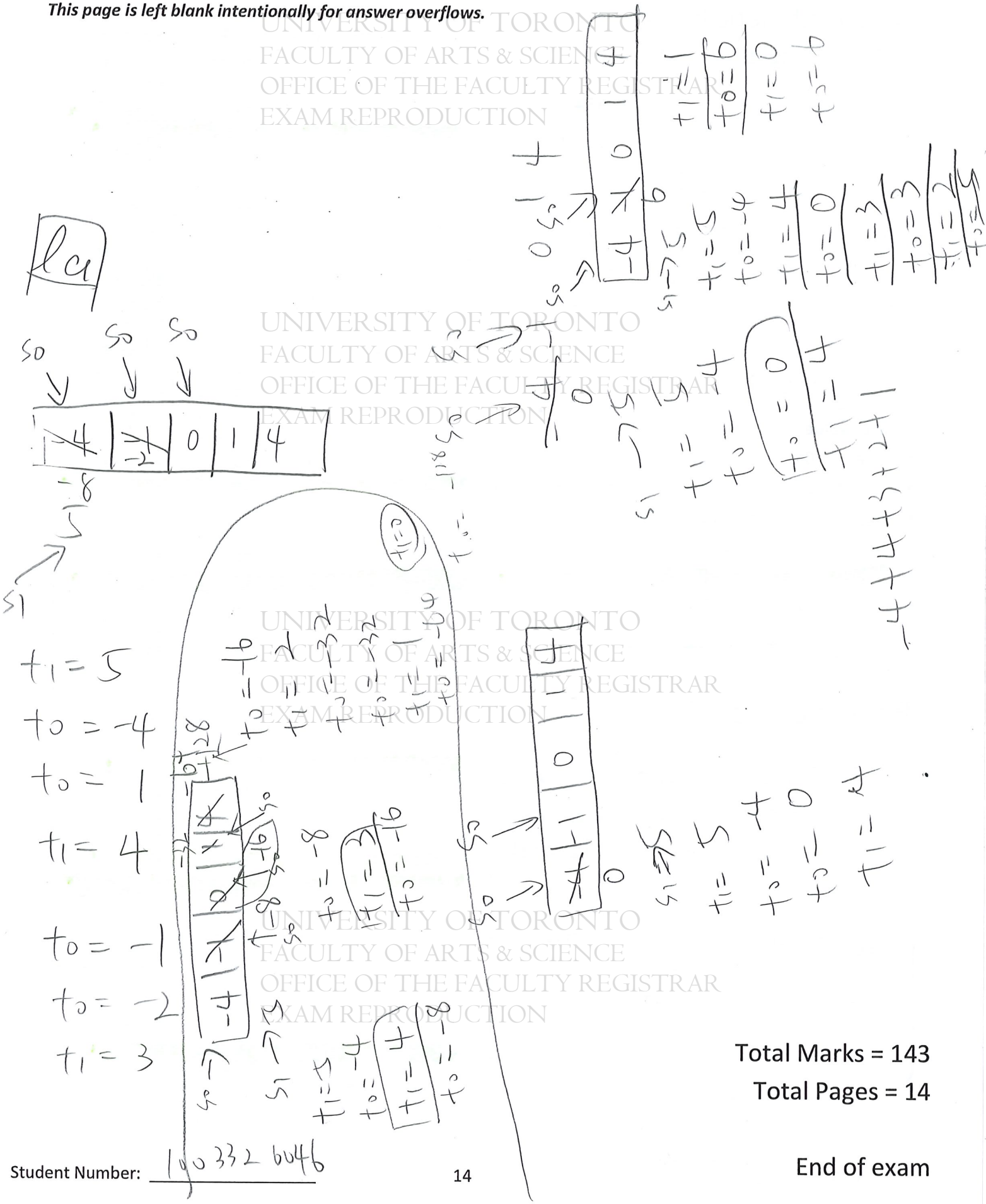
1a



Total Marks = 143

Total Pages = 14

End of exam

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