

[<c219ec5f>] security_sk_free+0xf/0x2g
[<c2451efb>] __sk_free+0x9b/0x120
[<c25ae7c1>] ? _raw_spin_unlock_irqres
[<c2451ffd>] sk_free+0x1d/0x30
[<c24f1024>] unix_release_sock+0x174/g

Popcorn Compiler Internals 101: The Gory Details





Goals

- Understand the design & flow of the Popcorn compiler at a high level
- Peel back the covers on LLVM internals & Popcornspecific modifications
 - Architecture-agnostic middle-end (LLVM intermediate representation)
 - Architecture-specific back-end (target-specific machine code)
- Dig into runtime stack transformation
 - How compiler-generated metadata is stored & used at runtime
 - How migration is invoked on the source node
 - How execution resumes on the destination node





What we won't cover

- Traditional compiler topics
 - The language frontend or language parsing
 - Instruction selection or scheduling
 - Target-agnostic/specific optimizations
 - Will cover topics necessary for understanding the Popcorn compiler
- The internals of Popcorn Linux's kernel
- Performance of the system
- Benefits of migration (the hard research stuff)
 - When to migrate (performance, energy, security)
 - Where to migrate





50,000 foot view of Popcorn Linux & its compiler





Popcorn Linux

- Goal transparently execute compiled, sharedmemory C/C++ applications across physically distinct, heterogeneous-ISA systems
- Developers take advantage of scalability & heterogeneity with no code modifications!



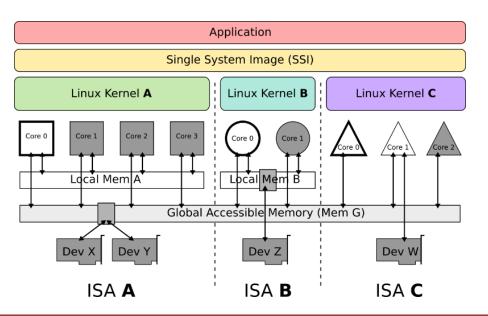






Popcorn Linux

- Multiple kernels provides single system image (SSI)
 allowing threads to migrate freely between nodes*
 - Thread migration stop & resume thread on new node
 - Data migration transfer data pages between nodes on-demand



*Antonio Barbalace, Robert Lyerly, Christopher Jelesnianski, Anthony Carno, Ho-Ren Chuang, Vincent Legout, and Binoy Ravindran.
2017. Breaking the Boundaries in Heterogeneous-ISA Datacenters. In Proceedings of the Twenty-Second International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '17).





Popcorn Linux

- Threads invoke the kernel's migration service through userland syscalls
 - Can't migrate arbitrarily, only at migration points (details later)
- Kernels migrate data on-demand through the pagefault mechanism
 - Compiler/runtime need to ensure memory accesses observed by kernel are semantically equivalent across all architectures, i.e., pointers reference the same thing and are accessed the same way on all architectures

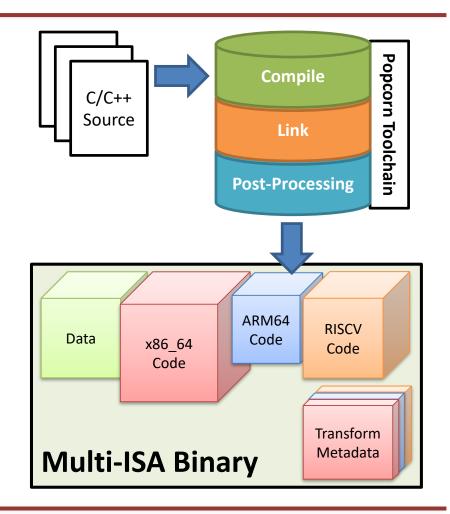
99% of the compiler implementation is aimed at satisfying this requirement!





Popcorn Compiler Toolchain

- Compiler toolchain builds multi-ISA binaries
 - Create mostly-common virtual address space (data, code, heap)
 - Pointers are valid across all ISAs
 - Dynamically transform thread execution state (stack, registers) between ISA-specific formats at migration time
 - Transform pointers to be valid
 - Instrument generated code with migration points

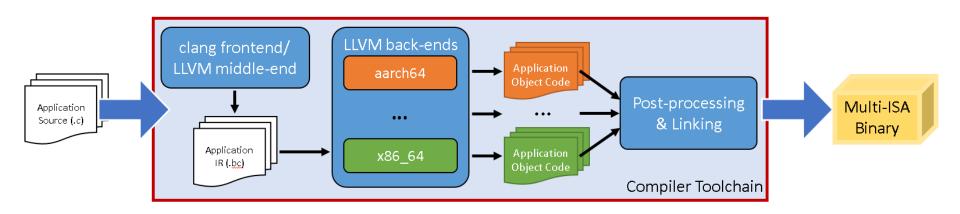






Popcorn Compiler Toolchain

- Built on top of clang/LLVM
 - clang/LLVM 3.7.1, GNU gold 2.27, musl-libc 1.1.18
 - Custom address space alignment, post-processing tools
 - State transformation/migration libraries

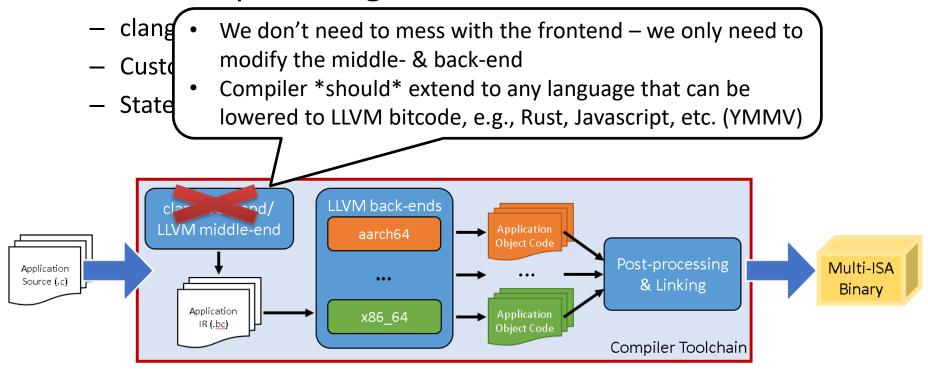






Popcorn Compiler Toolchain

Built on top of clang/LLVM







Assumptions

- The ISAs have the following characteristics
 - 64-bit address space, meaning pointers are 64 bits
 - Little-endian data format
 - Some RISC architectures can switch between endianness formats, e.g., ARM64 & POWER8
 - Could potentially be relaxed for code, e.g., SPARCv9 allows little-endian data but requires big-endian code
 - Primitive data types have the same sizes & alignments
 - Characters 8 bits, shorts 16 bits, integers/longs 32 bits
 - Long longs/pointers 64 bits
 - Single precision floating point 32 bits, double 64 bits (IEEE format)
- Applications are statically linked, no dynamic libraries





Assumptions

- The ISAs have the following characteristics
 - 64-bit address space, meaning pointers are 64 bits
 - Little-endian data format
 - Some RISC architect ARM64 & POWER8
 - Could potentially be data but requires big-enuis

e.g., Forces compiler to lay out all data, i.e., primitives, arrays, structs/objects, in the same format across all architectures

- Primitive data types have the same sizes & alignments
 - Characters 8 bits, shorts 16 bits, integers/longs 32 bits
 - Long longs/pointers 64 bits
 - Single precision floating point 32 bits, double 64 bits (IEEE format)
- Applications are statically linked, no dynamic libraries





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Limitations

- No inline assembly opaque to liveness analysis in middle-/back-end
- No architecture-specific extensions
 - E.g., crypto instructions, ISA-specific SIMD, etc.

- Note: by limitations, we mean you cannot have state created by these limitations live during migration – stack transformation can't handle it!
 - E.g., you cannot have live data in SIMD registers during migration





Part 1: A day in the life of an LLVM compilation





Part 1: A day in the life of an LLVM compilation

All source & log files are available in the "vanilla-compile" folder





```
$ clang -02 -c hello.c
$ ls
hello.c hello.o
```





What's actually happening on the inside? clang/LLVM are designed to be very modular – let's break it down...

```
$ clang -02 -c hello.c
$ ls
hello.c hello.o
```





```
#include <stdio.h>
int main(int argc, char** argv)
{
   printf("Hello, world!\n");
   return 0;
}
```





clang -O2 -emit-llvm -S hello.c

```
#include <stdio.h>
int main(int argc, char** argv)
{
   printf("Hello, world!\n");
   return 0;
}
```





clang -02 -emit-llvm -S hello.c

```
#include <stdio.h>
int main(int argc, char** argv)
{
   printf("Hello, world!\n");
   return 0;
}
```

- -emit-llvm: lower C code to LLVM IR
- -S: emit in human-readable format





clang -O2 -emit-llvm -S hello.c

hello.ll

```
#include <stdio.h>
int main(int argc, char** argv)
{
   printf("Hello, world!\n");
   return 0;
}
```







- Bitcode is ISA-agnostic, but looks like low-level assembly
 - Conceptually, assembly for some virtual machine or virtual ISA (the "VM" in LLVM)
 - Program objects (functions, global data, etc.) have not been placed in the virtual address space
 - No stack frame particulars (e.g., return address location)
 - No registers or stack slots for program variables ("values" in LLVM)
- See the <u>language reference manual</u> for a detailed explanation of LLVM's IR





hello.ll

Layouts, sizes & alignments of primitive types, e.g., integers, floating-point





hello.ll

Target architecture/ABI





hello.ll

Global variable definition





hello.ll

Function definition





hello.ll

Function body in single-static assignment form (SSA), organized as a series of basic blocks containing operations

 Basic block: a sequence of non-control flow instructions terminated by control flow, e.g., branch or jump





hello.ll

declare i32 @puts(i8* nocapture readonly) #1

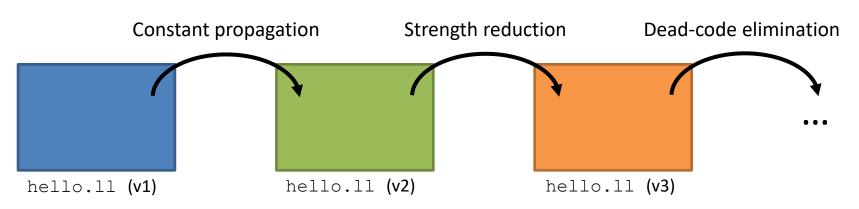
Function declaration – definition lives in another source file or "compilation module" in LLVM terminology





Optimizing LLVM IR

- The optimizer (opt) is LLVM's "middle-end"
 - Don't worry, clang includes these optimizations!
- LLVM applies a large number of target-agnostic optimizations to the IR
 - Optimizations structured as a series of *passes* run over the IR, which consume IR & produce (hopefully) optimized IR







Optimizing LLVM IR

- What is single static assignment?
 - Program variables are lowered to values which have the following characteristics:
 - Each value is assigned exactly once
 - Each value must be defined before its use
 - Once assigned, a value is immutable
 - Program variables assigned multiple times are lowered to distinct values (versioned) by the compiler
 - LLVM bitcode has no notion of a variable inside of functions only values!





Optimizing LLVM IR

- Why single static assignment?
 - Provides lots of useful information by construction
 - Explicit use-def chains of a value in a function
 - Liveness ranges for determining when a value is live inside a function
 - Enables many useful analyses & compiler optimizations
 - Instruction scheduling
 - Liveness analysis/register allocation
 - Tons of optimizations see Wikipedia for examples





- The system compiler (11c) is LLVM's back-end
 - Again, clang includes this too!
 - Implements the semantics of the IR using operations defined by the target's ISA
- LLVM implements code generation through its <u>target-independent code generator</u>
 - Another series of passes analyze and transform bitcode to assembly
 - Targets are "plugins" which describe opcodes, registers, ABIs, etc.
 - Most target-specific code lowering is implemented in a targetindependent manner!





- LLVM has a complex pattern-matching/graph-based framework for instruction selection & scheduling
 - The subject of several Ph.D. theses, not this tutorial
- The backend lowers bitcode into another type of IR, called machine code IR
 - Also in SSA, but very close to the target architecture









llc hello.ll





llc hello.ll

hello.s



```
.text
              .file
                            "hello.11"
              .qlobl
                            main
              .align
                            16, 0x90
              .type
                            main, @function
main:
                                           # @main
              .cfi startproc
# BB#0:
                                            # %entry
              pushq
                            %rax
.Ltmp0:
              .cfi def cfa offset 16
              movl
                            $.Lstr, %edi
              callq
                            puts
              xorl
                            %eax, %eax
                            %rdx
              popq
              retq
.Lfunc end0:
              .size
                            main, .Lfunc end0-main
              .cfi endproc
                            .Lstr,@object # @str
              .type
              .section
              .rodata.str1.1, "aMS", @progbits, 1
.Lstr:
              .asciz
                            "Hello, world!"
              .size
                            .Lstr, 14
```





llc hello.ll

hello.s

hello.ll

```
.text
              .file
                             "hello.ll"
              .qlobl
                            main
              .align
                            16, 0x90
              .type
                            main, @function
main:
                                            # @main
              .cfi startproc
# BB#0:
                                            # %entry
              pushq
                            %rax
.Ltmp0:
              .cfi def cfa offset 16
              movl
                             $.Lstr, %edi
              callq
                             puts
              xorl
                            %eax, %eax
                             %rdx
              popq
              retq
.Lfunc end0:
              .size
                            main, .Lfunc end0-main
              .cfi endproc
                             .Lstr,@object # @str
              .type
              .section
              .rodata.str1.1, "aMS", @progbits, 1
.Lstr:
              .asciz
                             "Hello, world!"
              .size
                             .Lstr, 14
```





llc -debug-only=regalloc hello.ll

```
****** MACHINEINSTRS ******
# Machine code for function main: Post SSA
0B
         BB#0: derived from LLVM BB %entry
16B
                   ADJCALLSTACKDOWN64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
32B
                    %vreq2<def> = MOV32ri64 <qa:@str>; GR32:%vreq2
                    %vreg3<def> = SUBREG TO REG 0, %vreg2, 4; GR64:%vreg3 GR32:%vreg2
48B
                    %RDI<def> = COPY %vreq3; GR64:%vreq3
64B
                    CALL64pcrel32 <ga:@puts>, <regmask>, %RSP<imp-use>, %RDI<imp-use,kill>,
80B
                             %RSP<imp-def>, %EAX<imp-def,dead>
96B
                   ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
112B
                    %vreq5<def> = MOV32r0 %EFLAGS<imp-def,dead>; GR32:%vreq5
128B
                    %EAX<def> = COPY %vreq5; GR32:%vreq5
                   RETO %EAX<kill>
144B
```





All values in middle-end which could *potentially* be held in a register are lowered to **virtual registers** (vregs)

- LLVM starts by assuming a virtual register set with unlimited registers
- Deciding which values are actually placed in registers and which are spilled to the stack is the purpose of the *register allocator*





llc -debug-only=regalloc hello.ll



***** MACHINEINSTRS ******



11c -debug-only=regalloc hello.ll

```
******** MACHINEINSTRS
# Machine code for funct
```

Operands are encoded as part of the instruction

 Registers, constants, references to other program objects (here, reference to the string literal "Hello, world!")





11c -debug-only=regalloc hello.ll

```
Physical registers appear prior to register allocation due to ABI calling conventions

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Physical registers appear prior to register allocation due to ABI calling conventions

Physical registers appear prior to register allocation due to ABI calling conventions

Physical registers appear prior to register allocation due to ABI calling conventions

Physical registers appear prior to registers; GR32:%vreg3

REDICAL PROPRIOR ARCHARGE AR
```



******* MACHINEINSTRS ******



Post-register allocation

```
# Machine code for function main: Post SSA
0B
         BB#0: derived from LLVM BB %entry
16B
                    ADJCALLSTACKDOWN64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                    %EDI<def,dead> = MOV32ri64 <qa:@str>, %RDI<imp-def>
64B
80B
                    CALL64pcrel32 <qa:@puts>, <reqmask>, %RSP<imp-use>, %RDI<imp-use,kill>,
%RSP<imp-def>, %EAX<imp-def,dead>
96B
                    ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                    %EAX<def> = MOV32r0 %EFLAGS<imp-def,dead>
128B
                    RETQ %EAX<kill>
144B
```



****** MACHINEINSTRS ******



Post-register allocation

```
****** MACHINEINSTRS ******
# Machine code for function main: Post SSA
0B
         BB#0: derived from LLVM BB %entry
16B
                   ADJCALLSTACKDOWN64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
64B
                   %EDI<def,dead> = MOV32ri64 <qa:@str>, %RDI<imp-def>
80B
                   CALL64pcrel32 <qa:@puts>, <reqmask>, %RSP<imp-use>, %RDI<imp-use,kill>,
%RSP<imp-def>, %EAX<imp-def,dead>
96B
                   ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                   %EAX<def> = MOV32r0 %EFLAGS<imp-def,dead>
128B
                   RETO %EAX<kill>
144B
```

- Vregs are assigned to physical registers or stack slots based on liveness analysis
 - In this case, LLVM was able to eliminate several vreg definitions by allocating them to the same physical register used in the calling conventions (%edi, %eax)





Compiler Goals Redux: In-Depth





- Remember, we must ensure pointers are used in a semantically equivalent way across all architectures
- Approaches
 - Lay out program objects in a common format and at the same virtual address across all compilations
 - Transform program objects between ISA-specific formats (either statically or at migration time), update references accordingly
- The Popcorn compiler utilizes a mixture of both





- Popcorn lays out applications in a mostly-common format
 - Program objects (global data, functions, the heap) placed at identical addresses for all architectures
 - Stack/register set highly optimized for each ISA no common format
 - ISA defines number and types of registers
 - Compiler tailors stack frame to each ISA based on register allocation results, i.e., compiler spills values to stack that it can't put in registers
- Transform stack & registers between formats at migration time, everything else is aligned at link-time





- Data objects are equivalent across all architectures
 - Same primitive type sizes & alignments, compiler is forced to lay out higher order types in an identical format
 - Can be placed at identical locations at link-time (details later)
- Code cannot be in identical format for different ISAs
 - Like register set, operations/operand format is defined by ISA
 - The manner in which a processor implements a given piece of code is dependent on the operations it supports
 - In other words, a single piece of code compiled for two different architectures, while semantically identical, executes in different ways





```
void vec_add(const int* a, const int* b, int* c, size_t num) {
    size_t i;
    for(i = 0; i < num; i++)
        c[i] = a[i] + b[i];
}</pre>
```

```
file format elf64-x86-64
                                                                                                               vec add x86.o:
                   file format elf64-littleaarch64
vec_add_arm.o:
                                                                                                               Disassembly of section .text:
Disassembly of section .text:
                                                                                                               0000000000000000 <vec_add>:
                                                                                                                  0: 48 85 c9
                                                                                                                                         test %rcx,%rcx
00000000000000000 <vec add>:
                                                                                                                  3: 74 22
                                                                                                                                                27 <vec_add+0x27>
   0: b40000e3 cbz x3, 1c <vec add+0x1c>
                                                                                                                  5: 66 66 2e 0f 1f 84 00 data16 nopw %cs:0x0(%rax,%rax,1)
   4: b8404408 ldr w8, [x0],#4
                                                                                                                  c: 00 00 00 00
   8: b8404429 ldr w9, [x1],#4
                                                                                                                 10: 8b 06
                                                                                                                                                (%rsi),%eax
   c: 0b080128 add w8, w9, w8
                                                                                                                 12: 03 07
                                                                                                                                                (%rdi),%eax
                                                                                                                 14: 89 02
                                                                                                                                                %eax,(%rdx)
  10: b8004448 str w8, [x2],#4
                                                                                                                 16: 48 83 c7 04
                                                                                                                                                $0x4,%rdi
  14: d1000463 sub x3, x3, #0x1
                                                                                                                 1a: 48 83 c6 04
                                                                                                                                                $0x4,%rsi
  18: b5ffff63 cbnz x3, 4 <vec_add+0x4>
                                                                                                                 1e: 48 83 c2 04
                                                                                                                                                $0x4,%rdx
  1c: d65f03c0 ret
                                                                                                                 22: 48 ff c9
                                                                                                                 25: 75 e9
                                                                                                                                                10 <vec_add+0x10>
                                                                                                                 27: c3
                                                                                                                                         reta
```





```
void vec_add(const int* a, const int* b, int* c, size_t num) {
    size_t i;
    for(i = 0; i < num; i++)
        c[i] = a[i] + b[i];
}</pre>
```

Disassembly of section .text: 0000000000000000 <vec_add>: 0: 48 85 c9 test %rcx,%rcx 3: 74 22 27 <vec add+0x27> 5: 66 66 2e 0f 1f 84 00 data16 nopw %cs:0x0(%rax,%rax,1) c: 00 00 00 00 10: 8b 06 (%rsi),%eax 12: 03 07 (%rdi),%eax 14: 89 02 %eax,(%rdx) 16: 48 83 c7 04 \$0x4,%rdi 1a: 48 83 c6 04 \$0x4,%rsi 1e: 48 83 c2 04 \$0x4,%rdx

reta

file format elf64-x86-64

vec add x86.o:

22: 48 ff c9 25: 75 e9

27: c3





10 <vec_add+0x10>

```
void vec_add(const int* a, const int* b, int* c, size_t num) {
   size_t i;
   for(i = 0; i < num; i++)
      c[i] = a[i] + b[i];
}</pre>
```

```
file format elf64-x86-64
                                                                                                           vec add x86.o:
                   file format elf64-littleaarch64
vec_add_arm.o:
                                                                                                           Disassembly of section .text:
Disassembly of section .text:
                                                                                                           0000000000000000 <vec_add>:
                                                                                                              0: 48 85 c9
                                                                                                                                    test %rcx,%rcx
                                                 Perform addition
                                                                                 Perform addition
00000000000000000 <vec add>:
                                                                                                              3: 74 22
                                                                                                                                           27 <vec add+0x27>
   0: b40000e3 cbz x3, 1c <vec add+0x1c>
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                                                & update pointers
  4: b8404408 ldr w8, [x0],#4
                                                                                                              c: 00 00 00 00
  8: b8404429 ldr w9, [x1],#4
                                                                                                            10: 8b 06
                                                                                                                                           (%rsi),%eax
  c: 0b080128 add w8, w9, w8
                                                                                                             12: 03 07
                                                                                                                                           (%rdi),%eax
                                                                                  Update pointers
                                                                                                                                           %eax,(%rdx)
                                                                                                            14: 89 02
 10: b8004448 str w8, [x2],#4
                                                                                                             16: 48 83 c7 04
                                                                                                                                           $0x4,%rdi
 14: d1000463 sub x3, x3, #0x1
                                                                                                             1a: 48 83 c6 04
                                                                                                                                           $0x4,%rsi
                                                                                                                                     add
 18: b5ffff63 cbnz x3, 4 <vec add+0x4>
                                                                                                             1e: 48 83 c2 04
                                                                                                                                           $0x4.%rdx
 1c: d65f03c0 ret
                                                                                                             22: 48 ff c9
                                                                                                             25: 75 e9
                                                                                                                                           10 <vec_add+0x10>
                                                                                                             27: c3
                                                                                                                                     reta
```





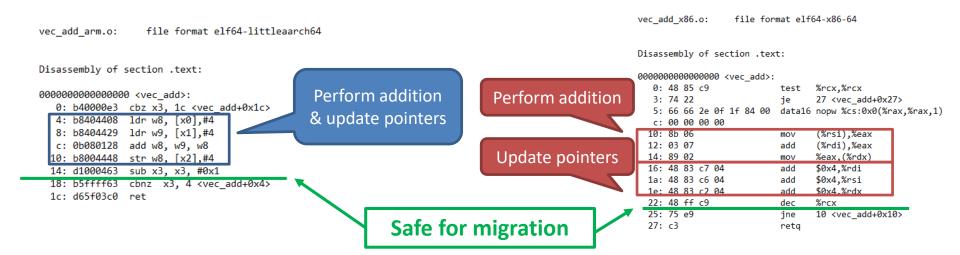
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```
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                                                                                 Perform addition
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                                                                                                              3: 74 22
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                                                                                                              5: 66 66 2e 0f 1f 84 00 data16 nopw %cs:0x0(%rax,%rax,1)
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                                                                                                              c: 00 00 00 00
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                                                                                                            10: 8b 06
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                                                                                                                                           (%rdi),%eax
                                                                                 Update pointers
                                                                                                                                           %eax,(%rdx)
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                                                                                                                                           $0x4,%rdi
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                                                                                                            1a: 48 83 c6 04
                                                                                                                                           $0x4,%rsi
                                                                                                                                    add
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                                                                                                            1e: 48 83 c2 04
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                                                                                                            22: 48 ff c9
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                                                                                                            25: 75 e9
                                                                                                                                           10 <vec add+0x10>
                                                                                                            27: c3
                                                                                                                                    reta
```





```
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    size_t i;
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        c[i] = a[i] + b[i];
}</pre>
```







- Questions in heterogeneous-ISA execution*
 - 1. Given a program address in machine code for one ISA, how do we find the equivalent address in code for another ISA (if there is one)?
 - 2. If we've established such a mapping, how do we generate a transformation of execution state (registers, stack frames) between ISA-specific formats? How do we ensure such a mapping is feasible?

*David G. von Bank, Charles M. Shub, and Robert W. Sebesta. 1994. A unified model of pointwise equivalence of procedural computations. *ACM Trans. Program. Lang. Syst.* 16, 6 (November 1994), 1842-1874.





- Questions in heterogeneous-ISA execution*
 - 1. Given a program address in machine code for one ISA, how do we find the equivalent address in code for another ISA (if there is one)?
 - 2. If we've established such a mapping, how do we generate a transformation of execution state (registers, stack frames) between ISA-specific formats? How do we ensure such a mapping is feasible?

The compiler programmatically selects a set of all such *equivalence points* and inserts call-outs to a migration library. These inserted points are called *migration points*.

*David G. von Bank, Charles M. Shub, and Robert W. Sebesta. 1994. A unified model of pointwise equivalence of procedural computations. *ACM Trans. Program. Lang. Syst.* 16, 6 (November 1994), 1842-1874.





Part 2: A day in the life of a Popcorn compilation





Part 2: A day in the life of a Popcorn compilation

All source & log files are available in the "het-compile" folder





Generating LLVM IR

fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
   unsigned i;
   for(i = 0; i < max; i++)
   {
      if((i % 5) == 0 && (i % 3) == 0)
          printf("fizzbuzz\n");
      else if((i % 5) == 0)
          printf("fizz\n");
      else if((i % 3) == 0)
          printf("buzz\n");
   }
}</pre>
```





Generating LLVM IR

clang -02 -emit-llvm -S fizzbuzz.c

fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
    unsigned i;
    for(i = 0; i < max; i++)
    {
        if((i % 5) == 0 && (i % 3) == 0)
            printf("fizzbuzz\n");
        else if((i % 5) == 0)
            printf("fizz\n");
        else if((i % 3) == 0)
            printf("buzz\n");
    }
}</pre>
```





Generating LLVM IR

clang -02 -emit-llvm -S fizzbuzz.c

fizzbuzz.ll

fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
   unsigned i;
   for(i = 0; i < max; i++)
   {
      if((i % 5) == 0 && (i % 3) == 0)
          printf("fizzbuzz\n");
      else if((i % 5) == 0)
          printf("fizz\n");
      else if((i % 3) == 0)
          printf("buzz\n");
   }
}</pre>
```

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  %cmp.23 = icmp eq i32 %max, 0
 br i1 %cmp.23, label %for.end, label %for.body.preheader
for.body.preheader: ; preds = %entry
 br label %for.body
for.body: ; preds = %for.body.preheader, %for.inc
  %i.024 = phi i32 [ %inc, %for.inc ], [ 0, %for.body.preheader ]
  %rem = urem i32 %i.024, 5
  %rem2 = urem i32 %i.024, 3
  %cmp3 = icmp eq i32 %rem2, 0
  ... (if-else statement implementation) ...
for.inc: ; preds = %if.then, %if.else.8, %if.then.11, %if.then.6
  %inc = add nuw i32 %i.024, 1
  %exitcond = icmp eq i32 %inc, %max
  br il %exitcond, label %for.end.loopexit, label %for.body
for.end.loopexit: ; preds = %for.inc
 br label %for.end
for.end: ; preds = %for.end.loopexit, %entry
  ret void
}
```





fizzbuzz.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  %cmp.23 = icmp eq i32 %max, 0
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                    [ 0, %for.body.preheader ]
  ... (if-else statement implementation) ...
for inc:
  ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
  br label %for.end
for.end:
  ret void
```





opt -select-migration-points -migration-points -S -o fizzbuzz-migpoints.ll fizzbuzz.ll

fizzbuzz.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  %cmp.23 = icmp eq i32 %max, 0
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                    [ 0, %for.body.preheader ]
  ... (if-else statement implementation) ...
for inc:
  ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
  br label %for.end
for.end:
  ret void
```





opt -select-migration-points -migration-points -S -o fizzbuzz-migpoints.ll fizzbuzz.ll

fizzbuzz.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  %cmp.23 = icmp eq i32 %max, 0
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                   [ 0, %for.body.preheader ]
 ...(if-else statement implementation)...
for inc:
  ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
  br label %for.end
for.end:
  ret void
```

opt lets you select individual passes to be run over the IR

- Popcorn passes are patched into LLVM at compiler install time
- Explore Popcorn passes/LLVM mods in <repo>/patches/llvm/src





opt -select-migration-points -migration-points -S -o fizzbuzz-migpoints.ll fizzbuzz.ll

fizzbuzz.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  %cmp.23 = icmp eq i32 %max, 0
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                    [ 0, %for.body.preheader ]
 ... (if-else statement implementation) ...
for inc:
  ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
 br label %for.end
for.end:
  ret void
```

fizzbuzz-migpoints.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  call void @check migrate(void (i8*)* null, i8* null)
  %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
  br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                    [ 0, %for.body.preheader ]
  ... (if-else statement implementation) ...
for.inc:
  ...(increment loop induction variable)...
  br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
  br label %for.end
for.end:
  call void @check migrate(void (i8*)* null, i8* null)
  ret void, !popcorn !2
```





opt -select-migration-points -migration-points -S -o fizzbuzz-migpoints.ll fizzbuzz.ll

fizzbuzz.ll

fizzbuzz-migpoints.ll

Compiler inserts migration points at beginning & end of all functions by default

- check_migrate defined in libmigrate.a
 and linked in by the compiler
- See SelectMigrationPoints.cpp in compiler repo for tuning options

```
define void @fizzbuzz(i32 %max) #0 {
  call void @check migrate(void (i8*)* null, i8* null)
  %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
  br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
  br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                    [ 0, %for.body.preheader ]
  ... (if-else statement implementation) ...
for.inc:
  ...(increment loop induction variable)...
  br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
  br label %for.end
for.end:
  call void @check migrate(void (i8*)* null, i8* null)
  ret void, !popcorn !2
```





- Need to accomplish the following:
 - Tag program locations (all call sites) with a unique ID
 - Record where live values at that location are stored
- Can't do either at the bitcode level!
 - No code layout what does a program location mean at the IR level?
 - No storage allocated for live values
- Insert *stackmap* intrinsic functions into bitcode
 - Record program and storage locations as back-end lowers bitcode to concrete representation
 - Modified for Popcorn Linux
 - See <u>Stack maps and patch points in LLVM</u> for more details





- Need to accomplish the following:
 - Tag program locations (all call sites) with a unique ID
 - Record where live at leastion are stored
- Pop quiz why **all** call sites instead of just migration points?
 - No code layout what does a program location mean at the IR level?
 - No storage allocated for live values
- Insert stackmap intrinsic functions into bitcode
 - Record program and storage locations as back-end lowers bitcode to concrete representation
 - Modified for Popcorn Linux
 - See <u>Stack maps and patch points in LLVM</u> for more details





fizzbuzz-migpoints.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
 br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                   [ 0, %for.body.preheader ]
 ... (if-else statement implementation) ...
for inc:
 ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
 br label %for.end
for.end:
 call void @check migrate(void (i8*)* null, i8* null)
 ret void, !popcorn !2
```





opt -insert-stackmaps -S -o fizzbuzz-stackmaps.ll fizzbuzz-migpoints.ll

fizzbuzz-migpoints.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
 br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                   [ 0, %for.body.preheader ]
 ... (if-else statement implementation) ...
for inc:
 ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
 br label %for.end
for end:
 call void @check migrate(void (i8*)* null, i8* null)
 ret void, !popcorn !2
```





opt -insert-stackmaps -S -o fizzbuzz-stackmaps.ll fizzbuzz-migpoints.ll

fizzbuzz-migpoints.ll

fizzbuzz-stackmaps.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end,
                 label %for.body.preheader
for.body.preheader:
 br label %for.body
for.body:
  %i.024 = phi i32 [ %inc, %for.inc ],
                   [ 0, %for.body.preheader ]
 ... (if-else statement implementation) ...
for inc:
 ... (increment loop induction variable)...
 br i1 %exitcond, label %for.end.loopexit,
                   label %for.body
for.end.loopexit:
 br label %for.end
for end:
 call void @check migrate(void (i8*)* null, i8* null)
 ret void, !popcorn !2
```

```
define void @fizzbuzz(i32 %max) #0 {
entry:
  call void @check migrate(void (i8*)* null, i8* null)
  call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0,
                             i32 0, i32 %max)
  %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
  br i1 %cmp.23, label %for.end, label %for.body.preheader
if.then:
  %puts22 = tail call i32 @puts(i8* getelementptr inbounds
              ([9 \times i8], [9 \times i8] * @str.4, i64 0, i64 0))
  call void (i64, i32, ...) @llvm.experimental.stackmap(i64 1,
                            i32 0, i32 %i.024, i32 %max)
  br label %for inc
for.end:
                                                    ; preds =
%for.end.loopexit, %entry
  call void @check migrate(void (i8*)* null, i8* null)
  call void (i64, i32, ...) @llvm.experimental.stackmap(i64 4,
  ret void, !popcorn !2
```





```
call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0, i32 0, i32 %max)
```





Unique call-site ID – made uniqued across all compiled files during post-processing (only have global view at link-time)

```
call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0, i32 0, i32 %max)
```





Inserting Stackmaps

Shadow bytes – unused by Popcorn

call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0, i32 0, i32 %max)





Inserting Stackmaps

List of live values at this program location

```
call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0, i32 0, i32 %max)
```





Inserting Stackmaps

```
call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0, i32 0, i32 %max)
```

We **create** equivalence points by inserting stackmaps into the bitcode

- Tags equivalent program locations across all compilations, as the same IR is lowered through multiple target-specific back-ends
- Lists all live values at equivalence point back-ends are simply responsible for recording where live values are located
- Back-ends must **not** optimize across stackmaps as this violates these invariants (see slide notes)





fizzbuzz-stackmaps.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0,
                            i32 0, i32 %max)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end, label %for.body.preheader
if.then:
  %puts22 = tail call i32 @puts(i8* getelementptr inbounds
             ([9 \times i8], [9 \times i8] * @str.4, i64 0, i64 0))
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 1,
                            i32 0, i32 %i.024, i32 %max)
 br label %for.inc
for.end:
                                                   ; preds =
%for.end.loopexit, %entry
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 4,
 ret void, !popcorn !2
```





clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll

fizzbuzz-stackmaps.11

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0,
                            i32 0, i32 %max)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end, label %for.body.preheader
if.then:
  %puts22 = tail call i32 @puts(i8* getelementptr inbounds
             ([9 \times i8], [9 \times i8] * @str.4, i64 0, i64 0))
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 1,
                            i32 0, i32 %i.024, i32 %max)
 br label %for.inc
for.end:
                                                   ; preds =
%for.end.loopexit, %entry
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 4,
 ret void, !popcorn !2
```





clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll

fizzbuzz-stackmaps

```
define void @fizzbuzz
entry:
  call void @check_mic
  call void (i64, i32,
  %cmp.23 = icmp eq i3
  br i1 %cmp.23, label
```

- -mllvm: Pass option directly to LLVM's middle-/back-end
- -optimize-regalloc: use an optimizing register allocator (versus LLVM's fast allocator), which calculates live value ranges in the backend; required by Popcorn's analyses





clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll

fizzbuzz-stackmaps.11

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0,
                            i32 0, i32 %max)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end, label %for.body.preheader
if.then:
  %puts22 = tail call i32 @puts(i8* getelementptr inbounds
              ([9 \times i8], [9 \times i8] * @str.4, i64 0, i64 0))
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 1,
                            i32 0, i32 %i.024, i32 %max)
 br label %for.inc
for.end:
                                                   ; preds =
%for.end.loopexit, %entry
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 4,
  ret void, !popcorn !2
```



ELF object file

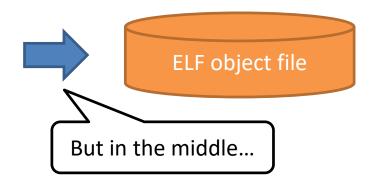




clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll

fizzbuzz-stackmaps.ll

```
define void @fizzbuzz(i32 %max) #0 {
entry:
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 0,
                            i32 0, i32 %max)
 %cmp.23 = icmp eq i32 %max, 0, !popcorn !2
 br i1 %cmp.23, label %for.end, label %for.body.preheader
if.then:
  %puts22 = tail call i32 @puts(i8* getelementptr inbounds
              ([9 \times i8], [9 \times i8] * @str.4, i64 0, i64 0))
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 1,
                            i32 0, i32 %i.024, i32 %max)
 br label %for.inc
for.end:
                                                   ; preds =
%for.end.loopexit, %entry
 call void @check migrate(void (i8*)* null, i8* null)
 call void (i64, i32, ...) @llvm.experimental.stackmap(i64 4,
  ret void, !popcorn !2
```







clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=regalloc

```
****** MACHINEINSTRS ******
# Machine code for function fizzbuzz: Post SSA
Function Live Ins: %EDI in %vreq4
0B
          BB#0: derived from LLVM BB %entry
              Live Ins: %EDI
                    %vreq5<def> = COPY %EDI; GR32:%vreq5
16B
                    ADJCALLSTACKDOWN64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
80B
96B
                    %EDI<def,dead> = MOV32r0 %EFLAGS<imp-def,dead>, %RDI<imp-def>
                    %ESI<def,dead> = MOV32r0 %EFLAGS<imp-def,dead>, %RSI<imp-def>
112B
128B
                    CALL64pcrel32 <ga:@check migrate>, <regmask>, %RSP<imp-use>, %RDI<imp-use>,
                                                                  %RSI<imp-use, kill>
                    ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
144B
160B
                    ADJCALLSTACKDOWN64 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                    STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
176B
192B
                    ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
208B
                    CMP32ri8 %vreq5, 0, %EFLAGS<imp-def>; GR32:%vreq5
                    JE 1 <BB#10>, %EFLAGS<imp-use,kill>
224B
              Successors according to CFG: BB#10 BB#1
```





clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=regalloc

```
***** MACHINEINSTRS ******
# Machine code for function fizzbuzz: Post SSA
Function Live Ins: %EDI i
                          Bitcode stackmaps are lowered to machine code IR
         BB#0: derived
                          stackmaps
             Live Ins:
                             First 2 arguments unchanged (ID, shadow bytes)
                             Bitcode values lowered to machine code
                             operands depending on where they're allocated
                                                                                 RDI<imp-use>,
                             (virtual registers, constants, stack slots)
                                            RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                                OWN64 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                   STACKMAP 0, 0, %vreg5, ...; GR32:%vreg5
176B
                   ADJCALLSTACKUP64 0, 0, %RSP<imp-def>, %EFLAGS<imp-def,dead>, %RSP<imp-use>
                   CMP32ri8 %vreq5, 0, %EFLAGS<imp-def>; GR32:%vreq5
                   JE 1 <BB#10>, %EFLAGS<imp-use, kill>
             Successors according to CFG: BB#10 BB#1
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
****** STACK TRANSFORMATION METADATA ******
****** Function: fizzbuzz
***** REGISTER MAP *******
[%vreq5 -> %R14D] GR32
[%vreq11 -> %EDX] GR32
[%vreg12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
i32 %max: in register %R14D (vreg 5)
Duplicate operand locations:
*** Finding architecture-specific live values ***
 STACKMAP 0, 0, %vreg5, ...; GR32:%vreg5
 -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
****** STACK TRANSFORMATION METADATA ******
****** Function: fizzbuzz
***** REGISTER MAP *******
                                                   Metadata emitted by vanilla stackmaps is
[%vreq5 -> %R14D] GR32
[%vreq11 -> %EDX] GR32
                                                   not complete
[%vreq12 -> %AL] GR8
                                                        Intended to allow capturing enough
                                                        live state to jump to optimized
*** Stack slot copies ***
                                                        implementation (e.g., hot-patching
Stackmap 0:
                                                        optimized code in virtual machine)
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
                                                       Need to augment with complete
i32 %max: in register %R14D (vreg 5)
                                                        frame information
                                                       See StackTransformMetadata.cpp
Duplicate operand locations:
                                                        for more details
*** Finding architecture-specific live values ***
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
 -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
    ***** STACK TRANSFORMATION METADATA *******
     **** Function: fizzbuzz
   ***** REGISTER MAP ******
[%vreq5 -> %R14D] GR32
                                    Register allocation results
[%vreq11 -> %EDX] GR32
[%vreq12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
  STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
Duplicate operand locations:
*** Finding architecture-specific live values ***
  STACKMAP 0, 0, %vreg5, ...; GR32:%vreg5
  -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
    **** Function: fizzbuzz
    ***** REGISTER MAP *******
[%vreg12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
                                           Mapping of IR values -> machine-code values
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
                                             Value *may* be live in multiple locations
i32 %max: in register %R14D (vreg 5)
Duplicate operand locations:
*** Finding architecture-specific live values ***
 STACKMAP 0, 0, %vreg5, ...; GR32:%vreg5
 -> Call instruction SlotIndex 128B, searching vreqs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
    ***** STACK TRANSFORMATION METADATA
      **** Function: fizzbuzz
     **** REGISTER MAP ******
[%vreg12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
  STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
                                             Handle architecture-specific live values that
Duplicate operand locations:
                                             may arise due to backend-optimizations or ABI
*** Finding architecture-specific live values ***
  STACKMAP 0, 0, %vreg5, ...; GR32:%vreg5
  -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
     **** STACK TRANSFORMATION METADATA ******
       *** Function: fizzbuzz
     **** REGISTER MAP ******
[%vreg12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
  STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
Duplicate operand locations:
*** Finding architecture-specific li
                                      SlotIndex: instruction location in machine code IR
  STACKMAP 0, 0, %vreq5, ...; GD52:%\req5
  -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





```
clang -c -mllvm -optimize-regalloc -o fizzbuzz.o fizzbuzz-stackmaps.ll -mllvm -debug-only=stacktransform
     *** Function: fizzbuzz
     **** REGISTER MAP ******
[%vreq12 -> %AL] GR8
*** Stack slot copies ***
Stackmap 0:
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
                  Looking for registers/stack slots live across stackmap but not
                  contained in stackmap
                     Back-end will issue warning if it finds live value it can't handle
                     during transformation – pay attention to these warnings!
*** Finding archit
 STACKMAP 0, 0, %vreq5, ...; GR32:%vreq5
 -> Call instruction SlotIndex 128B, searching vregs 0 -> 31 and stack slots 0 -> 0
```





readelf -SW fizzbuzz.o

There are 17 section headers, starting at offset 0x5e0:

Section Headers:

	i iicaacib.														
[Nr]	Name	Type	Address	Off	Size	ES	Flg	Lk	Inf	Al					
[0]		NULL	0000000000000000	000000	000000	00		0	0	0					
[1]	.strtab	STRTAB	0000000000000000	0004b0	00012f	00		0	0	1					
[2]	.text	PROGBITS	0000000000000000	000040	0000b9	00	AX	0	0	16					
[3]	.rela.text	RELA	0000000000000000	0003a8	0000c0	18		16	2	8					
[4]	.data	PROGBITS	0000000000000000	0000fc	000000	00	WA	0	0	4					
[5]	.bss	NOBITS	0000000000000000	0000fc	000000	00	WA	0	0	4					
[6]	.rodata.str1.1	PROGBITS	0000000000000000	0000fc	000013	01	AMS	0	0	1					
[7]	.comment	PROGBITS	0000000000000000	00010f	000035	01	MS	0	0	1					
[8]	.note.GNU-stack	PROGBITS	0000000000000000	000144	000000	00		0	0	1					
[9]	.stack_transform.	unwind PROGBITS	0000000000	000000	000144	0000	10 () 4		0	0	4			
	.stack_transform.											0	0	8	
[11]	<pre>.rela.stack_trans</pre>	form.unwind_aran	ge RELA	000000	0000000	0000	000)468	000	0018	18		16	10	8
	.llvm_stackmaps		0000000000000000	000168	000118	00	А	0	0	8					
[13]	.rela.llvm_stackm	aps RELA	000000000000000000000000000000000000000	000 000	480 0000	018	18		16	12	8				
[14]	.eh_frame	PROGBITS	0000000000000000	000280	000038	00	А	0	0	8					
[15]	.rela.eh_frame	RELA	0000000000000000	000498	000018	18		16	14	8					
[16]	.symtab	SYMTAB	0000000000000000	0002b8	0000f0	18		1	7	8					
Key to	Key to Flags:														
ıw) W	rite), A (alloc),	X (execute), M (merge), S (string:	s), l (i	large)										
I (ir	nfo), L (link orde	r), G (group), T	(TLS), E (exclude	e), x (ı	unknown))									

- O (extra OS processing required) o (OS specific), p (processor specific)





readelf -SW fizzbuzz.o

There are 17 section headers, starting at offset 0x5e0:

```
Metadata describing callee-save
                                     information for functions
                                        Unwind frames from the stack
[ 9] .stack transform.unwind PROGBITS
                                           000000000000000 000144 000010 04
[10] .stack transform.unwind arange PROGBITS
                                                  000000000000000 000158 000010 10
W (write), A (alloc), X (execute), M (merge), S (strings), 1 (large)
I (info), L (link order), G (group), T (TLS), E (exclude), x (unknown)
O (extra OS processing required) o (OS specific), p (processor specific)
```





readelf -SW fizzbuzz.o

There are 17 section headers, starting at offset 0x5e0:

```
Stack transformation metadata
                                 Program locations (function + offset)
                                 Live value locations
    .stack transform.unwind arange
    .llvm stackmaps
                      PROGBITS
                                      0000000000000000 000168 000118 00
    .rela.llvm stackmaps RELA
W (write), A (alloc), X (execute), M (merge), S (strings), 1 (large)
I (info), L (link order), G (group), T (TLS), E (exclude), x (unknown)
O (extra OS processing required) o (OS specific), p (processor specific)
```





```
Reading section .llvm stackmaps: Found 1 stackmaps
Stackmap v1: 1 functions, 0 constants, 5 call sites
 Function 0: address=0, stack size=24, number of unwinding entries: 4, offset into unwinding
section: 0
 Call site 0: function 0, offset @ 19, 1 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 14
 Call site 1: function 0, offset @ 92, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 2: function 0, offset @ 121, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 3: function 0, offset @ 154, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 4: function 0, offset @ 180, 0 locations, 0 live-outs, 0 arch-specific locations
```





```
Reading section .llvm stackmaps: Found 1 stackmaps
Stackmap v1: 1 functions, 0 constants, 5 call sites
 Function 0: address=0, size=24, number of unwinding entries: 4, offset into unwinding
section: 0
                                                                           pecific locations
 Call site 0: funct
                     Number of functions for which we have metadata,
   Location: in red
 Call site 1: funct
                                                                           ecific locations
                      number of stackmap call sites across all functions
   Location: in red
   Location: in register 14
 Call site 2: function 0, offset @ 121, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 14
 Call site 3: function 0, offset @ 154, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 4: function 0, offset @ 180, 0 locations, 0 live-outs, 0 arch-specific locations
```





```
Reading section .llvm stackmaps: Found 1 stackmaps
Stackmap v1: 1 functions, 0 constants, 5 call sites
 Function 0: address=0, stack size=24, number of unwinding entries: 4, offset into unwinding
section: 0
 Call site 0: function
                                   19, 1 locations, 0 live-outs, 0 arch-specific locations
   Location: in r
 Call site 1: fun
                                                                          specific locations
                     Per-function metadata describing frame size and
   Location: in r
                          how to unwind the frame to the caller
   Location: in :
 Call site 2: function 0, offset @ 121, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 14
 Call site 3: function 0, offset @ 154, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 4: function 0, offset @ 180, 0 locations, 0 live-outs, 0 arch-specific locations
```





```
Reading section .llvm stackmaps: Found 1 stackmaps
Stackmap v1: 1 functions, 0 constants, 5 call sites
 Function 0: address=0, stack size=24, number of unwinding entries: 4, offset into unwinding
section: 0
 Call site 0: function 0, offset @ 19, 1 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 14
 Call site 1: function offset @ 92, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register
   Location: in re
                    Per-call site information describing program location &
                                                                              cific locations
 Call site 2: fun
   Location: in r
                     live values (one per stackmap inserted into bitcode)
   Location: in
 Call site 3: function 0, offset @ 154, 2 locations, 0 live-outs, 0 arch-specific locations
   Location: in register 3
   Location: in register 14
 Call site 4: function 0, offset @ 180, 0 locations, 0 live-outs, 0 arch-specific locations
```





Putting It All Together

```
$ clang -02 -popcorn-migratable -c fizzbuzz.c
$ ls
fizzbuzz.c fuzzbuzz.o fizzbuzz_x86_64.o
$ file fizzbuzz.o
fizzbuzz.o: ELF 64-bit LSB relocatable, ARM aarch64, version 1 (GNU/Linux), not stripped
$ file fizzbuzz_x86_64.o
fizzbuzz x86 64.o: ELF 64-bit LSB relocatable, x86-64, version 1 (GNU/Linux), not stripped
```





Putting It All Together

- Insert migration library call-outs, collect stack transformation metadata at equivalence points
- Generate object files for all supported architectures simultaneously (requires -c)

```
$ clang -02 -popcorn-migratable -c fizzbuzz.c
$ ls
fizzbuzz.c fuzzbuzz.o fizzbuzz_x86_64.o
$ file fizzbuzz.o
fizzbuzz.o: ELF 64-bit LSB relocatable, ARM aarch64, version 1 (GNU/Linux), not stripped
$ file fizzbuzz_x86_64.o
fizzbuzz_x86_64.o: ELF 64-bit LSB relocatable, x86-64, version 1 (GNU/Linux), not stripped
```





Compilation Recap

- Inserts call-outs to migration library
- Constructs equivalence points by inserting stackmaps into LLVM bitcode
 - Tags program locations across compilations for all targets
 - Captures locations of all live values at equivalence points
- Generates single set of optimized LLVM bitcode and lowers it through multiple target-specific backends





Part 3: Linking & post-processing a Popcorn compilation





Part 3: Linking & post-processing a Popcorn compilation

All source & log files are available in the "het-link" folder





- The compiler has taken care of generating metadata required for stack/register transformation
- Still need to align global objects
 - Statically-allocated global data
 - Code, i.e., functions
 - We do not need to worry about dynamically-allocated data (heap)
 - Memory allocator (e.g., malloc) is responsible for arranging data in heap
 - Use semantically equivalent memory allocator (musl) on all architectures





- Linux uses the Executable and Linkable Format (ELF)
 - Data sections (statically allocated):
 - .rodata read-only global data initialized within the program
 - .data readable/writable global data initialized within the program
 - .bss readable/writable global data not initialized within the program
 - Linux initializes to zero
 - Code section:
 - text ISA-specific machine code generated by the compiler
 - Miscellaneous symbol/string tables, constructors/destructors,
 debugging information
 - Popcorn's compiler adds metadata sections required for stack transformation





- Use *linker scripts* to align symbols across all compilations
 - Program objects referenced by symbol requires all program objects have a symbol attached, including string literals
 - See NameStringLiterals.cpp in repo for details
 - After generating "vanilla" (read: unaligned) version of binary for each architecture, generate linker script & re-link
 - See the <u>documentation on linker scripts</u> for more details





- Linker scripts can't control placement of symbols, only ELF sections
 - Luckily, ELF format permits arbitrary numbers of sections in object files
 - Solution: place each program object in its own section
 - Requires -ffunction-sections & -fdata-sections (included automatically with -popcorn-migratable)





fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
    unsigned i;
    for(i = 0; i < max; i++)
    {
        if((i % 5) == 0 && (i % 3) == 0)
            printf("fizzbuzz\n");
        else if((i % 5) == 0)
            printf("fizz\n");
        else if((i % 3) == 0)
            printf("buzz\n");
    }
}</pre>
```





clang -02 -popcorn-migratable -c fizzbuzz.c

fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
   unsigned i;
   for(i = 0; i < max; i++)
   {
      if((i % 5) == 0 && (i % 3) == 0)
          printf("fizzbuzz\n");
      else if((i % 5) == 0)
          printf("fizz\n");
      else if((i % 3) == 0)
          printf("buzz\n");
   }
}</pre>
```





clang -02 -popcorn-migratable -c fizzbuzz.c

fizzbuzz.c

```
#include <stdio.h>

void fizzbuzz(unsigned max)
{
    unsigned i;
    for(i = 0; i < max; i++)
    {
        if((i % 5) == 0 && (i % 3) == 0)
            printf("fizzbuzz\n");
        else if((i % 5) == 0)
            printf("fizz\n");
        else if((i % 3) == 0)
            printf("buzz\n");
    }
}</pre>
```







fizzbuzz_x86_64.o (x86-64)





readelf -SW fizzbuzz.o

fizzbuzz.o (AArch64)

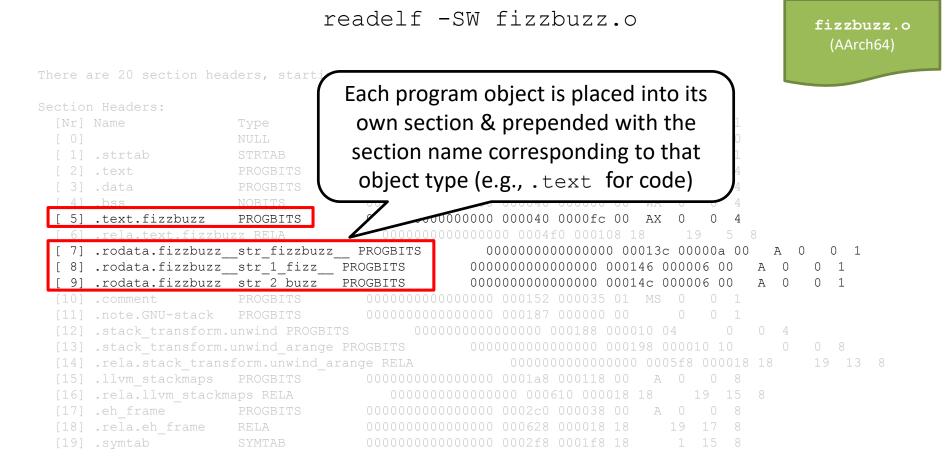
There are 20 section headers, starting at offset 0x7f0:

Section Headers:

[Nr]	Name	Type	Address	Off	Size	ES	Flg	Lk	Inf	Al					
[0]		NULL	00000000000000000	000000	000000	00		0	0	0					
[1]	.strtab	STRTAB	00000000000000000	000640	0001a9	00		0	0	1					
[2]	.text	PROGBITS	00000000000000000	000040	000000	00	ΑX	0	0	4					
[3]	.data	PROGBITS	00000000000000000	000040	000000	00	WA	0	0	4					
[4]	.bss	NOBITS	00000000000000000	000040	000000	00	WA	0	0	4					
[5]	.text.fizzbuzz	PROGBITS	00000000000000000	000040	0000fc	00	AX	0	0	4					
[6]	.rela.text.fizzbu	zz RELA	000000000000000000000000000000000000000	00 0004:	f0 00010	08 1	8	1	. 9	5	8				
[7]	.rodata.fizzbuzz_	_str_fizzbuzz	PROGBITS 0	0000000	0000000	00 0	013	0.0	000a	a 00)	Α	0	0 1	
[8]	.rodata.fizzbuzz_	_str_1_fizz P	ROGBITS 0000	0000000	000000	0001	46 (0000	06 (00	Α	0	0	1	
[9]	.rodata.fizzbuzz_	_str_2_buzz P	ROGBITS 0000	0000000	000000	0001	4c (0000	06 (00	Α	0	0	1	
[10]	.comment	PROGBITS	00000000000000000	000152	000035	01	MS	0	0	1					
[11]	.note.GNU-stack	PROGBITS	00000000000000000	000187	000000	00		0	0	1					
[12]	.stack_transform.	unwind PROGBITS	000000000	000000	000188	0000	10 () 4		0	0	4			
[13]	.stack_transform.	unwind_arange P	ROGBITS 0000	0000000	000000	0001	98 (0000	10 1	10		0	0	8	
[14]	.rela.stack_trans	form.unwind_ara	nge RELA	00000	0000000	0000	000)5f8	000	0018	18		19	13	8
[15]	.llvm_stackmaps	PROGBITS	00000000000000000	0001a8	000118	00	A	0	0	8					
[16]	.rela.llvm_stackm	aps RELA	000000000000000000000000000000000000000	000 000	610 0000	018	18		19	15	8				
[17]	.eh_frame	PROGBITS	00000000000000000	0002c0	000038	00	A	0	0	8					
[18]	.rela.eh frame	RELA	00000000000000000	000628	000018	18		19	17	8					
								-		-					











- We use a modified linker based on GNU's gold and a python tool pyalign for alignment
- First linking pass
 - Link vanilla (unaligned) version of binary for each target
 - Dump section names, including sizes & alignments, into a map file
- Alignment
 - Parse binaries/map file and generate linker script for each target
- Second linking pass
 - Link heterogeneous (aligned) version of binary for each target using linker scripts generated by pyalign





```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map_aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz_aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc eh -end-goup
```









```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map_aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz_aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc eh -end-goup
```



```
Archive member included because of file (symbol)
                                                                                      map aarch64.txt
Memory map
 ** file header
                   0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 0 0 0
                                                  0 \times 40
 ** segment headers
                    0x0000000000400040
                                                  0xe0
                    0x0000000000400120
                                              0x21744
.text
                                                  0x24 0x4 /home/rlyerly/Downloads/popcorn-compiler/test-
 .text.exit
                   0x0000000000400120
install/aarch64/lib/libc.a(exit.o)
                   0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
                                                             exit
 .text
                   0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 4 4
                                                   0x0 0x4 main.o
 .text.main
                   0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 4 4
                                                  0x7c 0x4 main.o
                    0x0000000000400144
                                                             main
```





```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc eh -end-goup
```



 $0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 4 4$

0x0000000000400144

map aarch64.txt

```
Section name
.text
                     0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
                                                  0x21744
                                                      0x24 0x4 /home/rlyerly/Downloads/popcorn-compiler/test-
 .text.exit
                     0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
install/aarch64/lib/libc.a(exit.o)
                     0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
                                                                  exit
                     0x0000000000400144
```

.text.main

.text

0x0 0x4 main.o 0x7c 0x4 main.o

main





```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc eh -end-goup
                                                                             map aarch64.txt
       ** file header
                           Virtual memory address
                      0x0000000000400120
                                             0x21744
      .text
                      0x0000000000400120
                                               0x24 0x4 /home/rlyerly/Downloads/popcorn-compiler/test-
       .text.exit
      install/aarch64/lib/libc.a(exit.o)
                      0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
                                                         exit
       .text
                      0x0000000000400144
                                                 0x0 0x4 main.o
        .text.main
                      0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 4 4
                                                0x7c 0x4 main.o
                      0x0000000000400144
                                                         main
```





```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map_aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz_aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc_eh -end-goup
```



Archive member included because of file (symbol

map_aarch64.txt

Memory map

** file header

 $0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 0 0 0$

** segment headers

0x0000000000400040

0x0000000000400120 0x0000000000400144

.text 0x000000000400144 .text.main 0x000000000400144

0x0000000000400144



0x21744

0x24 0x4 /home/rlyerly/Downloads/popcorn-compiler/test-

exit
0x0 0x4 main.o
0x7c 0x4 main.o
main

...





```
$ ld.gold -L/usr/lib/gcc-cross/aarch64-linux-gnu/5 -Map map_aarch64.txt \
    main.o fizzbuzz.o -o fizzbuzz_aarch64
    <install>/aarch64/lib/crt1.o <install>/aarch64/lib/libc.a \
    <install>/aarch64/lib/libmigrate.a <install>/aarch64/lib/libstack-transform.a \
    <install>/aarch64/lib/libelf.a <install>/aarch64/lib/libc.a \
    --start-group -lgcc -lgcc eh -end-goup
```



```
map aarch64.txt
 ** file header
 ** segment headers
                                                      Alignment
                                          0x21744
                  0x0000000000400120
.text
                                              0x24 0x4 /home/rlyerly/Downloads/popcorn-compiler/test-
 .text.exit
                  0x0000000000400120
install/aarch64/lib/libc.a(exit.o)
                  0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 2 0
                                                        exit
 .text
                  0x0000000000400144
                                               0x0 0x4 main.o
 .text.main
                  0 \times 0 0 0 0 0 0 0 0 0 0 4 0 0 1 4 4
                                              0x7c 0x4 main.o
                  0x0000000000400144
                                                        main
```





```
$ pyalign --compiler-inst <install> \
    --arm-bin fizzbuzz_aarch64 --arm-map map_aarch64.txt \
    --x86-bin fizzbuzz x86 64 --x86-map map x86 64.txt
```





```
$ pyalign --compiler-inst <install> \
    --arm-bin fizzbuzz_aarch64 --arm-map map_aarch64.txt \
    --x86-bin fizzbuzz_x86_64 --x86-map map_x86_64.txt
```



linker script arm.x





```
$ pyalign --compiler-inst <install> \
      --arm-bin fizzbuzz aarch64 --arm-map map aarch64.txt \
      --x86-bin fizzbuzz x86 64 --x86-map map x86 64.txt
                                                    linker script arm.x
/* Default linker script, for normal executables */
OUTPUT FORMAT ("elf64-littleaarch6
                 "elf64-littleaar
                                    Re-link each binary with
OUTPUT ARCH (aarch64)
                                    generated linker script –
ENTRY( start)
SECTIONS
                                      they're now aligned!
          : ALIGN(0x100000)
 .text
           . = . + 1;
           . = ALIGN(0x1000);
           . = ALIGN(0x10); /* align for .text.main */
          "main.o"(.text.main); /* size 0x7c */
           \cdot = ALIGN(0x10); /* align for .text.fizzbuzz */
          "fizzbuzz.o"(.text.fizzbuzz); /* size 0xfc */
```





- Need to reorganize LLVM's stackmap section
 - Not conducive for fast runtime acces
 - Variable sized components within a call site record
 - Stackmap sections from multiple files lumped together
 - Need to uniquify call site IDs across compilation units





gen-stackinfo -f fizzbuzz_aarch64 && readelf -SW fizzbuzz_aarch64





gen-stackinfo -f fizzbuzz_aarch64 && readelf -SW fizzbuzz_aarch64



There are 38 section headers, starting at offset 0x66a3cb:

Section Headers:

[Nr]	Name	Type	Address	Off	Size	ES	Flg	Lk	Inf	Al		
[0]		NULL	0000000000000000	000000	000000	00		0	0	0		
[1]	.text	PROGBITS	000000000500000	100000	024ec4	00	AX	0	0	1048576		
[2]	.rodata	PROGBITS	0000000000600000	200000	00438f	00	A	0	0	1048576		
[31]	.symtab	SYMTAB	0000000000000000	655618	00fe10	18		32	2280	8		
[32]	.strtab	STRTAB	0000000000000000	665428	0039ef	00		0	0	1		
[33]	.shstrtab	STRTAB	0000000000000000	668e17	000208	00		0	0	1		
[34]	.stack_transform.:	id PROGBITS	000000000000000000000000000000000000000	00 66901	lf 0007e	ec 3	34		0	0 0		
[35]	.stack transform.	addr PROGBITS	000000000000000000000000000000000000000	0000 669	980b 000	7ec	34		0	0 0		
[36]	.stack_transform.	live PROGBITS	000000000000000000000000000000000000000	0000 669	9ff7 000	348	0c		0	0 0		
[37]	.stack transform.a	arch const PROGB	ITS 000000	0000000	000 66a3	33f	0000)8c	14	0	0	0





gen-stackinfo -f fizzbuzz_aarch64 && readelf -SW fizzbuzz_aarch64



There are 38 section headers, starting at offset 0x66a3cb:

S	ection	n Headers:										
	[Nr]	Name	Type	Address	Off	Size	ES Flg	Lk	Inf	Al		
	[0]		NULL	00000000000000000	000000	000000	00	0	0	0		
	[1]	.text	PROGBITS	000000000500000	100000	024ec4	00 AX	0	0	10485	76	
	[2]	.rodata						0	0	10485	76	
			Consumed by t	he stack transfo	ormatio	on run	time					
	[31]	.symtab	consumed by t	ine stack transit	J. III a civ	J		32	2280	8		
	[32]	.strtab	STRT	000000000000000000000000000000000000000	665428	0039ef	0 0	0	0	1		
	[33]	ghetrtah	CURTAR	000000000000000000000000000000000000000	668e17	000208	00	0	0	1		
	[34]	.stack transform.	id PROGBITS	000000000000000000000000000000000000000	00 6690	lf 0007e	ec 34		0	0 0		
	[35]	.stack transform.	addr PROGBITS	00000000000	0000 66	980b 000	07ec 34		0	0 (О	
	[36]	.stack transform.	live PROGBITS	00000000000	0000 66	9ff7 000	0348 Oc		0	0 (С	
	[37]	.stack transform.	arch const PROGB!	ITS 000000	0000000	000 66a3	33f 000	08c	14	0	0	0
		_	_	•								





- The binaries are now ready for runtime migration
 - One binary per target in the format <name>_<target>
- Useful utilities:
 - check-align.py: consume the symbol tables of two binaries to verify that all symbols begin at aligned virtual addresses
 - check-stackmaps.py: sanity check the stackmaps generated by the compiler (same numbers and types of functions, call sites, live values)
 - Must be run post-alignment matches functions by address





Part 4: Migration & Stack Transformation





Migrating Between Architectures

Migration in Popcorn Linux

- Somebody (either inside or outside the application) proposes that a given thread migrates to a given destination node
- The check_migrate function queries whether a migration has been proposed for the current thread
- If so, check_migrate invokes stack transformation
 - Take a snapshot of current register set
 - Rewrite stack to another location in memory (in userspace)
 - Return populated destination ISA register set
- Pass rewritten register set to kernel's thread migration service
- Resume execution in check_migrate on destination





• Proposing migration (libmigrate:trigger.c):

syscall(SYSCALL_PROPOSE_MIGRATION, pid, nid)





• Proposing migration (libmigrate:trigger.c):

Direct shortcut to the system call interface

syscall (SYSCALL PROPOSE MIGRATION, pid, nid)





• Proposing migration (libmigrate:trigger.c):

System call number – proposing a migration

syscall (SYSCALL_PROPOSE_MIGRATION, pid, nid)





• Proposing migration (libmigrate:trigger.c):

For which task are we proposing migration

syscall(SYSCALL_PROPOSE_MIGRATION, pid, nid)





• Proposing migration (libmigrate:trigger.c):

To which node the task should migrate

syscall (SYSCALL PROPOSE MIGRATION, pid, nid)





Checking to see if a migration was proposed
 (libmigrate:migrate.c):

syscall(SYSCALL_MIGRATION_PROPOSED)





Checking to see if a migration was proposed

```
(libmigrate:migrate.c):
```

Return whether a migration was proposed for the current thread

- >= 0: proposed destination node
- < 0: no migration proposed

syscall(SYSCALL_MIGRATION_PROPOSED)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

syscall(SYSCALL_SCHED_MIGRATE, nid, regs_dst, sp, bp)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

```
Migrate the thing!
```

syscall(SYSCALL_SCHED_MIGRATE, nid, regs_dst, sp, bp)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

Where to migrate

syscall (SYSCALL_SCHED_MIGRATE, nid, regs_dst, sp, bp)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

Destination register set – thread will be restarted with these registers on destination

• Generated by stack transformation runtime

syscall(SYSCALL_SCHED_MIGRATE, nid, regs_dst, sp, bp)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

New stack & frame pointer on destination

syscall(SYSCALL_SCHED_MIGRATE, nid, regs_dst, sp, bp)





Invoking thread migration service

```
(libmigrate:migrate.c):
```

These interfaces are subject to change – see <repo>/lib/migrate for up-to-date versions!
syscall(S





Stack Transformation

- Rewrite entire stack from outermost frame inwards
- Stack transformation runtime (the "runtime") opens metadata sections using libelf
 - .stack_transform.unwind-per-function callee-saved register
 locations on the stack for frame unwinding
 - .stack_transform.unwind_arange address ranges for functions in the binary (used for bootstrapping outermost frame)
 - .stack_transform.id call sites (stackmaps) sorted by ID
 - .stack transform.addr call sites sorted by program location
 - .stack_transform.live live value location records
 - .stack_transform.arch_const architecture-specific live value records



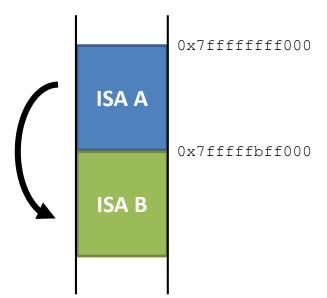


Stack Transformation

- All transformation is performed in userspace
 - Linux by default gives the main thread 8MB of stack space (musl is modified to do the same for spawned threads)

Divide stack into upper/lower half, rewrite from one to the other at

migration time





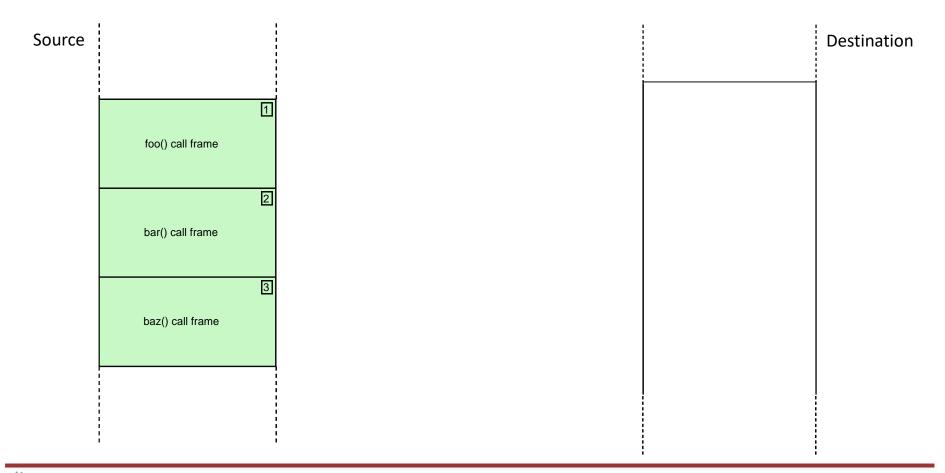


Stack Transformation

- Runtime initializes handles containing transformation metadata at program startup
 - Ways to tell runtime name of binary containing a target's metadata
 - 1. Set environment variable ST <target> BIN
 - 2. Define symbol <target> fn
 - 3. If (1) & (2) not used, runtime will default to appending target to current executing binary's name

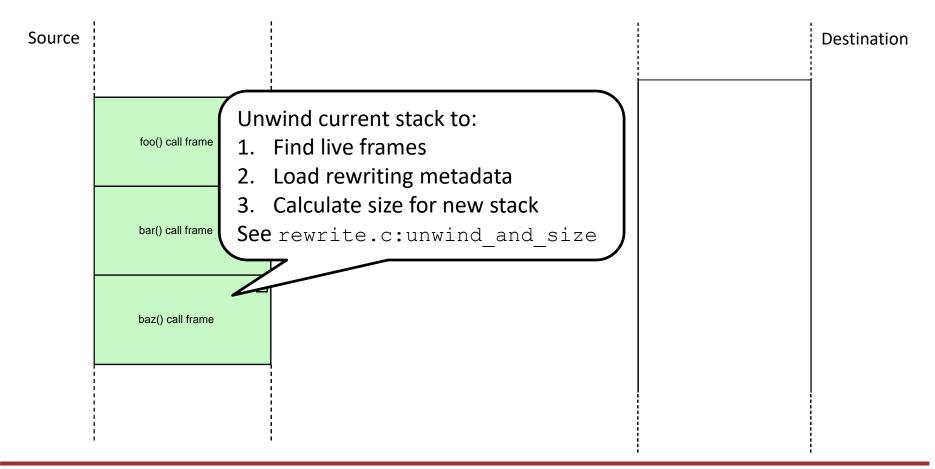






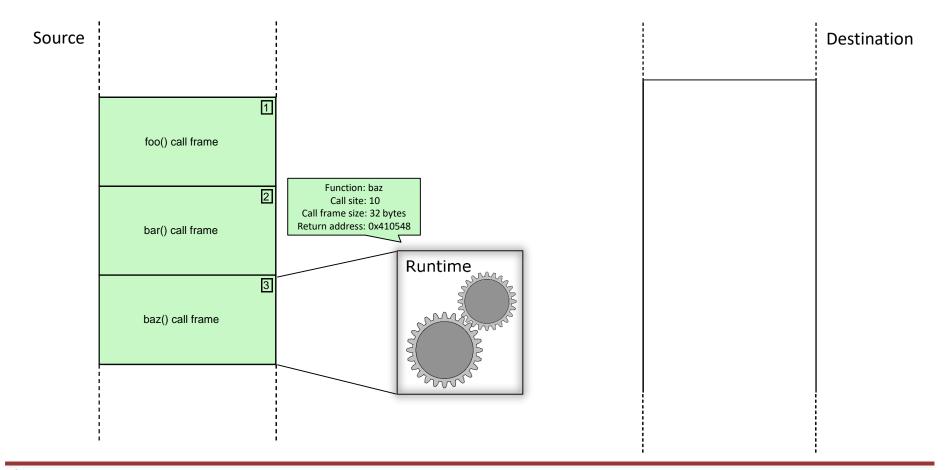






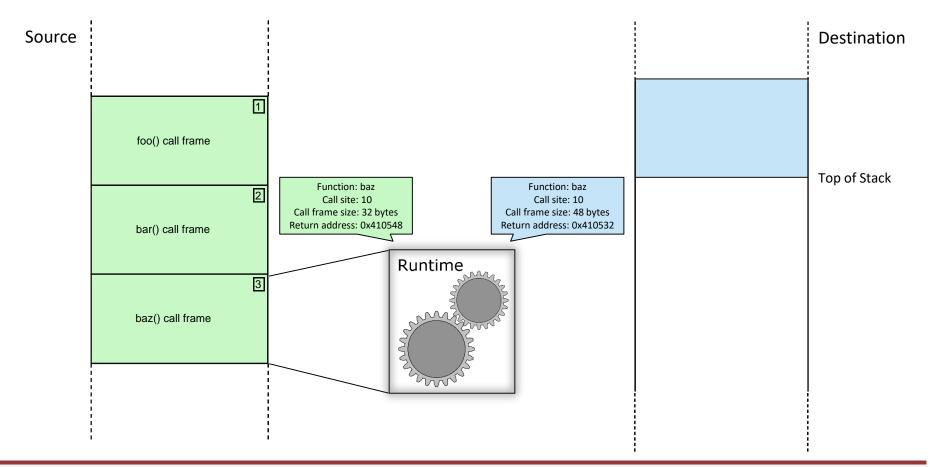






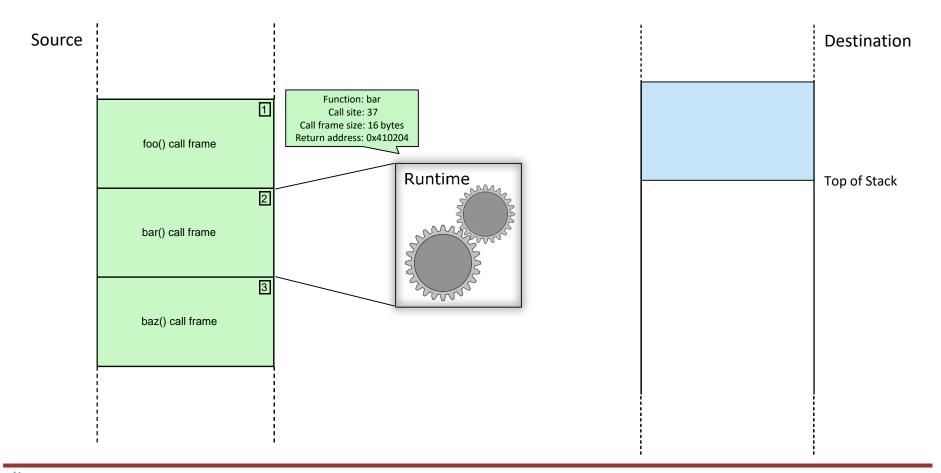






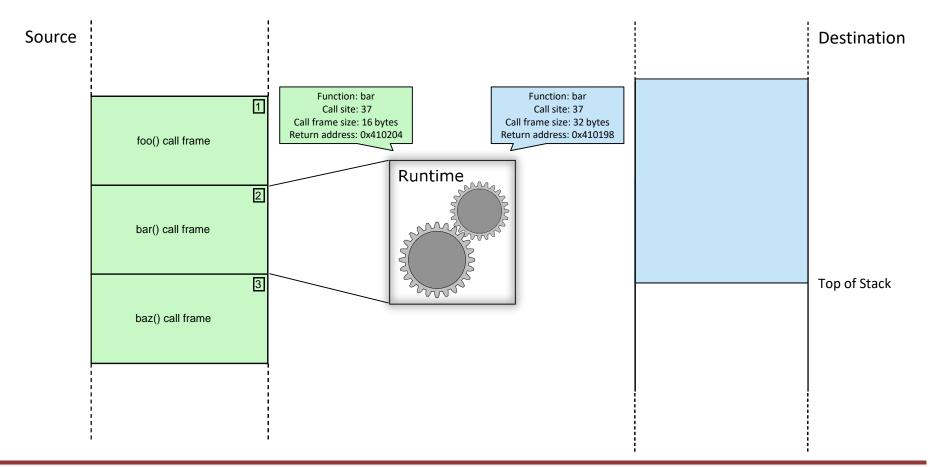






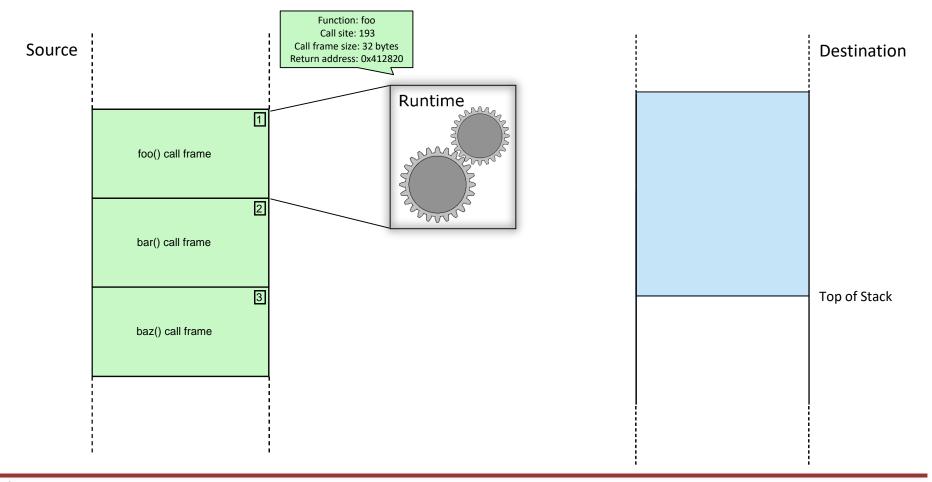






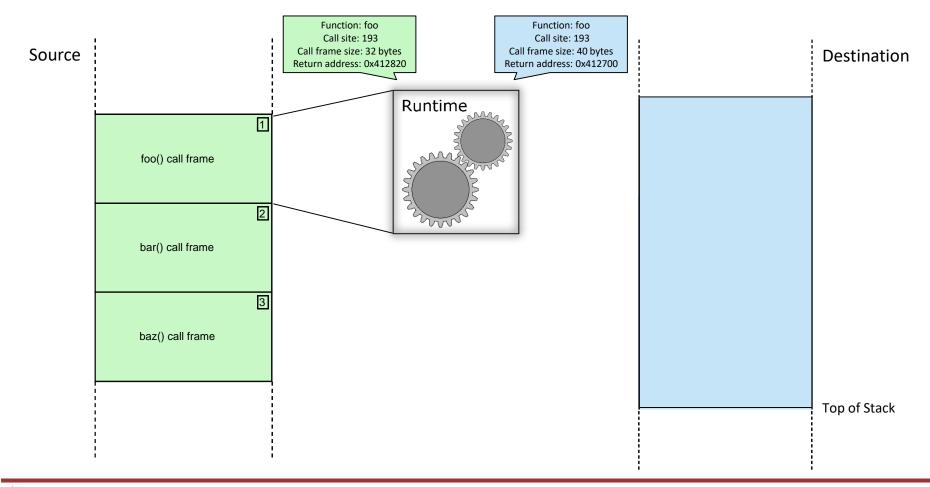






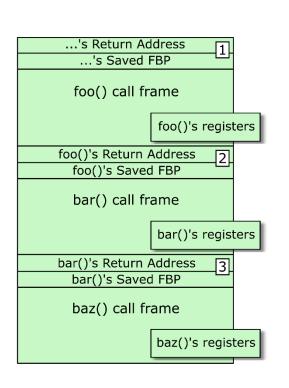


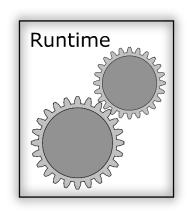


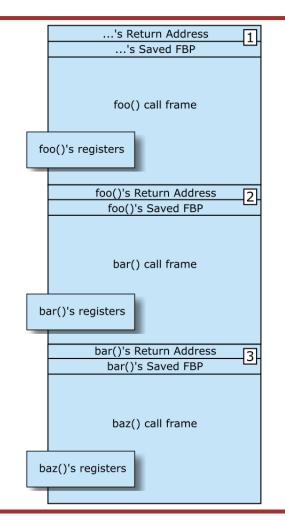






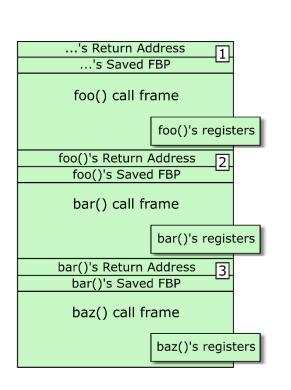


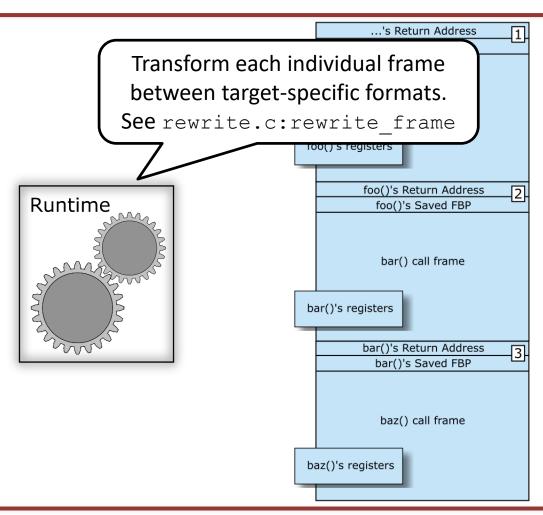






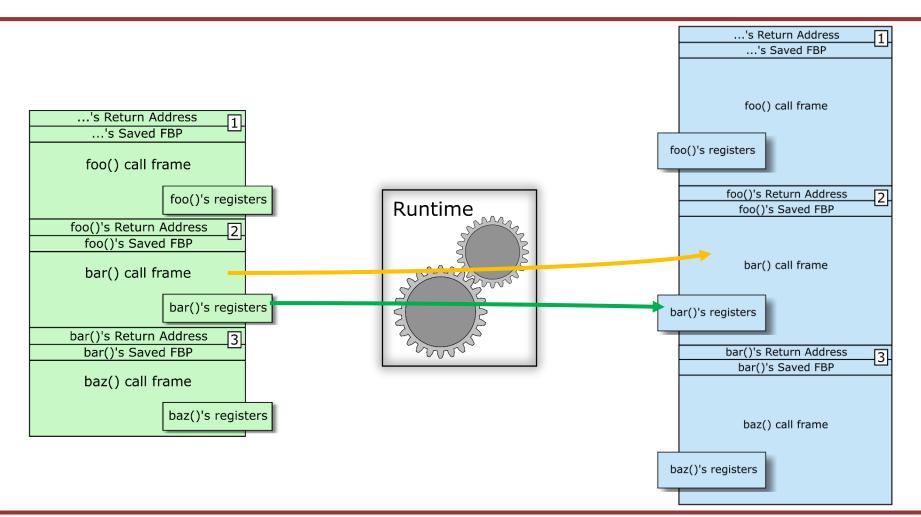






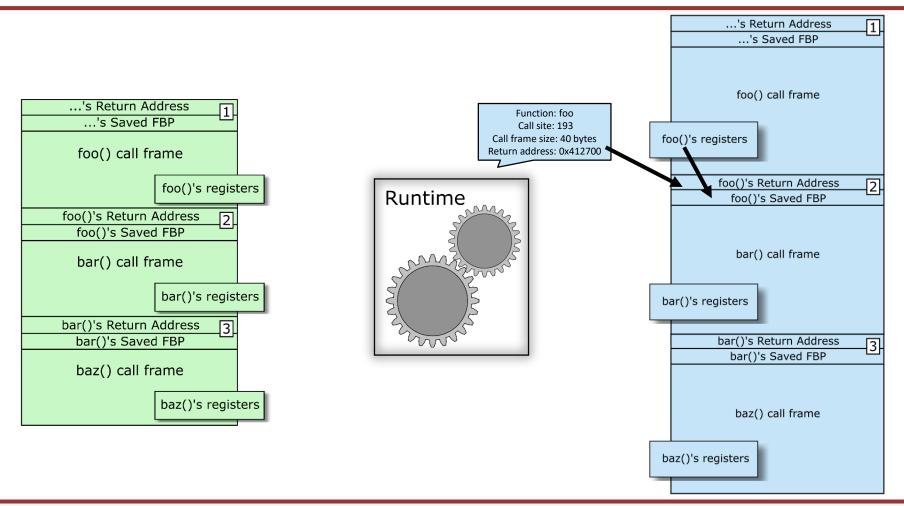






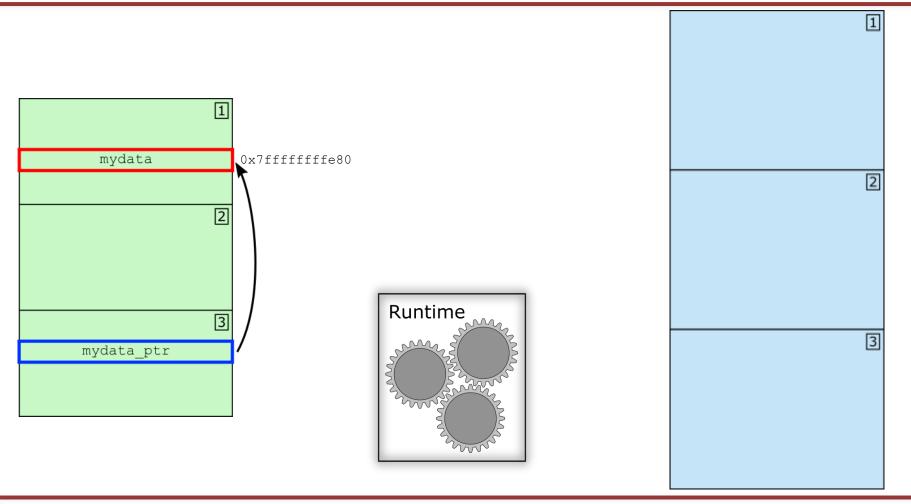






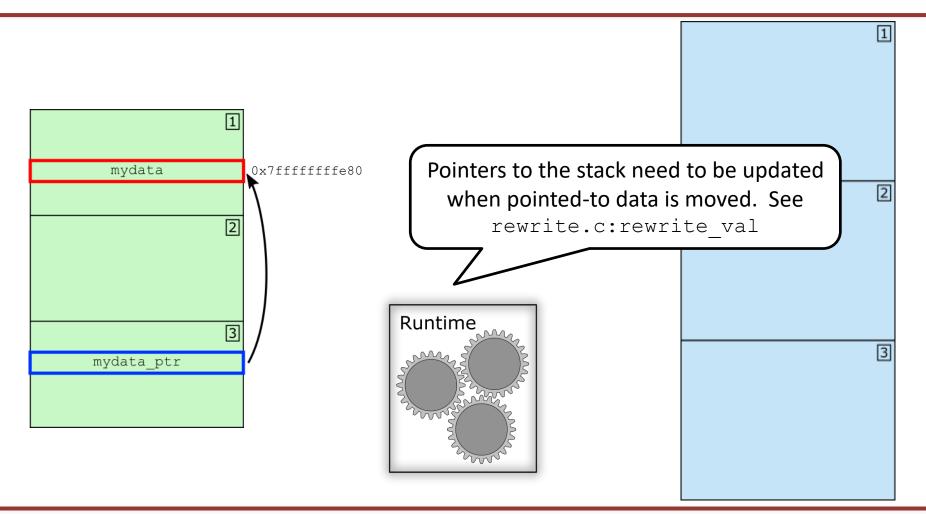






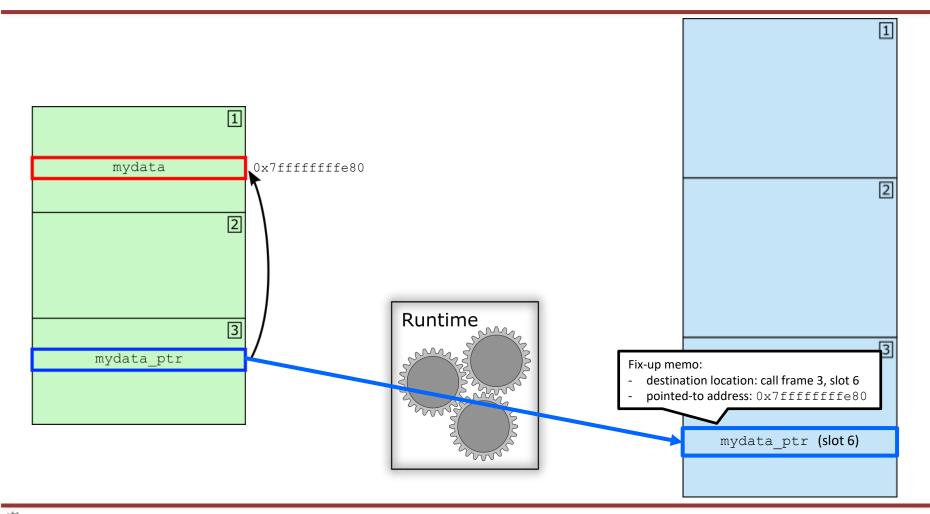






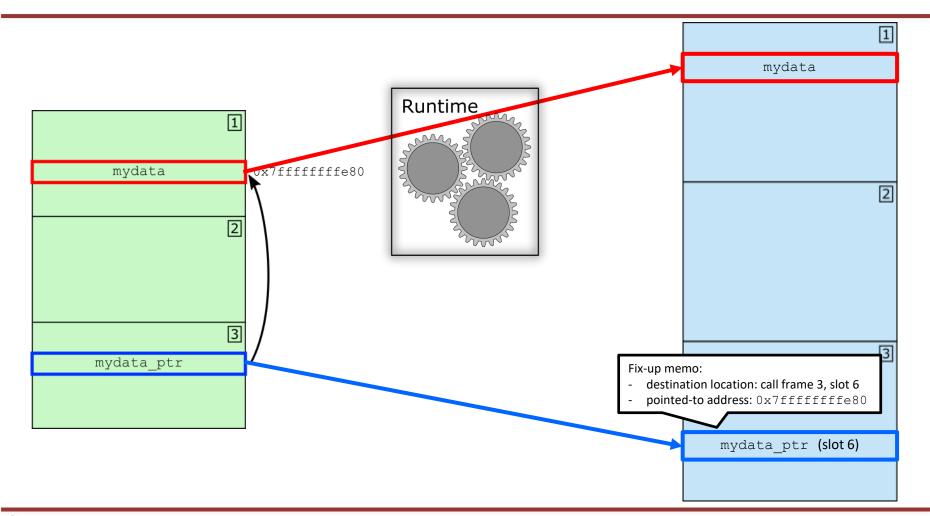






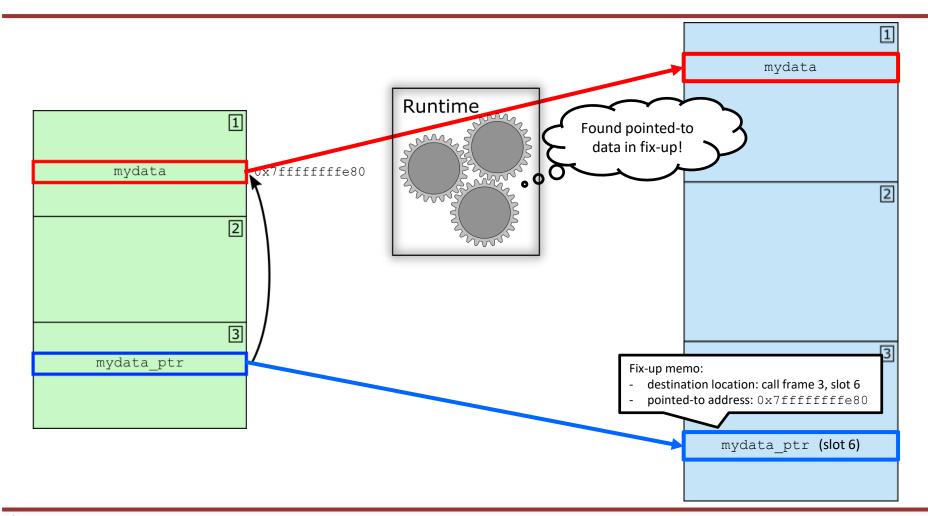






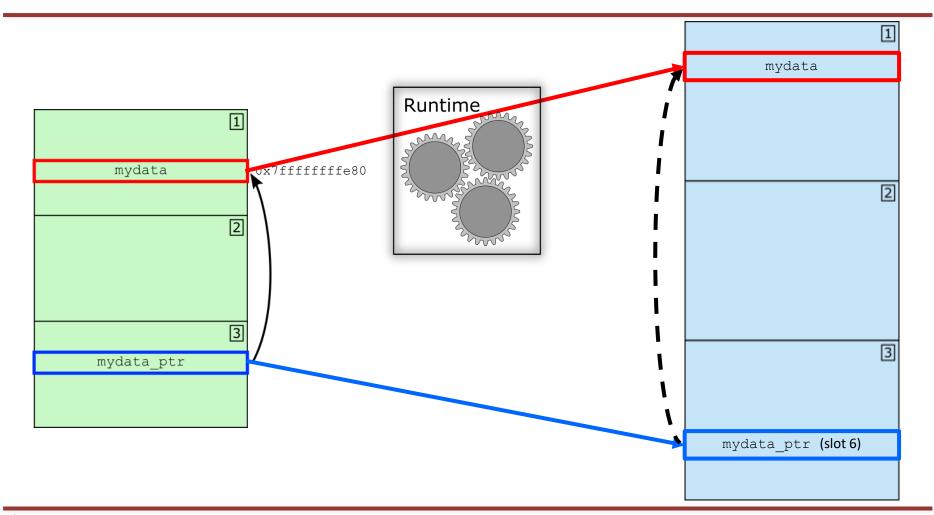
















Runtime Summary

- Migrations are proposed by threads/applications
- Threads check to see if migration is proposed at migration points
- If so, invoke migration procedure
 - Transform thread's register set, stack between target-specific formats
 - Invoke kernel's thread migration service
 - Bootstrap on destination & return to normal execution



