# DRAM Configuration Guide

**TCCxxxx-Android-ALL-V1.00E-DRAM Configuration Guide**

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Telechips

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## Revision History

| Date | Version | Description |
|---|---|---|
| 2010-12-15 | 1.00 | Initial release |
| 2014-03-25 | 1.10 | Update platform |

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# 1. Introduction

This document explains DRAM Configuration of Telechips Android platform.

The user can select couple of types of DRAM verified on the Telechips evaluation board and this document explains how to change the setting values.

The followings are DRAMs which can be selected in the SDK.

| | |
|---|---|
| DDR3 SDRAM | K4B2G1646C HCK0<br>K4B1G1646E HCH9<br>H5TQ2G63BFR H9C<br>H5TQ2G63BFR PBC<br>H5TQ1G83BFR H9C<br>H5TQ2G83BFR H9C<br>H5TQ2G83BFR PBC<br>IN5CB256M8BN CG<br>NT5CB256M8GN CG<br>PRN256M8V89CG8GQF 15E<br>H5TC4G83MFR H9A<br>H5TQ4G83AFR PBC<br>W632GG8KB 12 |

# 2. How to select DRAM

The following is how to select DRAM which has been already added in the Android SDK.
DRAM which can be selected in the SDK is a device tested on the Telechips emulation board.

In the Android SDK, DRAM setting is done in two, the bootloader and kernel.

## 2.1. How to select DRAM on bootloader

In order to select DRAM in the bootlaoder,"***bootable\bootloader\lk\target\tcc8920(x)_evm\rules.mk***" or "***bootable\bootloader\lk\target\tcc893x_evm\rules.mk***"
should be changed as below.

- DRAM Type

```
#TCC_MEM_TYPE := DRAM_DDR2
TCC_MEM_TYPE := DRAM_DDR3   <<- selected
```

- DRAM Size

```
#TCC_MEM_SIZE := 512
TCC_MEM_SIZE := 1024   <<- selected
```

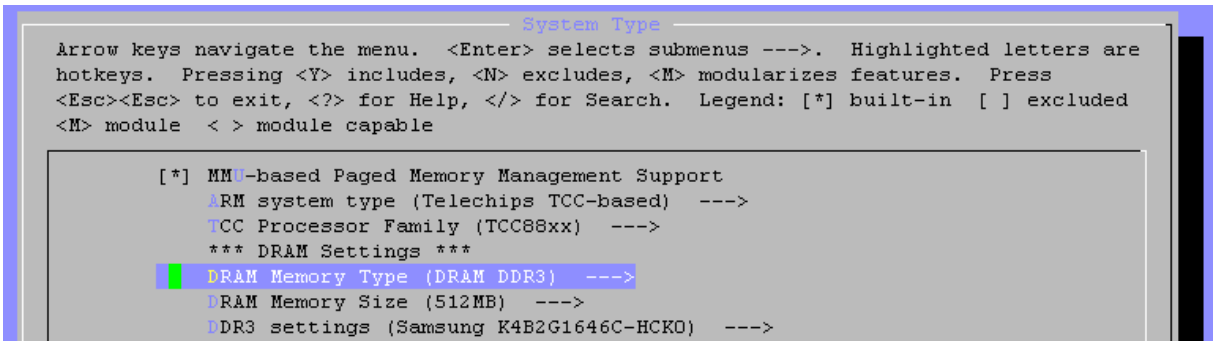
- DRAM Product

```
#DEFINES += CONFIG_DDR3_H5TQ4G83AFR_PBC
#DEFINES += CONFIG_DDR3_H5TC4G83MFR_H9A
#DEFINES += CONFIG_DDR3_H5TQ1G83BFR_H9C
#DEFINES += CONFIG_DDR3_H5TQ2G63BFR_H9C
#DEFINES += CONFIG_DDR3_H5TQ2G63BFR_PBC
#DEFINES += CONFIG_DDR3_H5TQ2G83BFR_H9C
DEFINES += CONFIG_DDR3_H5TQ2G83BFR_PBC    <<- selected
#DEFINES += CONFIG_DDR3_IN5CB256M8BN_CG
#DEFINES += CONFIG_DDR3_K4B1G1646E_HCH9
#DEFINES += CONFIG_DDR3_K4B2G1646C_HCK0
#DEFINES += CONFIG_DDR3_NT5CB256M8GN_CG
#DEFINES += CONFIG_DDR3_PRN256M8V89CG8GQF_15E
```

## 2.2. How to select DRAM on kernel

In order to select DRAM in the kernel, move to ***"kernel\"*** and execute ***make menuconfig.***

Enter into the system type of Memuconfig in order to select DRAM Type, Size, and Product.



# 3. How to change DRAM Configuration

This explains how to change the timing parameter of the selected DRAM.

Both the bootloader and kernel should be changed in the following locations.

| | |
|---|---|
| Bootloader | bootable/bootloader/lk/platform/tcc892x/include/tcc_ddr.h<br>bootable/bootloader/lk/platform/tcc893x/include/tcc_ddr.h |
| kernel | kernel\arch\arm\mach-tcc892x\include\mach\tcc_ddr.h<br>kernel\arch\arm\mach-tcc893x\include\mach\tcc_ddr.h |

These two files are the same. However, since bootloader and kernel are separately built, these files are located in the separate places.

## 3.1. Setting in case of DDR2 SDRAM

In the setting in DDR2 SDRAM, the configuration and access timing parameters of the DRAM can be changed by changing the defined values of ***CONFIG_DRAM_DDR2*** feature in tcc_ddr.h.

The followings are DRAM configuration related defines.

- DDR2_PHYSICAL_CHIP_NUM
  : The number of physical DRAM chips
- DDR2_LOGICAL_CHIP_NUM
  : The number of logical DRAM chips
  If two DRAM chips whose data bit is 16 bit are connected to 32Bit Data Bus of the TCC Memory Controller, the number of logical DRAM is one.
- DDR2_MAX_SPEED
  : It is available max clock speed. In the case of DDR2_800, the clock can be set to 400MHz.
- DDR2_CL
  : CAS Latency
- DDR2_PAGE_SIZE
  : Page size
- DDR2_BURST_LEN
  : Burst length
- DDR2_READ_BURST_TYPE
  : Read burst type
- DDR2_EA_MB_SIZE
  : The size of each chip (MByte unit)
- DDR2_TOTAL_MB_SIZE
  : Total size of entire chip (MByte unit)
- DDR2_ROWBITS
  : The number of row address bits
- DDR2_COLBITS
  : The number of column address bits
- DDR2_BANK_BITS
  : The number of bank address bits
- DDR2_BANK_NUM
  : The number of banks
- DDR2_PHYSICAL_DATA_BITS
  : The number of physical data bits
- DDR2_LOGICAL_DATA_BITS
  : The number of logical data bits
  If two DRAM chips whose data bit is 16 bit are connected to 32Bit Data Bus of the TCC Memory Controller, the number of logical data bit is 32.

The followings are DRAM access timing parameter related defines.

- DDR2_tRFC_ps
  : The auto-refresh command time (pico sec unit)
- DDR2_tREFI_ps
  : Average periodic refresh interval (pico sec unit)
- DDR2_tRRD_ps
  : Active bank x to Active bank y delay (pico sec unit)
- DDR2_tRRD_ck
  : Minimum required clock for tRRD (nCK unit)
- DDR2_tRAS_ps
  : RAS to pre-charge delay (pico sec unit)
- DDR2_tRAS_ck
  : Minimum required clock for tRAS (nCK unit)
- DDR2_tRC_ps
  : Active bank x to Active bank x delay (pico sec unit)
- DDR2_tRC_ck
  : Minimum required clock for tRC (nCK unit)
- DDR2_tRCD_ps
  : RAS to CAS minimum delay (pico sec unit)
- DDR2_tRCD_ck
  : Minimum required clock for tRCD (nCK unit)
- DDR2_tRP_ps
  : Pre-charge to RAS delay (pico sec unit)
- DDR2_tRP_ck
  : Minimum required clock for tRP (nCK unit)
- DDR2_tWTR_ps
  : Write to read delay (pico sec unit)
- DDR2_tWTR_ck
  : Minimum required clock for tWTR (nCK unit)
- DDR2_tWR_ps
  : Write to pre-charge delay (pico sec unit)
- DDR2_tWR_ck
  : Minimum required clock for tWR (nCK unit)
- DDR2_tRTP_ps
  : Read to pre-charge delay (pico sec unit)
- DDR2_tRTP_ck
  : Minimum required clock for tRTP (nCK unit)
- DDR2_tFAW_ps
  : Four bank activate time (pico sec unit)
- DDR2_tFAW_ck
  : Minimum required clock for tFAW (nCK unit)
- DDR2_tXSR_ck
  : Self refresh exit power down to next valid command delay (nCK unit)
- DDR2_tXP_ck
  : Exit power down to next valid command delay (nCK unit)
- DDR2_tCKE_ck
  : CKE minimum pulse width (nCK unit)
- DDR2_tMRD_ck
  : Mode register set command period (nCK unit)

## 3.2. Setting in case of DDR3 SDRAM

In the setting in DDR3 SDRAM, the configuration and access timing parameters of the DRAM can be changed by changing the defined values of ***CONFIG_DRAM_DDR3*** feature in tcc_ddr.h.

The followings are DRAM configuration related defines.

- DDR3_PHYSICAL_CHIP_NUM
  : The number of physical DRAM chips
- DDR3_LOGICAL_CHIP_NUM
  : The number of logical DRAM chips
  If two DRAM chips whose data bit is 16 bit are connected to 32Bit Data Bus of the TCC Memory Controller, the number of logical DRAM is one.
- DDR3_MAX_SPEED
  : It is available max clock speed.
- DDR3_CL
  : CAS Latency
- DDR3_AL
  : Additive Latency
- DDR3_PAGE_SIZE
  : Page size
- DDR3_BURST_LEN
  : Burst length
- DDR3_READ_BURST_TYPE
  : Read burst type
- DDR3_EA_MB_SIZE
  : The size of each chip (MByte unit)
- DDR3_TOTAL_MB_SIZE
  : Total size of entire chip (MByte unit)
- DDR3_ROWBITS
  : The number of row address bits
- DDR3_COLBITS
  : The number of column address bits
- DDR3_BANK_NUM
  : The number of banks

The followings are DRAM access timing parameter related defines.

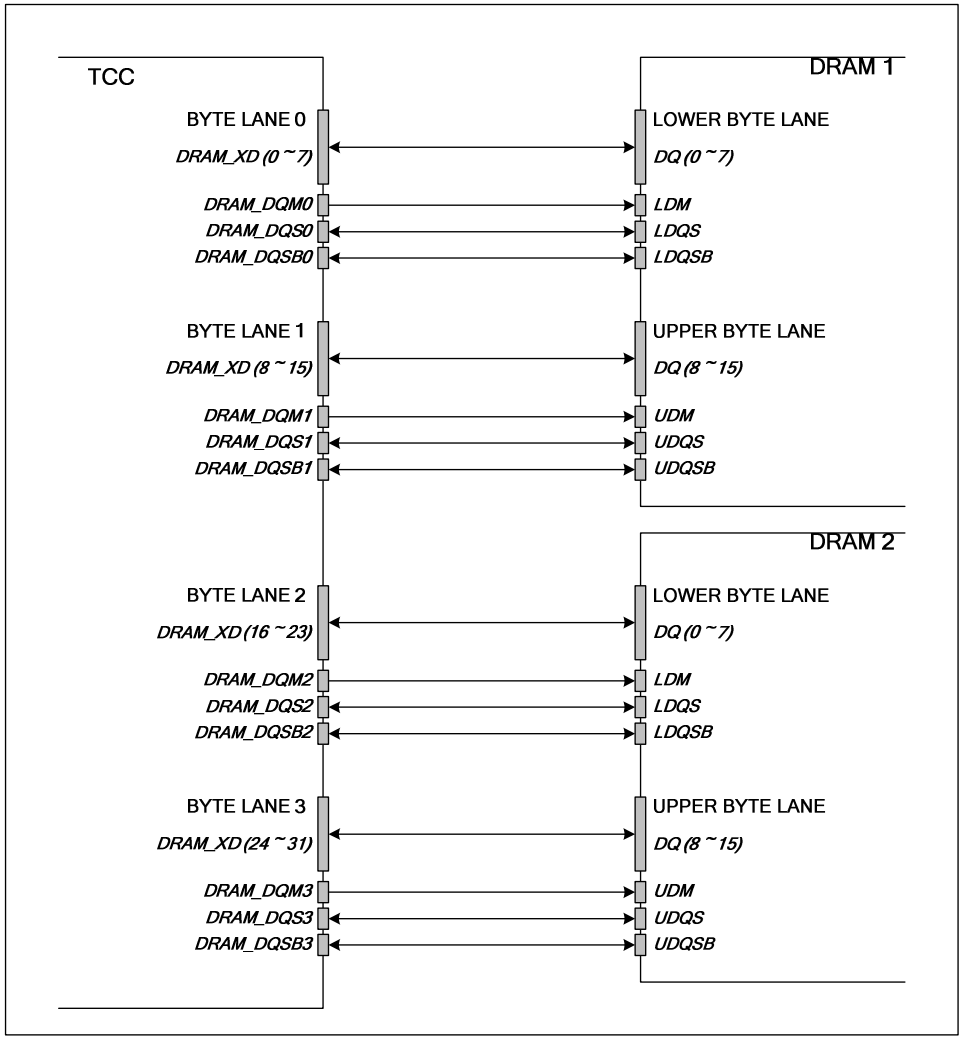
- DDR3_tRFC_ps
  : The auto-refresh command time (pico sec unit)
- DDR3_tREFI_ps
  : Average periodic refresh interval (pico sec unit)
- DDR3_tRCD_ps
  : RAS to CAS minimum delay (pico sec unit)
- DDR3_tRCD_ck
  : Minimum required clock for tRCD (nCK unit)
- DDR3_tRP_ps
  : Pre-charge to RAS delay (pico sec unit)
- DDR3_tRP_ck
  : Minimum required clock for tRP (nCK unit)
- DDR3_tRC_ps
  : Active bank x to Active bank x delay (pico sec unit)
- DDR3_tRC_ck
  : Minimum required clock for tRC (nCK unit)
- DDR3_tRAS_ps
  : RAS to pre-charge delay (pico sec unit)
- DDR3_tRAS_ck
  : Minimum required clock for tRAS (nCK unit)

- DDR3_tRTP_ps
  : Read to pre-charge delay (pico sec unit)
- DDR3_tRTP_ck
  : Minimum required clock for tRTP (nCK unit)
- DDR3_tWTR_ps
  : Write to read delay (pico sec unit)
- DDR3_tWTR_ck
  : Minimum required clock for tWTR (nCK unit)
- DDR3_tWR_ps
  : Write to pre-charge delay (pico sec unit)
- DDR3_tWR_ck
  : Minimum required clock for tWR (nCK unit)
- DDR3_tRRD_ps
  : Active bank x to Active bank y delay (pico sec unit)
- DDR3_tRRD_ck
  : Minimum required clock for tRRD (nCK unit)
- DDR3_tFAW_ps
  : Four bank activate time (pico sec unit)
- DDR3_tFAW_ck
  : Minimum required clock for tFAW (nCK unit)
- DDR3_tXS_ps
  : Exit self-refresh to command not requiring a locked DLL (pico sec unit)
- DDR3_tXS_ck
  : Minimum required clock for tXS (nCK unit)
- DDR3_tXP_ps
  : DLL on, any valid command, or DLL off to commands not requiring locked DLL (pico sec unit)
- DDR3_tXP_ck
  : Minimum required clock for tXP (nCK unit)
- DDR3_tCKE_ps
  : CKE minimum pulse width (pico sec unit)
- DDR3_tCKE_ck
  : Minimum required clock for tCKE (nCK unit)
- DDR3_tMRD_ck
  : Mode register set command period (nCK unit)

## 4. Example

This is the example of Hynix DDR3 SDRAM H5TQ2G63BFR PBC Memory setting with the above defines.

In the case of this memory, physically two chips are used. However, logically it is like one chip is used with the below H/W configuration.



The followings are the setting values with the above H/W configuration.

```
/*-----------------------------------------------------------------------------
 DDR3 Configuation
-----------------------------------------------------------------------------*/
#define DDR3_PINMAP_TYPE              0
#if defined(CONFIG_TCC_MEM_1024MB)
#define DDR3_LOGICAL_CHIP_NUM          2  // 1024MB(256MBx4 2CS)
#else
#define DDR3_LOGICAL_CHIP_NUM          1  // 512MB(256MBx2 1CS)
#endif
#define DDR3_MAX_SPEED         DDR3_1600
#define DDR3_CL                     11
#define DDR3_AL              AL_DISABLED
#define DDR3_BURST_LEN              BL_8
#define DDR3_READ_BURST_TYPE RBT_SEQUENTIAL
#define DDR3_EA_BIT_SIZE       SIZE_2GBIT
#define DDR3_TOTAL_MB_SIZE           (512*DDR3_LOGICAL_CHIP_NUM)
#define DDR3_ROWBITS                14
#define DDR3_COLBITS                10
#define DDR3_BANKBITS                3
#define DDR3_APBIT                  10

/*-----------------------------------------------------------------------------
 DDR3 Access Timing Parameters
-----------------------------------------------------------------------------*/
#define DDR3_tRFC_ps              160000
#define DDR3_tREFI_ps            7800000
#define DDR3_tRCD_ps              13750
#define DDR3_tRCD_ck                  1
#define DDR3_tRP_ps               13750
#define DDR3_tRP_ck                   1
#define DDR3_tRC_ps               48750
#define DDR3_tRC_ck                   1
#define DDR3_tRAS_ps              35000
#define DDR3_tRAS_ck                  1
#define DDR3_tRTP_ps               7500
#define DDR3_tRTP_ck                  4
#define DDR3_tWTR_ps               7500
#define DDR3_tWTR_ck                  4
#define DDR3_tWR_ps               15000
#define DDR3_tWR_ck                   1
#define DDR3_tRRD_ps               7500
#define DDR3_tRRD_ck                  5
#define DDR3_tFAW_ps              40000
#define DDR3_tFAW_ck                 30
#define DDR3_tXS_ps    (DDR3_tRFC_ps+10000)
#define DDR3_tXS_ck                   5
#define DDR3_tXP_ps                6000
#define DDR3_tXP_ck                   3
#define DDR3_tCKE_ps               5000
#define DDR3_tCKE_ck                  3
#define DDR3_tMRD_ck                  4
#define DDR3_tCCD_ck                  4
#define DDR3_tRAS_MAX_ps  (DDR3_tREFI_ps*9)
#define DDR3_tMOD_ps              15000
#define DDR3_tMOD_ck                 12
#define DDR3_tDLLK_ck               512
#define DDR3_tXPDLL_ps             24000
```

**EXAMPLE**

```
#define DDR3_tXPDLL_ck                10
#define DDR3_tXSDLL_ck      DDR3_tDLLK_ck
#define DDR3_tCKSRX_ps             10000
#define DDR3_tCKSRX_ck                5
#define DDR3_tCKSRE_ps             10000
#define DDR3_tCKSRE_ck                5
#define DDR3_tZQCS_ck                64
#define DDR3_tZQINIT_ck             512
#define DDR3_tZQOPER_ck             256
```