Roll No.:…….....

National Institute of Technology, Delhi

Name of the Examination: B.Tech.

End Semester Lab Examination (Spring, 2020)

Branch	**: ECE**	**Semester**	**: 6th**
Title of the Course	**:Basics of VLSI**	**Course Code**	**: ECB 351**

Time: 2 Hours **Maximum Marks: 50**

Note:1. All questions are compulsory.

2. Each question carries 1 mark.

3. Write the answer in one word or a maximum one line.

Q1. Write the full form ofVHDL.

Q2. The process of transforming a design entry information of the circuit into a set of logic equations in any EDA tool is known as _____

Q3. If A and B are two STD_LOGIC_VECTOR input signals, then legal assignment for A AND B is_____

Q4. Which kind of modeling is used in the following description?

```
ARCHITECTUREmy_archOFmy_designIS
BEGIN
c<= a OR b;
ENDmy_arch;
```

Q5. A user has designed JK flip flop by using the VHDL code. The output is continuously switching between 0 and 1. This condition is known as _____

Q6. What does RTL in digital circuit design stand for?

Q7. What is the full form of EDA?

Q8. How many logical operations are required to implement a Boolean function XY + X?

Q9. Can an entity have more than one architecture?

Q10. In a statement containing two or more operators of the same precedence, how the expression will be solved?

Q11. Does XNOR is a logical operator in VHDL?

Q12. _____ modeling uses logic gates and basic blocks to describe the functionality of the system.

Q13. Component instantiation is the part of _____ modeling.

Q14. Which logic function is described in the code given below?

```
ARCHITECTUREmy_funcOFmy_logicIS
begin
process(a, b, y)
begin
IF(a = '0' and b = '0')THEN
y <= '0';
ELSIF(a = '1' and b= '1')THEN
y<= '0';
ELSE y <= '1';
ENDif;
ENDprocess;
ENDmy_func;
```

Q15. Which modeling style does the following code represents?

```
Architecturemy_logicOFlogic_funcIS
Component gate_1
PORT(b1, b2 :INBIT;
s :OUTBIT);
ENDcomponent;
Component gate_2 IS
PORT(b1,b2 :INBIT;
C :OUTBIT);
ENDcomponent;
SIGNAL a, b, sum, carry :BIT;
begin
EXOR : gate_1 portmap(a, b, sum);
AND: gate_2 portmap(a,b ,carry);
ENDmy_logic
```

Q16. What is the use of a function called a port map()?

Q17. The operator '&' is called the_____ operator.

Q18. The operators like =, /=, <, >, >= are called _____

Q19. _____ operator is unary as well as a binary operator.

Q20. The code given below is a VHDL implementation of _____

```
ARCHITECTUREmy_circuitOFmy_logicIS
BEGIN
WITH ab SELECT
y <= x0 WHEN "00";
      x1 WHEN "01";
      x2 WHEN "10";
      x3 WHEN "11";
ENDmy_circuit;
```

Q21. A 4 to 16 decoder can be used as a code converter. What will be the inputs and outputs of the converter, respectively?

Q22. If only two-bit vectors are allowed to use in the VHDL code, then how many numbers of MUX will be required to implement 4 to 1 MUX?

Q23. What will be the value of count output, if the data din is 11001111?

```
ENTITYmy_logicIS
PORT(din :STD_LOGIC_VECTOR(7DOWNTO0);
Count :STD_LOGIC_VECTOR(3DOWNTO0));
ENDmy_logic;
ARCHITECTURE behavior OFmy_logicIS
BEGIN
Count <= "0000"
PROCESS(din)
BEGIN
L1:FORiIN0TO7LOOP
IF(din(i)= '1')THEN
Count = count+1;
```

```
ELSE
NEXT L1;
ENDLOOP;
ENDPROCESS;
END behavior;
```

Q24. Write the Boolean equivalent for the expression A + AB.

Q25. Transfer of one bit of information at a time is called _____

Q26. How many types of shift operators are there in VHDL?

Q27. In _____ counter universal clock is not used.

Q28. List out the Modes for Port in VHDL?

Q29. Write down the signal assignment operator.

Q30. List the three classes of data objects in VHDL.

Q31. What are composite data types?

Q32. List four different types of scalar data types in VHDL.

Q33. List all logical operators in VHDL.

Q34. In VHDL, exponentiation operator is defined by the symbol _____

Q35. What is the significance of the **wait** statement in VHDL?

Q36. In which part of the VHDL code, components must be declared?

Q37. Canthe ports of a componentbe left unconnected in VHDL?

Q38. Refer to the architecture given below, there are two outputs called x and y. The structure defined is a full adder circuit. Which of the outputs corresponds to sum output of the adder?

```
ARCHITECTURE arch1 OF design IS
COMPONENT xor2 IS
PORT(i1, i2 :INSTD_LOGIC;
o :OUTSTD_LOGIC);
ENDCOMPONENT;
COMPONENT and2 IS
PORT(a1, a2 :INSTD_LOGIC;
P :OUTSTD_LOGIC);
ENDCOMPONENT;
COMPONENT or2 IS
```

```
PORT(d1, d2 :INSTD_LOGIC;
r :OUTSTD_LOGIC);
ENDCOMPONENT;
SIGNAL s1, s2, s3, s4, s5 :STD_LOGIC;
BEGIN
X1: xor2 PORTMAP(a, b, s1);
X2 : xor2 PORTMAP(s1, c, y);
X3: and2 PORTMAP(a, b, s2);
X4 : and2 PORTMAP(a, c, s3);
X5: and2 PORTMAP(b, c, s4);
X6: or2 PORTMAP(s2, s3, s5);
X7: or2 PORTMAP(s4, s5, x);
END arch1;
```

Q39. Refer to the code given below, which type of modeling is used to describe the system?

```
ARCHITECTURE and_1 OFand_gateIS
begin
process(a, b, y)
begin
IF(a = '1' and b = '1')THEN
y <= '1';
ELSE y <='0';
endIF;
ENDprocess;
END and_1;
```

Q40. The signal assignment is considered as a _____ statement.

Q41. Write down the symbol for variable assignment statement.

Q42. Does order of statements matter in concurrent assignment?

Q43. In the signal assignment statement, which delay is used?

```
x <=1AFTER 10ns
```

Q44. If there is more than one process in a VHDL code, how they are executed?

Q45. If no signal in the sensitivity list is changed, then how many times the process will be executed?

Q46. Refer to the code given below, what kind of circuit is designed?

```
SIGNALx :INBIT;
SIGNALy :OUTBIT;
SIGNALclk:INBIT;
PROCESS(clk)
BEGIN
IF(clk'EVENTandclk= '1')
y ;&lt= x;
ENDPROCESS
```

Q47. What logic is described in the following logic?

```
PROCESS(a, b)
IF(a = '1' AND b = '0' OR a= '0' AND b = '1')THEN
y &lt;= '1';
ELSIF(a = '1' AND b= '1')THEN
y &lt;= '0';
ELSE
 y &lt;= '0';
ENDIF
```

Q48. How many styles of loop statement does the VHDL have?

Q49. **FOR** loop uses a loop index, the type of loop index is _____

Q50. A for loop is initiated as given below, in total how many iterations will be there for the FOR loop?

```
FORiIN0TO5LOOP
```

******* End of Question Paper*****