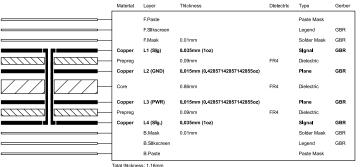
Top Fabrication (Scale 1:1)

Layer Stack Legend Stackup: JLC04121H-7628



Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
USB	90	±10 %	L1	0.17	0.275	L2



All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

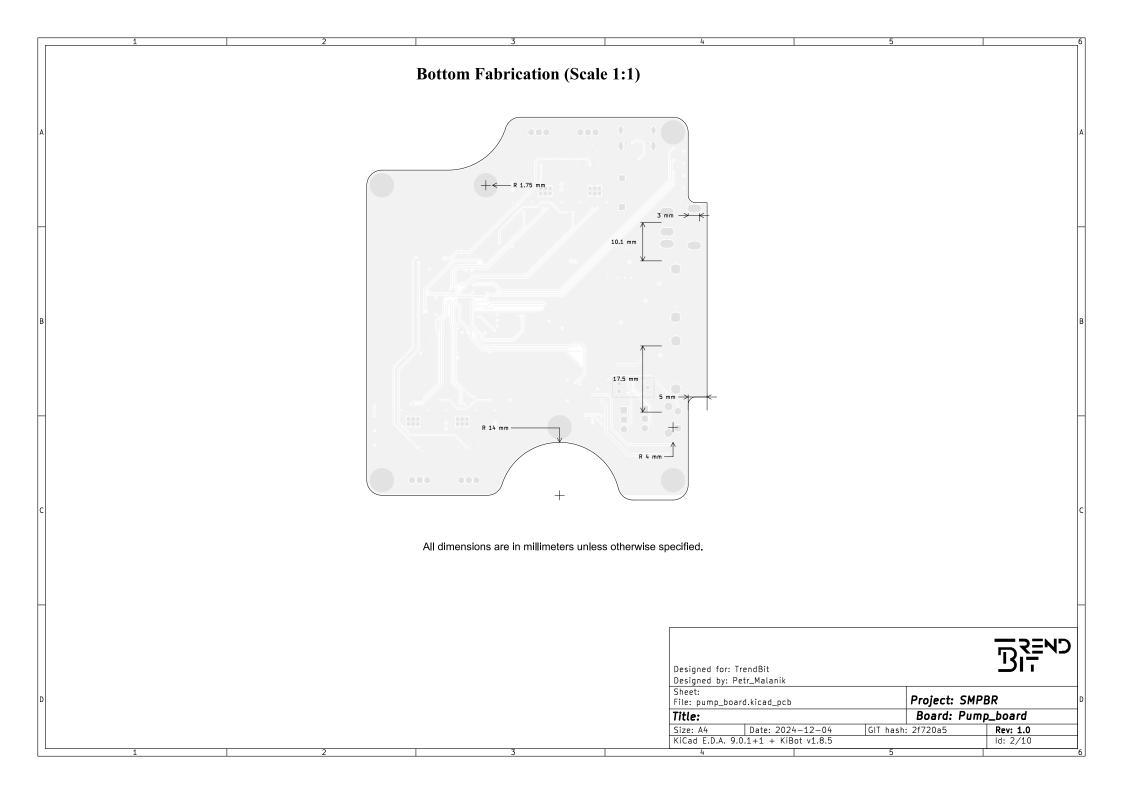
SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

- 4) SURFACE FINISH: ENIG
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Ph FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:
- A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
- B. Tg 170 C OR EQUIVALENT.
- C. EQUIVALENT MATERIAL SHALL BE ROHS COMPLIANT, HALOGEN FREE AND APPROVED BY TRENDBIT.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE 90.000 × 101.250 mm BOARD THICKNESS 1.160 mm TRACE WIDTH 0.170 mm TRACE TO TRACE -0.000 mm MIN. HOLE (PTH) 0.300 mm MIN. HOLE (NPTH) 0.650 mm ANNULAR RING 0.075 mm COPPER TO HOLE 0.150 mm COPPER TO EDGE 0.300 mm 0.250 mm HOLE TO HOLE

- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

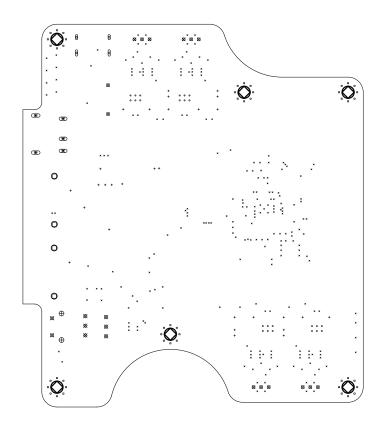
Designed for: TrendBit Designed by: Petr_Malaník Sheet: Project: SMPBR File: pump_board.kicad_pcb Board: Pump_board Title: Size: A4 Date: 2024-12-04 GIT hash: 2f720a5 Rev: 1.0 KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5 ld: 1/10



Drill Drawing L1 - L4 (Scale 1:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	250	0.30mm (11.81mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Via
0	24	0.33mm (12.99mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
+	29	0.50mm (19.69mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Vla
0	48	0.50mm (19.69mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
⋄	4	0.60mm (23.62mlls)	PTH	Slot	L1 (Slg) - L4 (Slg,)	Pad
×	14	0.80mm (31.50mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
*	5	0.90mm (35.43mlls)	PTH	Slot	L1 (Slg) - L4 (Slg,)	Pad
×	2	0.99mm (38.98mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
×	6	1.00mm (39.37mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
⊕	2	1.30mm (51.18mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
0	4	1.60mm (62.99mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
٥	6	3,20mm (125,98mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
	Total 394					



Designed for: Tre Designed by: Pet				BIT	
Sheet: File: pump_board	d.kicad_pcb		Project: SMP	BR	D
Title:			Board: Pum	p_board	
Size: A4	Date: 2024-12-04	GIT hash	: 2f720a5	Rev: 1.0	
KiCad E.D.A. 9.0	.1+1 + KiBot v1.8.5			ld: 3/10	

