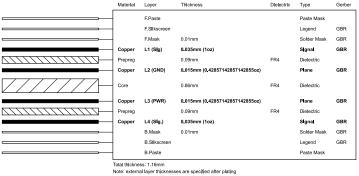
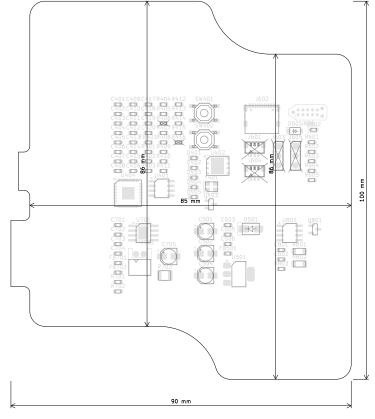
Top Fabrication (Scale 1:1)

Layer Stack Legend Stackup: JLC04121H-7628



Impedance Table

	Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
I	USB	90	±10 %	L1	0.17	0.275	L2



All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY

 SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

- 4) SURFACE FINISH: ENIG
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
- SILK SCREEN LEGEND TO BE APPLIED PER LAYER
 STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK,
- ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS
 AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:
- A. FLAMMABILITY RATING MUST MEET OR EXCEED
- UL94V-0 REQUIREMENTS. B. Tg 170 C OR EQUIVALENT.
- C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY TRENDBIT.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE 90.000 × 100.000 mm BOARD THICKNESS 1.160 mm TRACE WIDTH N/A mm TRACE TO TRACE 0.100 mm MIN. HOLE (PTH) 0.350 mm MIN. HOLE (NPTH) 0.650 mm ANNULAR RING 0.140 mm 0.150 mm COPPER TO HOLE COPPER TO EDGE 0.300 mm 0.250 mm HOLE TO HOLE

- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

