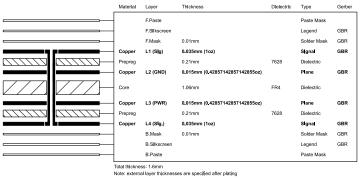
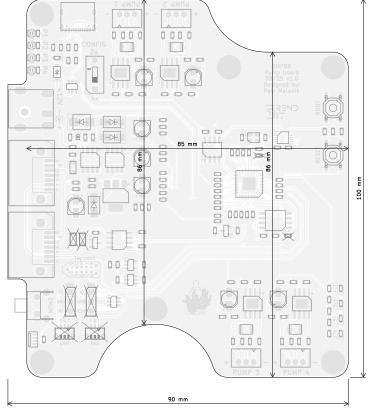
## **Top Fabrication (Scale 1:1)**

#### **Layer Stack Legend Stackup: JLC04161H-7628**



# **Impedance Table**

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
USB	90	±10 %	L1	0.17	0.275	L2



All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.

DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

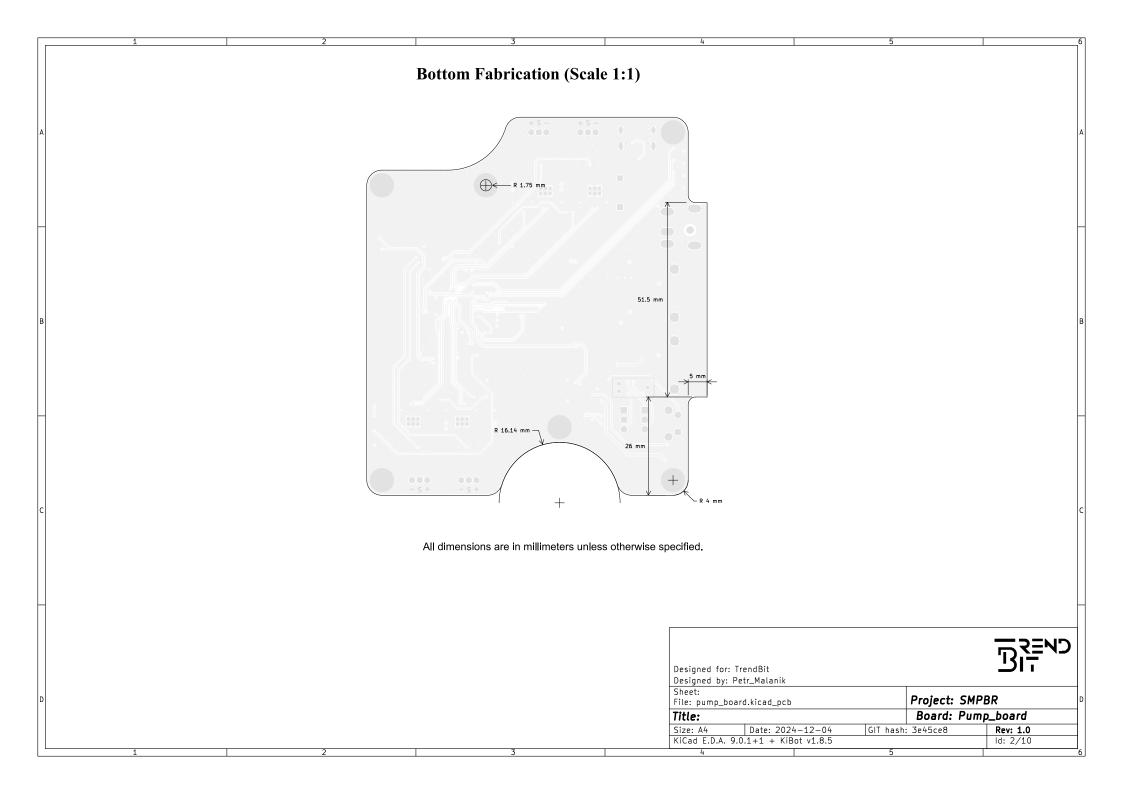
> SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

- 4) SURFACE FINISH: ENIG
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Ph FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:
- A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
- B. Tg 170 C OR EQUIVALENT.
- C. EQUIVALENT MATERIAL SHALL BE ROHS COMPLIANT, HALOGEN FREE AND APPROVED BY TRENDBIT.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE 90.000 × 100.000 mm BOARD THICKNESS 1.600 mm TRACE WIDTH 0.170 mm TRACE TO TRACE -0.000 mm MIN. HOLE (PTH) 0.300 mm MIN. HOLE (NPTH) 0.650 mm ANNULAR RING 0.075 mm COPPER TO HOLE 0.150 mm COPPER TO EDGE 0.300 mm 0.250 mm HOLE TO HOLE

- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

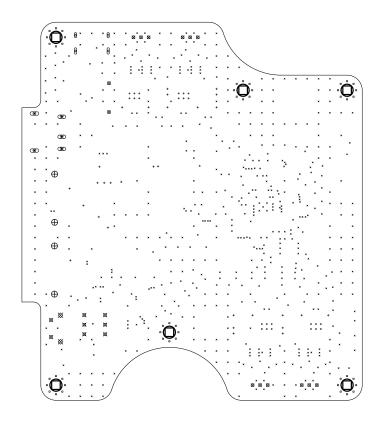
Designed for: TrendBit Designed by: Petr\_Malaník Sheet: Project: SMPBR File: pump\_board.kicad\_pcb Board: Pump\_board Title: Size: A4 Date: 2024-12-04 GIT hash: 3e45ce8 Rev: 1.0 KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5 ld: 1/10



# **Drill Drawing L1 - L4 (Scale 1:1)**

### **Drill Table**

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	639	0.30mm (11.81mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Via
0	24	0.30mm (11.81mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
+	30	0.50mm (19.69mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Vla
	48	0.50mm (19.69mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
<b>⋄</b>	4	0.60mm (23.62mlls)	PTH	Slot	L1 (Slg) - L4 (Slg,)	Pad
Ø	14	0.80mm (31.50mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
*	5	0.90mm (35.43mlls)	PTH	Slot	L1 (Slg) - L4 (Slg,)	Pad
×	8	1.00mm (39.37mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
*	2	1.30mm (51.18mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
<b>⊕</b>	4	1.60mm (62.99mlls)	PTH	Round	L1 (Slg) - L4 (Slg,)	Pad
0	6	3.20mm (125.98mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
	Total 784					



Designed for: TrendBit
Designed by: Petr\_Malaník

Sheet:
File: pump\_board.kicad\_pcb

Title:

Size: A4 | Date: 2024-12-04 | GIT hash: 3e45ce8 | Rev: 1.0 |
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5 | Id: 3/10

