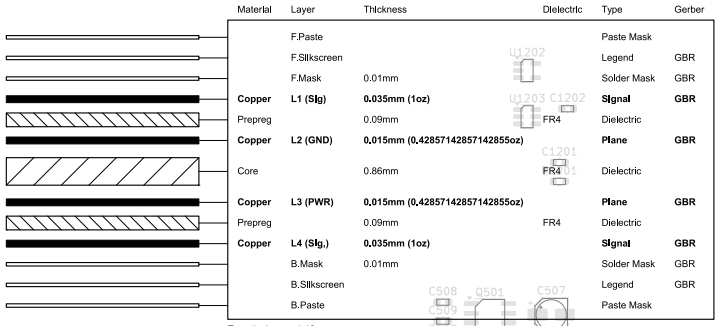
Top Fabrication (Scale 1:1)

Layer Stack Legend Stackup: JLC04121H-7628

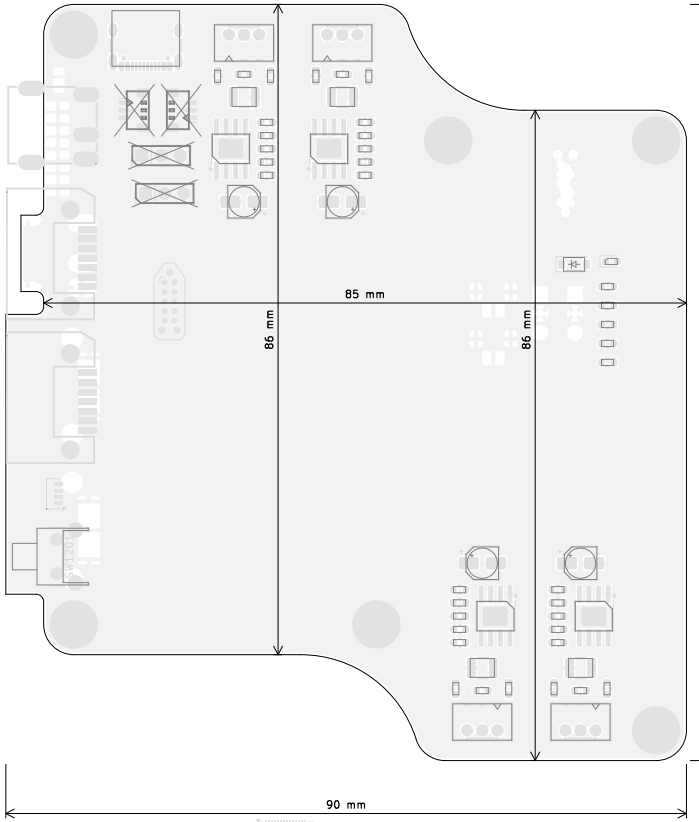


Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste			Paste Mask	
	F.Silkscreen			Legend	GBR
	F.Mask	0.01mm		Solder Mask	GBR
Copper	L1 (Sig)	0.035mm (1oz)		Signal	GBR
Prepreg		0.09mm	FR4	Dielectric	
Copper	L2 (GND)	0,015mm (0,42857142857142855oz)		Plane	GBR
Core		0.86mm	FR4	Dielectric	
Copper	L3 (PWR)	0,015mm (0,42857142857142855oz)		Plane	GBR
Prepreg		0.09mm	FR4	Dielectric	
Copper	L4 (Sig,)	0.035mm (1oz)		Signal	GBR
	B.Mask	0.01mm		Solder Mask	GBR
	B.Silkscreen			Legend	GBR
	B.Paste			Paste Mask	

Total thickness: 1.16mm
Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
USB	90	±10 %	L1	0.17	0.275	L2



All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1) FABRICATE PER IPC-6012A CLASS 2.

2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

   DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

   SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

4) SURFACE FINISH: ENIG

5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.

6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.

7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.

8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING

9) PCB MATERIAL REQUIREMENTS:

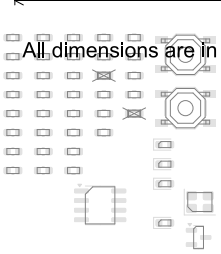
   A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
   B. Tg 170 C OR EQUIVALENT.
   C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY TRENDBIT.

10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE	90.000 × 100.000 mm
BOARD THICKNESS	1.160 mm
TRACE WIDTH	N/A mm
TRACE TO TRACE	0.100 mm
MIN. HOLE (PTH)	0.350 mm
MIN. HOLE (NPTH)	0.650 mm
ANNULAR RING	0.140 mm
COPPER TO HOLE	0.150 mm
COPPER TO EDGE	0.300 mm
HOLE TO HOLE	0.250 mm

11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.

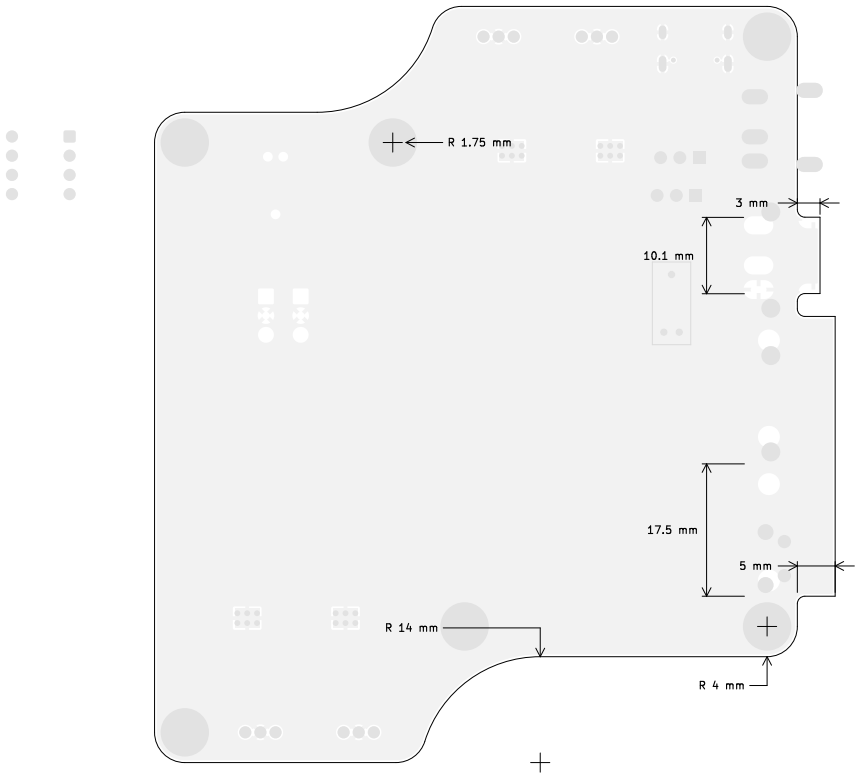
12) CONFIRM SPACE WIDTHS AND SPACINGS.



Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**
Size: A4 / Date: 2024-12-04 / GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5	Id: 1/10

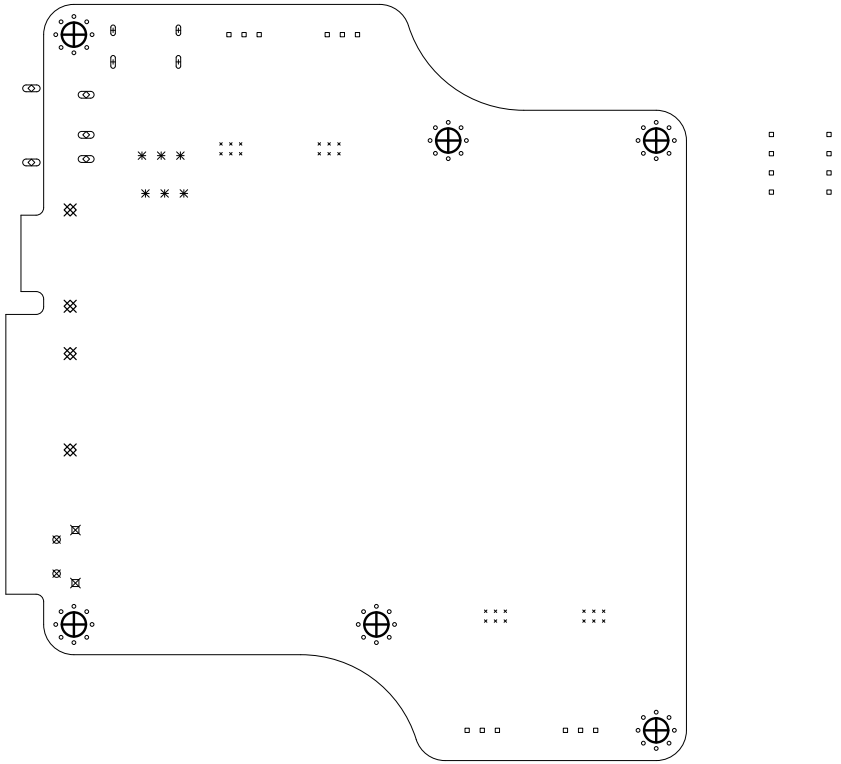
Bottom Fabrication (Scale 1:1)



All dimensions are in millimeters unless otherwise specified.

Designed for: TrendBit Designed by: Petr_Malaník			
Sheet: File: pump_board.kicad_pcb			***Project: SMPBR***
Title:			***Board: Pump_board***
Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 2/10

Drill Drawing L1 - L4 (Scale 1:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	24	0.33mm (12.99mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
○	48	0.50mm (19.69mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
+	4	0.60mm (23.62mils)	PTH	Slot	L1 (Sig) - L4 (Sig,)	Pad
□	20	0.80mm (31.50mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
◇	5	0.90mm (35.43mils)	PTH	Slot	L1 (Sig) - L4 (Sig,)	Pad
⊠	2	0.99mm (38.98mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
✳	6	1.00mm (39.37mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
⊠	2	1.30mm (51.18mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
⊠	4	1.60mm (62.99mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
⊕	6	3.20mm (125.98mils)	PTH	Round	L1 (Sig) - L4 (Sig,)	Pad
	Total 121					

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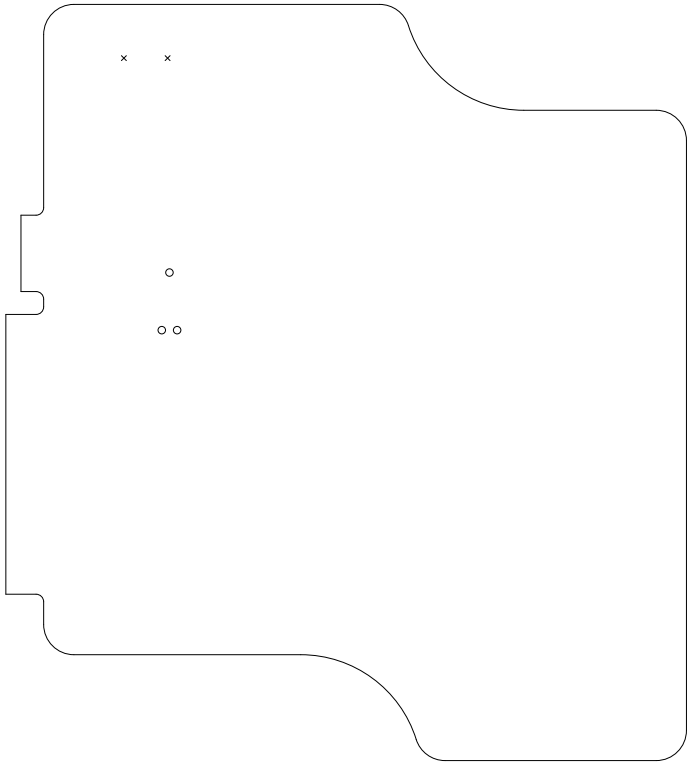
Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 3/10

Drill Drawing L1 - L4 (Scale 1:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	2	0.65mm (25.59mils)	NPTH	Round	L1 (Sig) - L4 (Sig,)	Mechanical
○	3	0.99mm (39.00mils)	NPTH	Round	L1 (Sig) - L4 (Sig,)	Mechanical
	Total 5					



Designed for: TrendBit
Designed by: Petr_Malaník

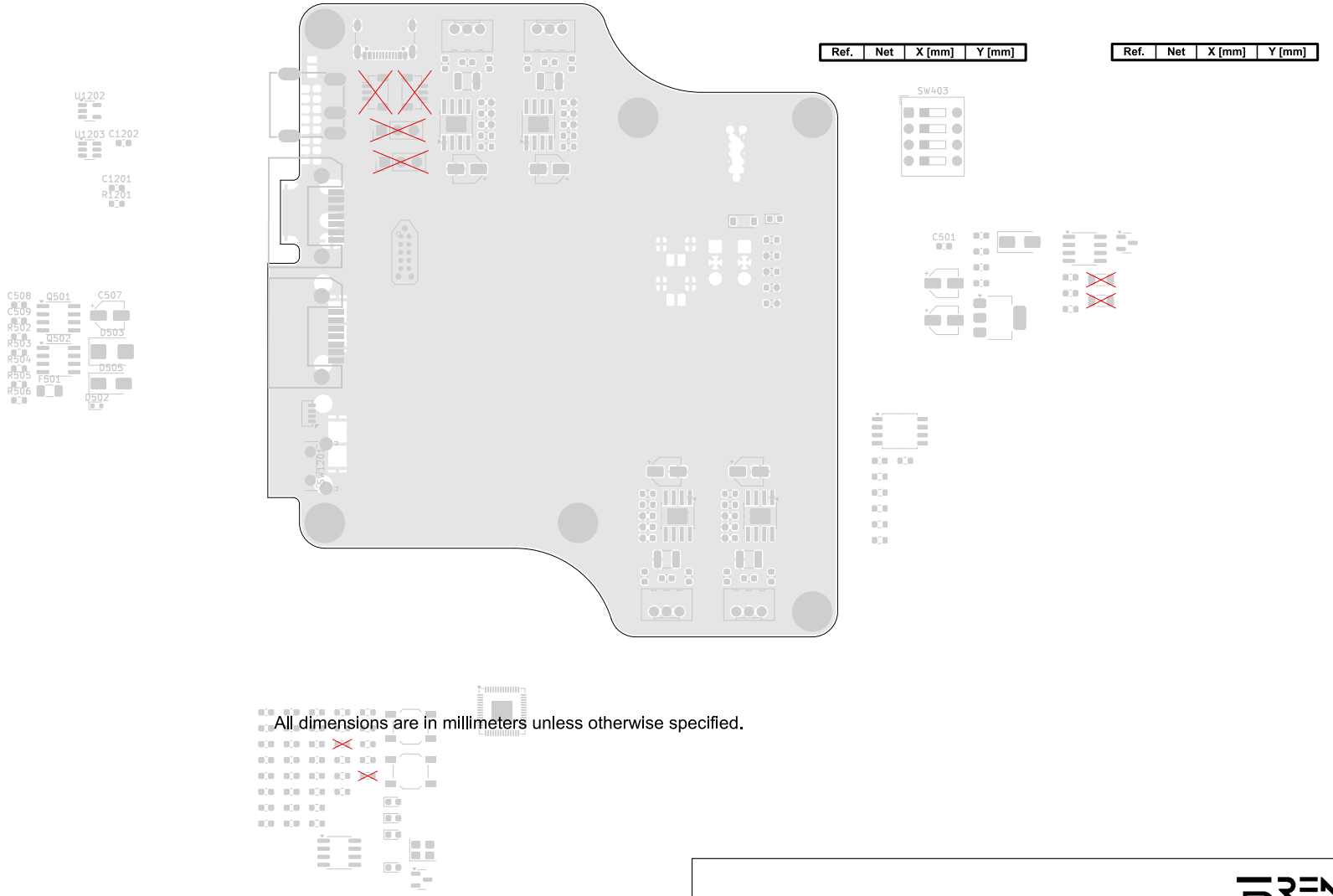
Sheet: File: pump_board.kicad_pcb	***Project: SMPBR***
Title:	***Board: Pump_board***

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 4/10

Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]

Ref.	Net	X [mm]	Y [mm]



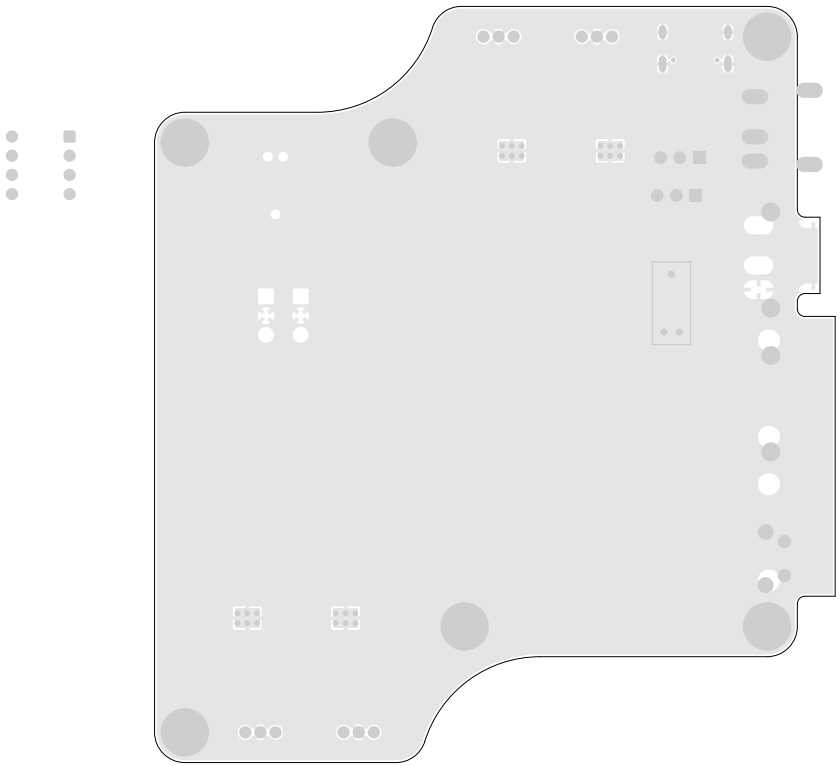
All dimensions are in millimeters unless otherwise specified.

Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 5/10

Bottom Test Points (Scale 1:1)



Ref.	Net	X [mm]	Y [mm]

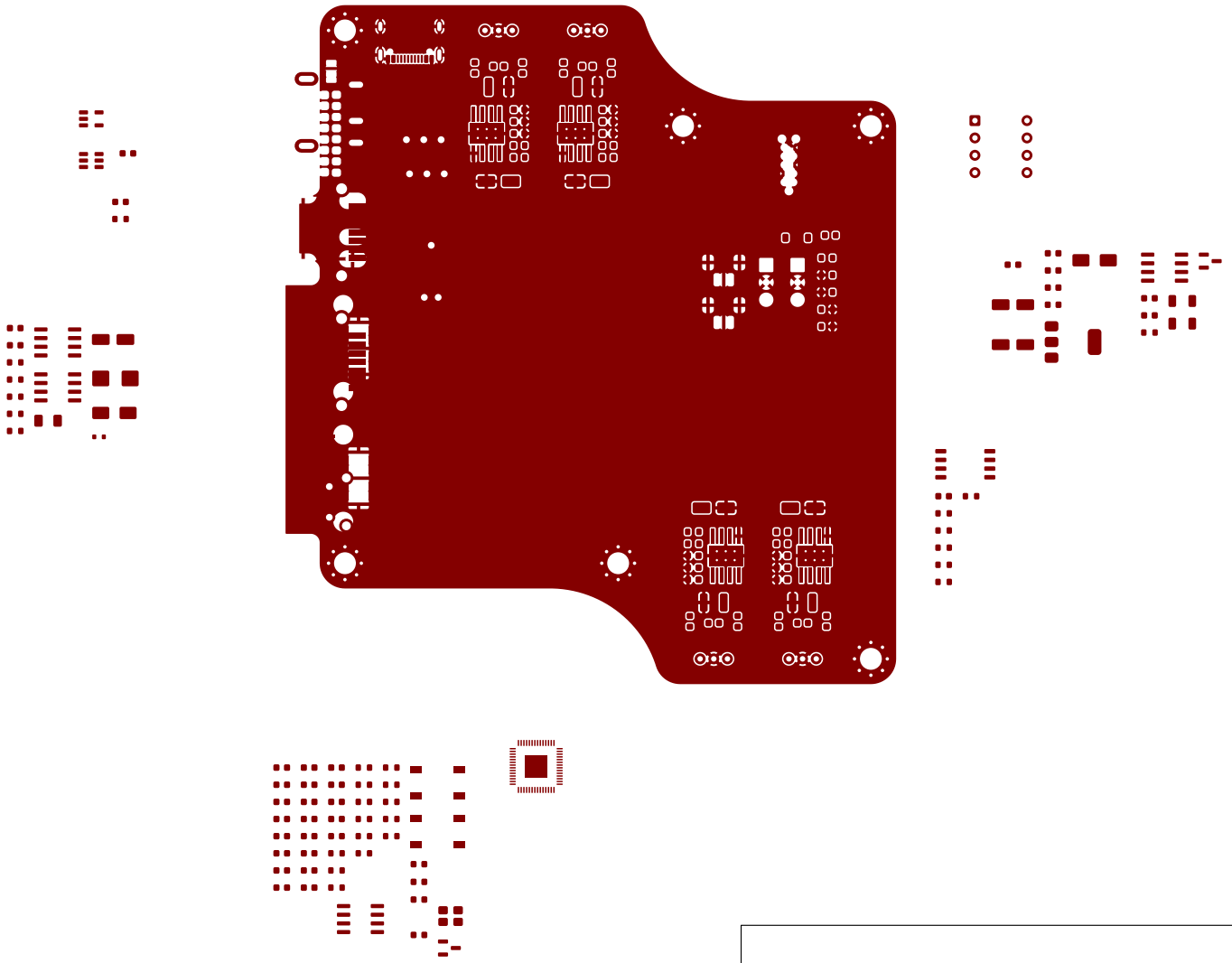
All dimensions are in millimeters unless otherwise specified.

Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 6/10

L1 (Sig) (Scale 1:1)

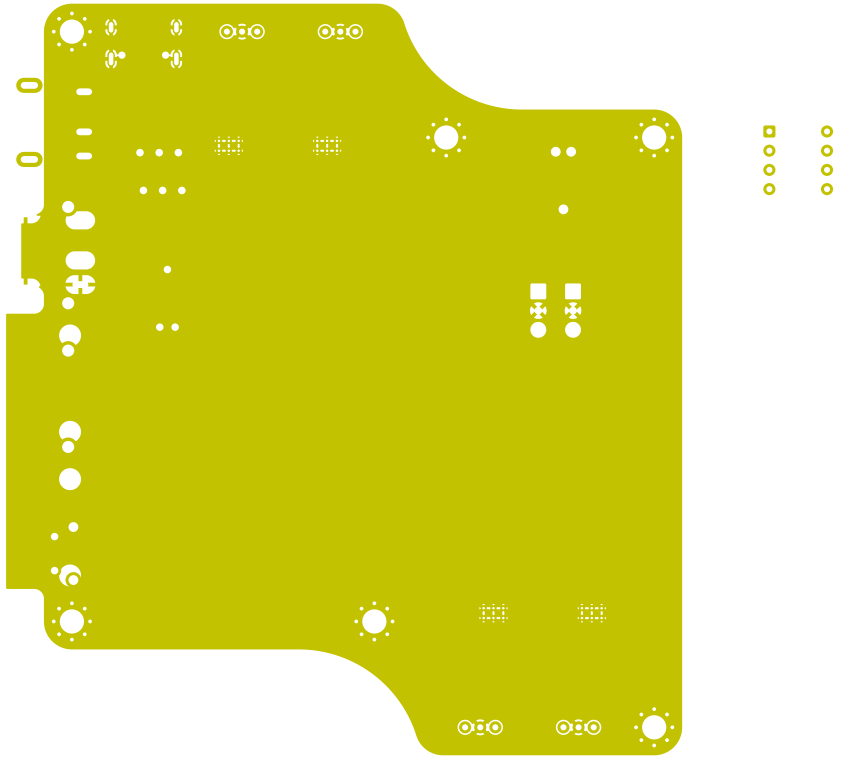


Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 7/10

L2 (GND) (Scale 1:1)

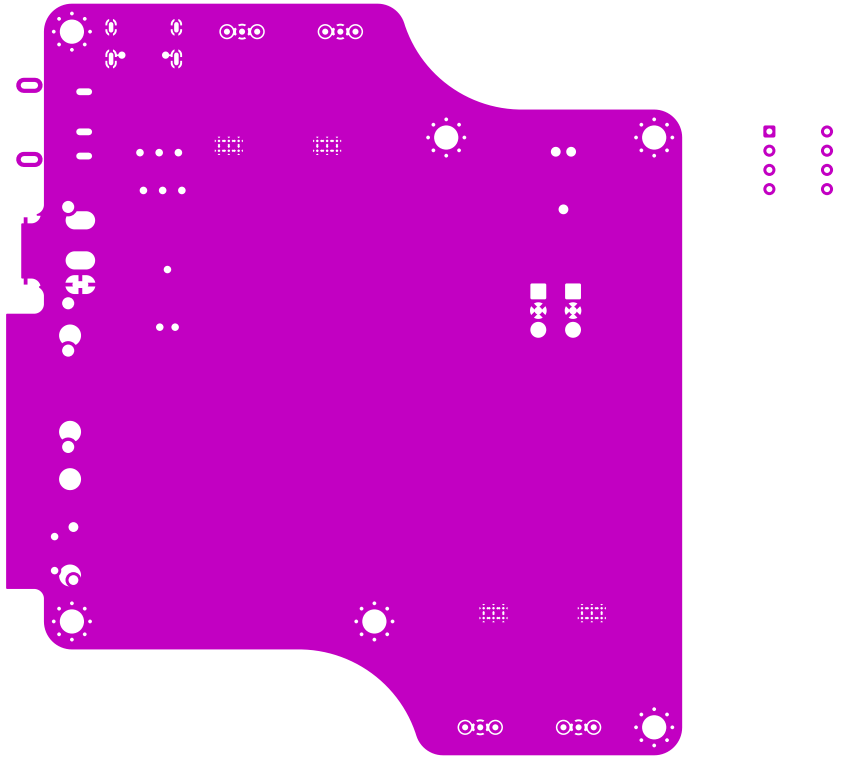


Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 8/10

L3 (PWR) (Scale 1:1)

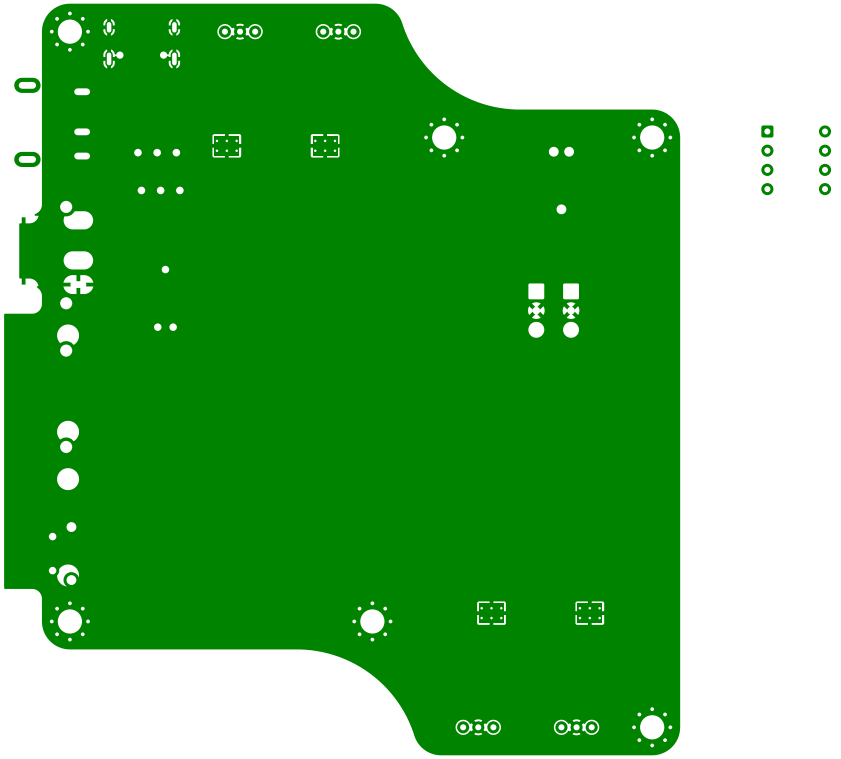


Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 9/10

L4 (Sig,) (Scale 1:1)



Designed for: TrendBit
Designed by: Petr_Malaník

Sheet: File: pump_board.kicad_pcb	**Project: SMPBR**
Title:	**Board: Pump_board**

Size: A4	Date: 2024-12-04	GIT hash: a985fdb	**Rev: 1.0**
KiCad E.D.A. 9.0.1+1 + KiBot v1.8.5			Id: 10/10