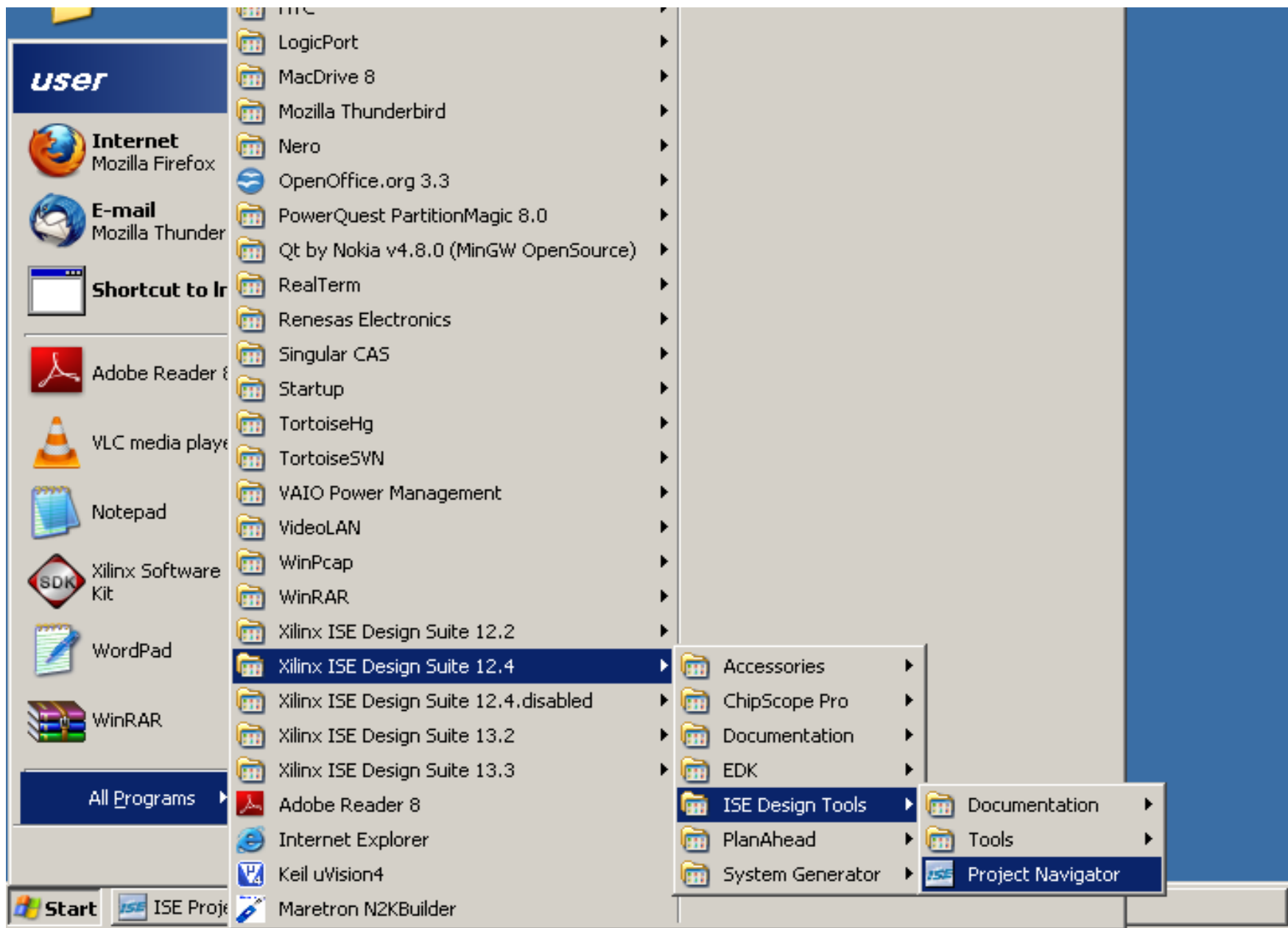
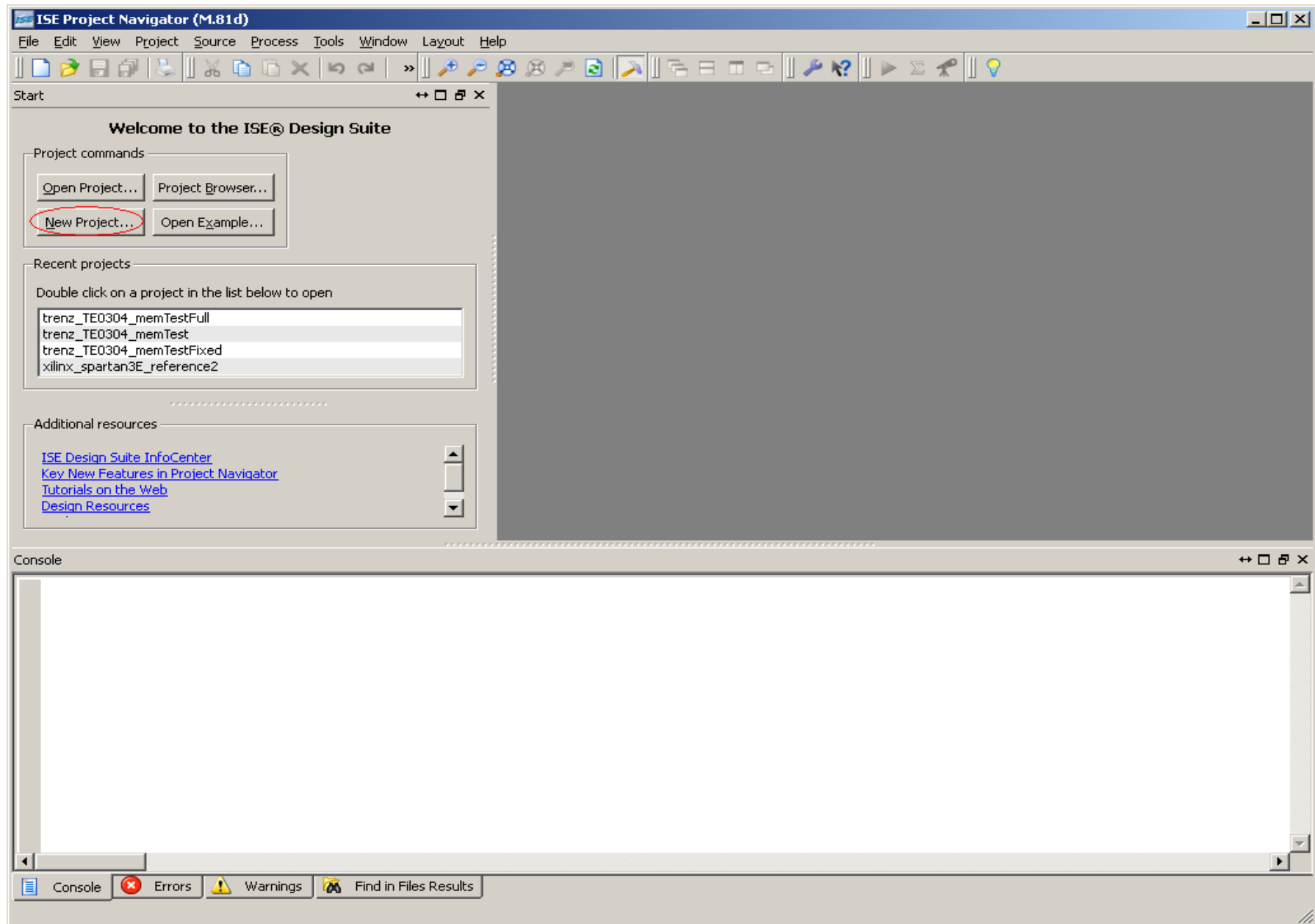


TE0300 platform

reference project creation sequence



start Xilinx ISE Project Navigator



click button to create a new project

New Project Wizard

Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name: trenz_TE0300_reference

Location: C:\m2sync\trenz_TE0300_reference ...

Working Directory: C:\m2sync\trenz_TE0300_reference ...

Description:

Select the type of top-level source for the project

Top-level source type:
HDL

More Info Next > Cancel

choose project name, then click Next

New Project Wizard

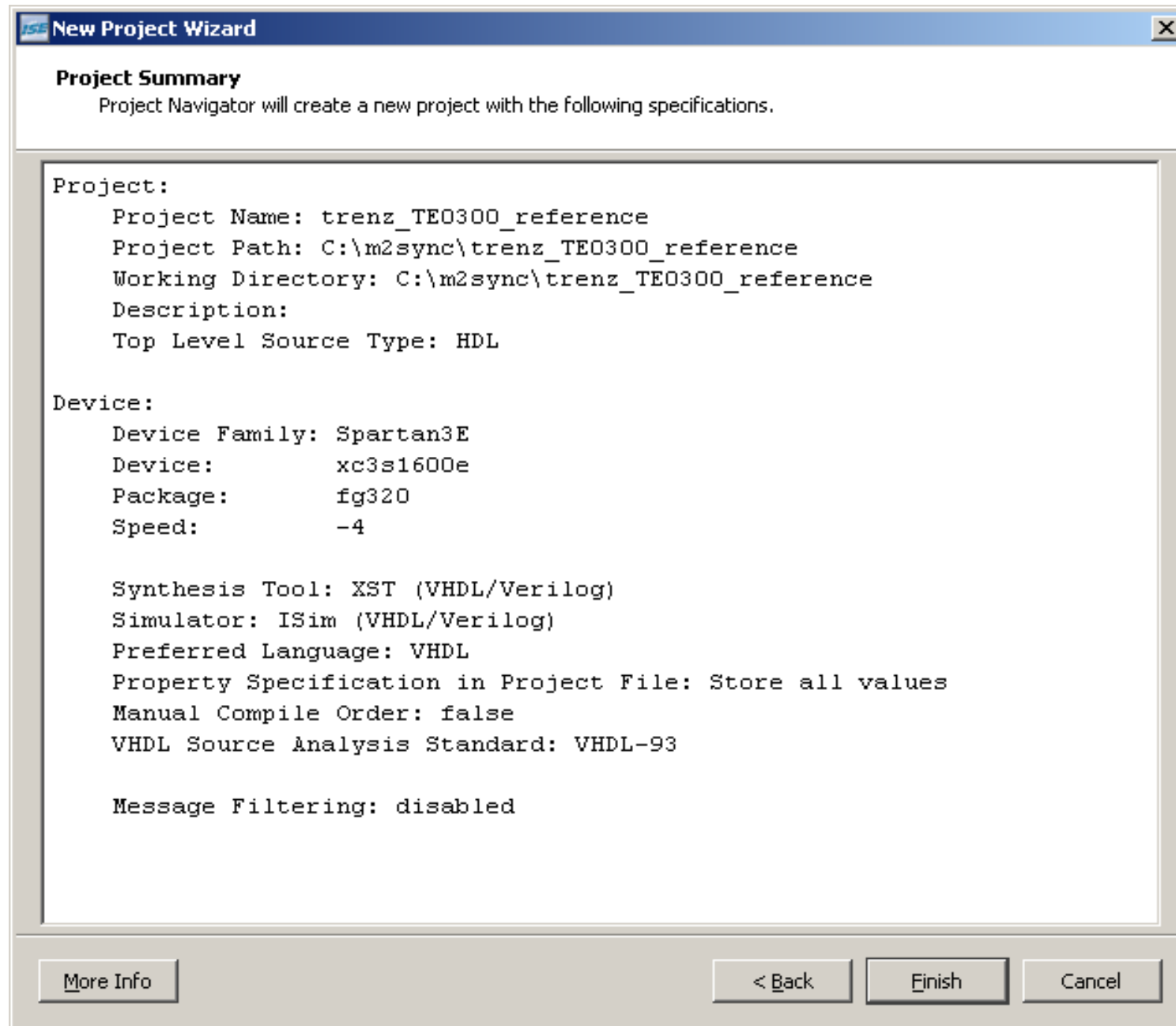
Project Settings
Specify device and project properties.

Select the device and design flow for the project

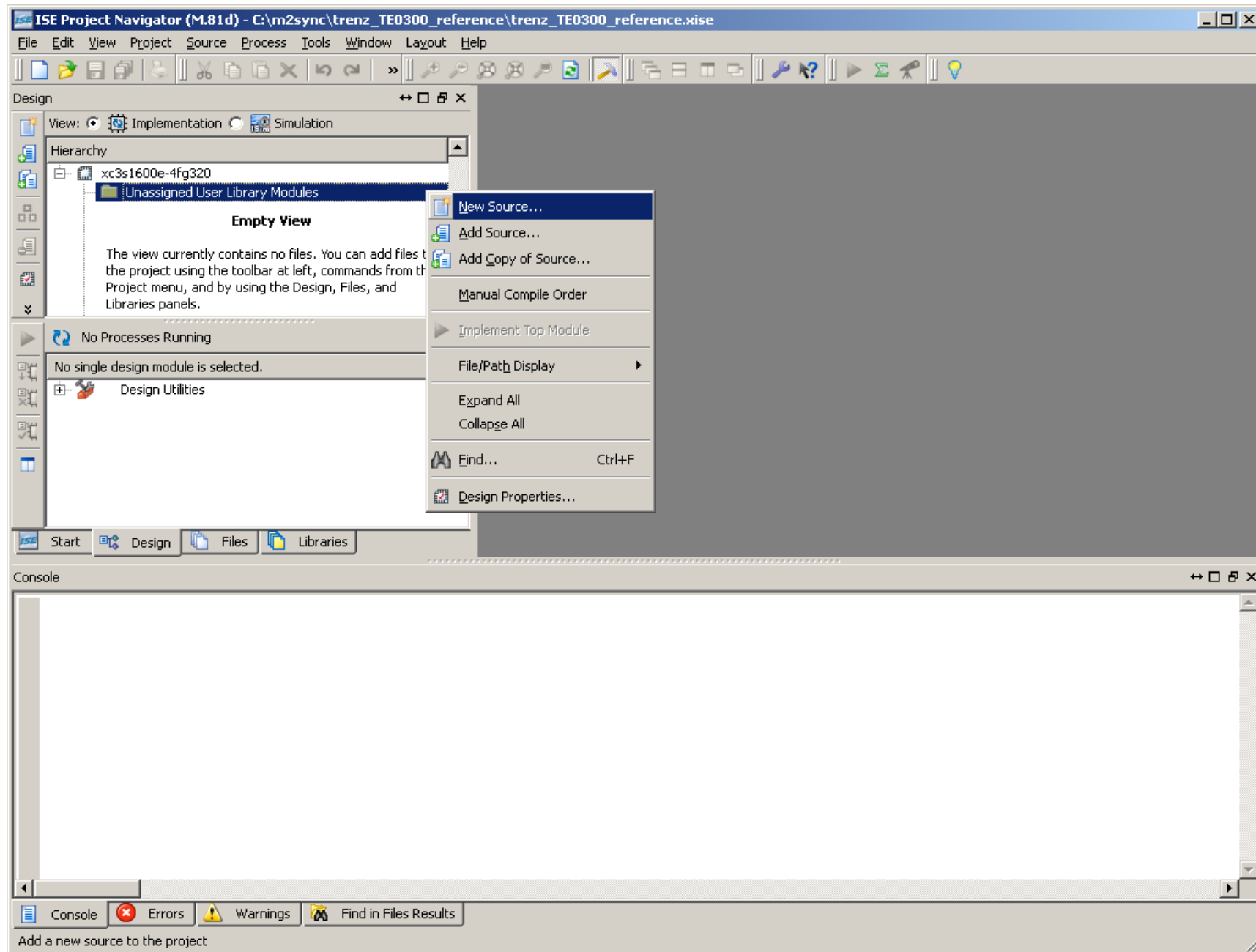
Property Name	Value
Product Category	All
Family	Spartan3E
Device	XC3S1600E
Package	FG320
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

[More Info](#) [< Back](#) [Next >](#) [Cancel](#)

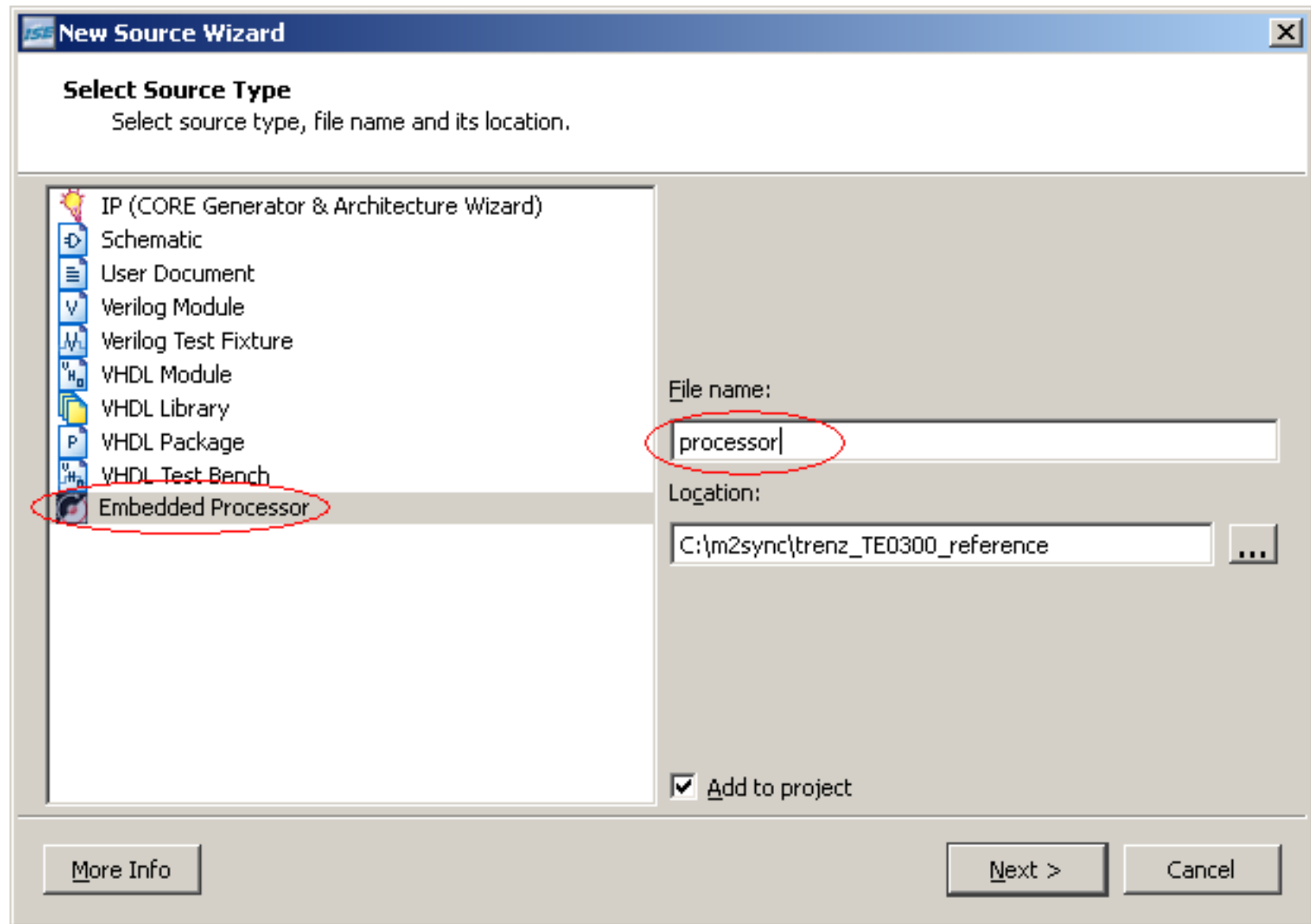
provide correct Family, Device, Package and Speed,
then click Next



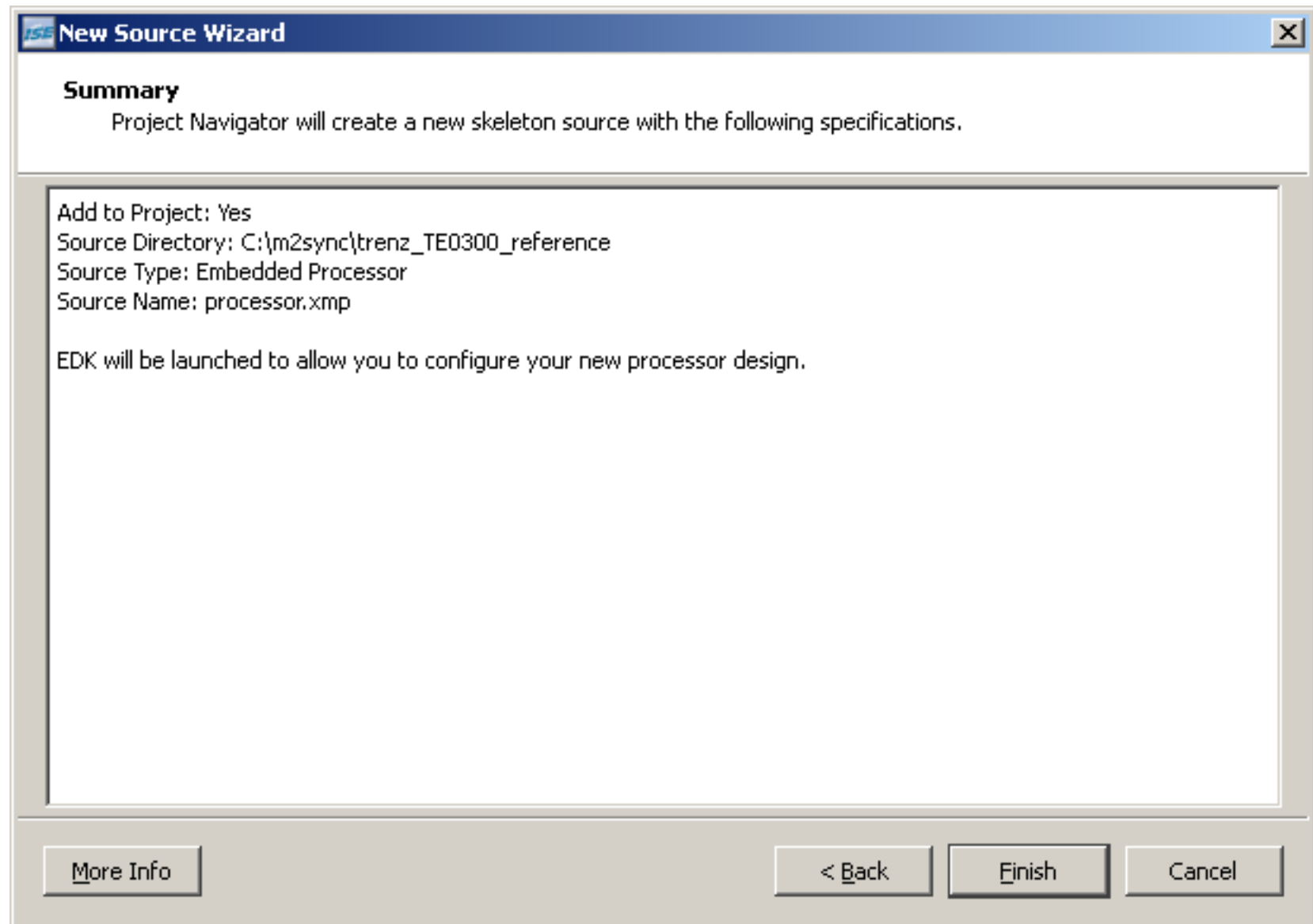
verify configuration and click Finish



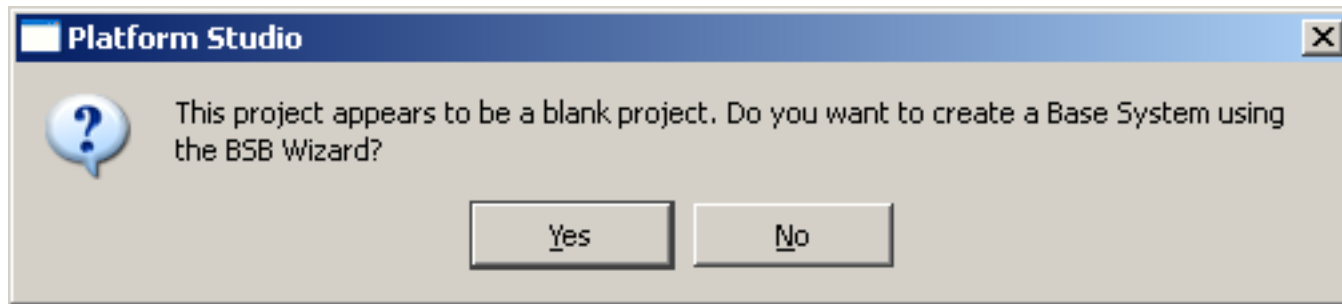
right button menu to add New Source



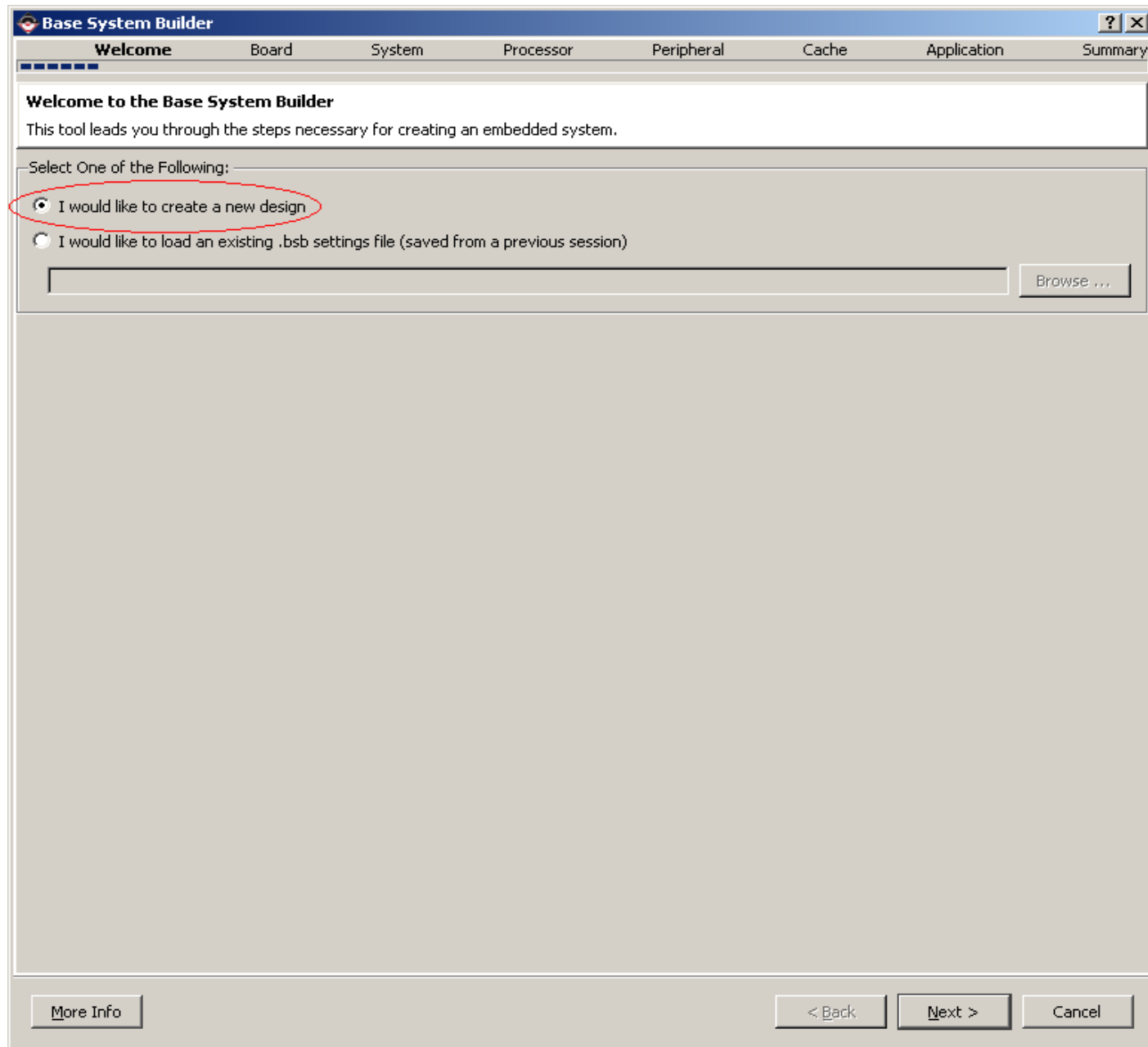
choose Embedded Processor, provide File name
then click Next



verify configuration then click Finish



confirm Yes to launch BSB Wizard



choose create new design then click Next

Base System Builder

Welcome **Board** System Processor Peripheral Cache Application Summary

Board Selection

Select a target development board.

Board

☒ I would like to create a system for the following development board

Board Vendor:

Board Name:

Board Revision:

☐ I would like to create a system for a custom board

Board Information

Architecture: Device: Package: Speed Grade:

☐ Use Stepping

Reset Polarity:

Related Information

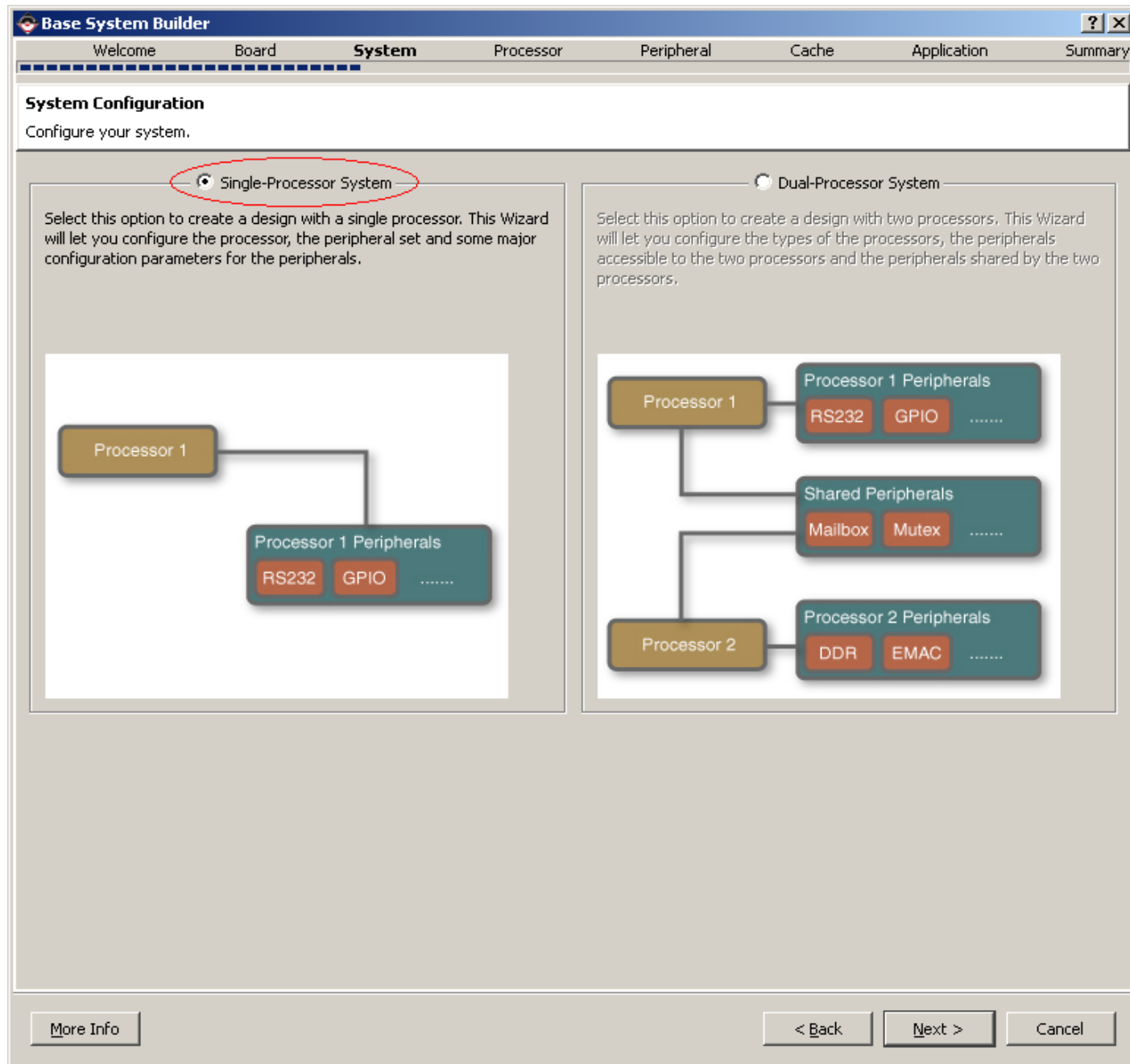
[Vendor's Website](#)

[Vendor's Contact Information](#)

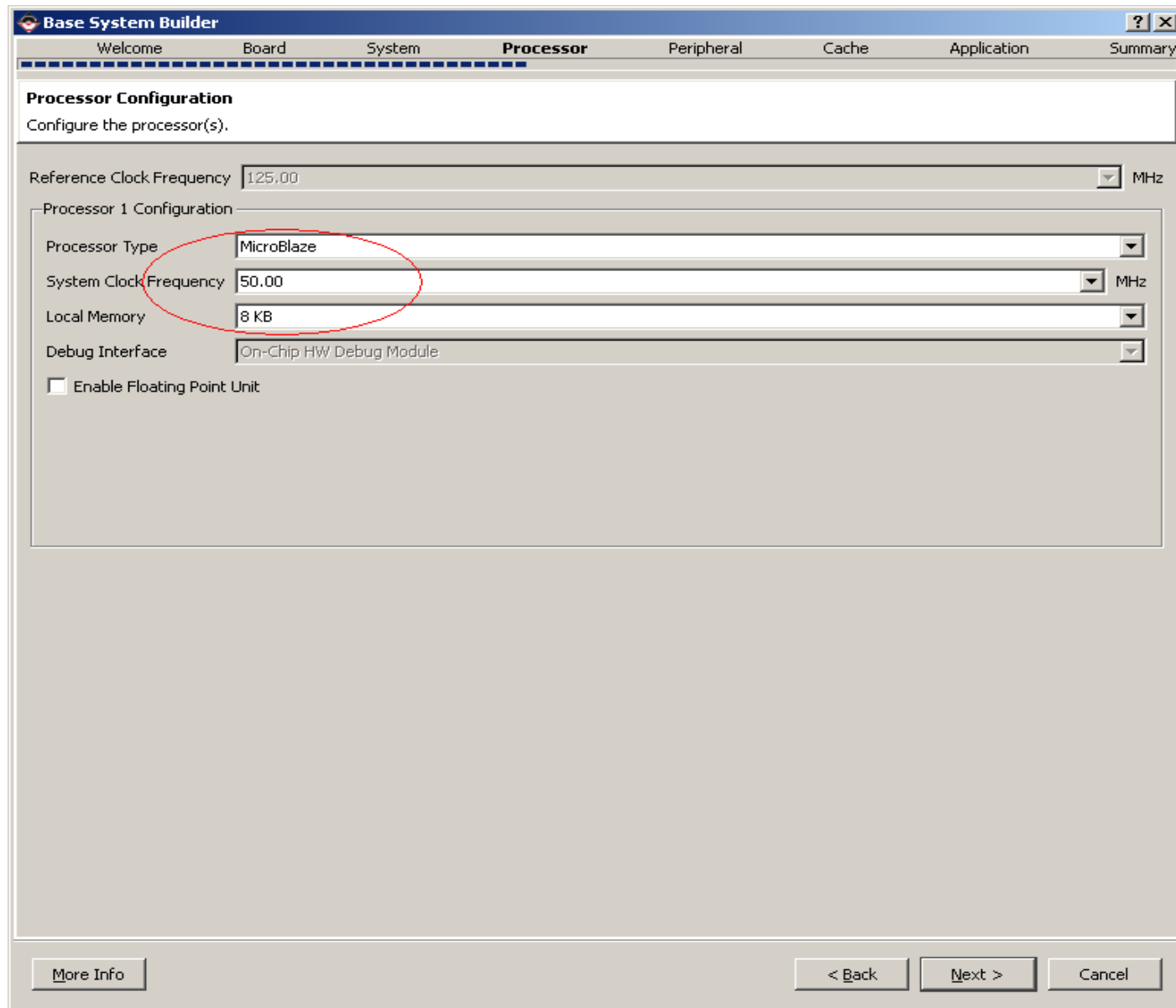
[Third Party Board Definition Files Download Website](#)

The FPGA Micromodule integrates a leading-edge Spartan-3E 1600K gates FPGA, an USB2.0 microcontroller, DDR Ram, configuration Flash and power supply on a tiny footprint. A large number of configurable I/Os are provided via shock proof B2B mini-connectors.

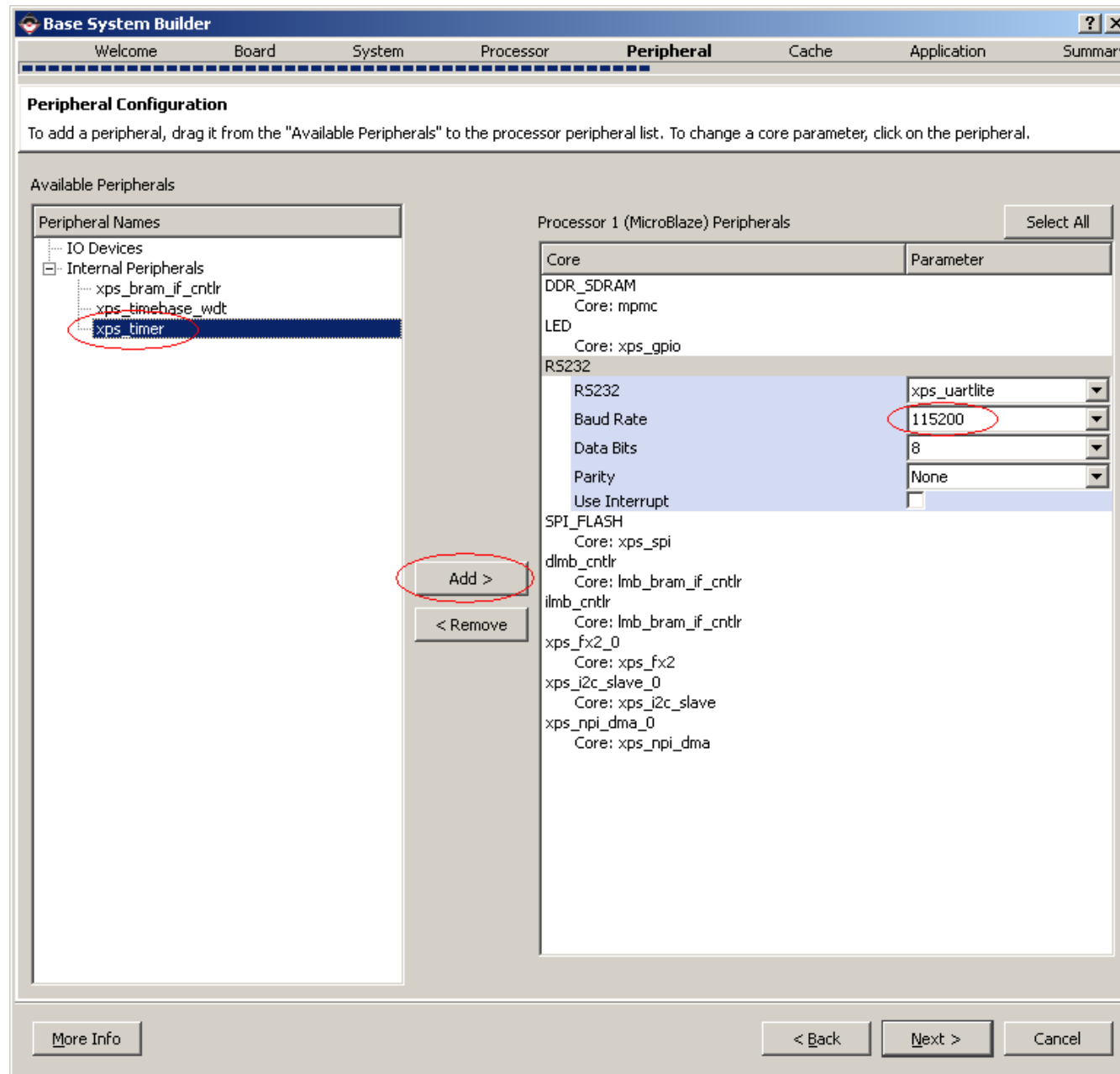
choose correct Vendor, Name and Revision then
click Next



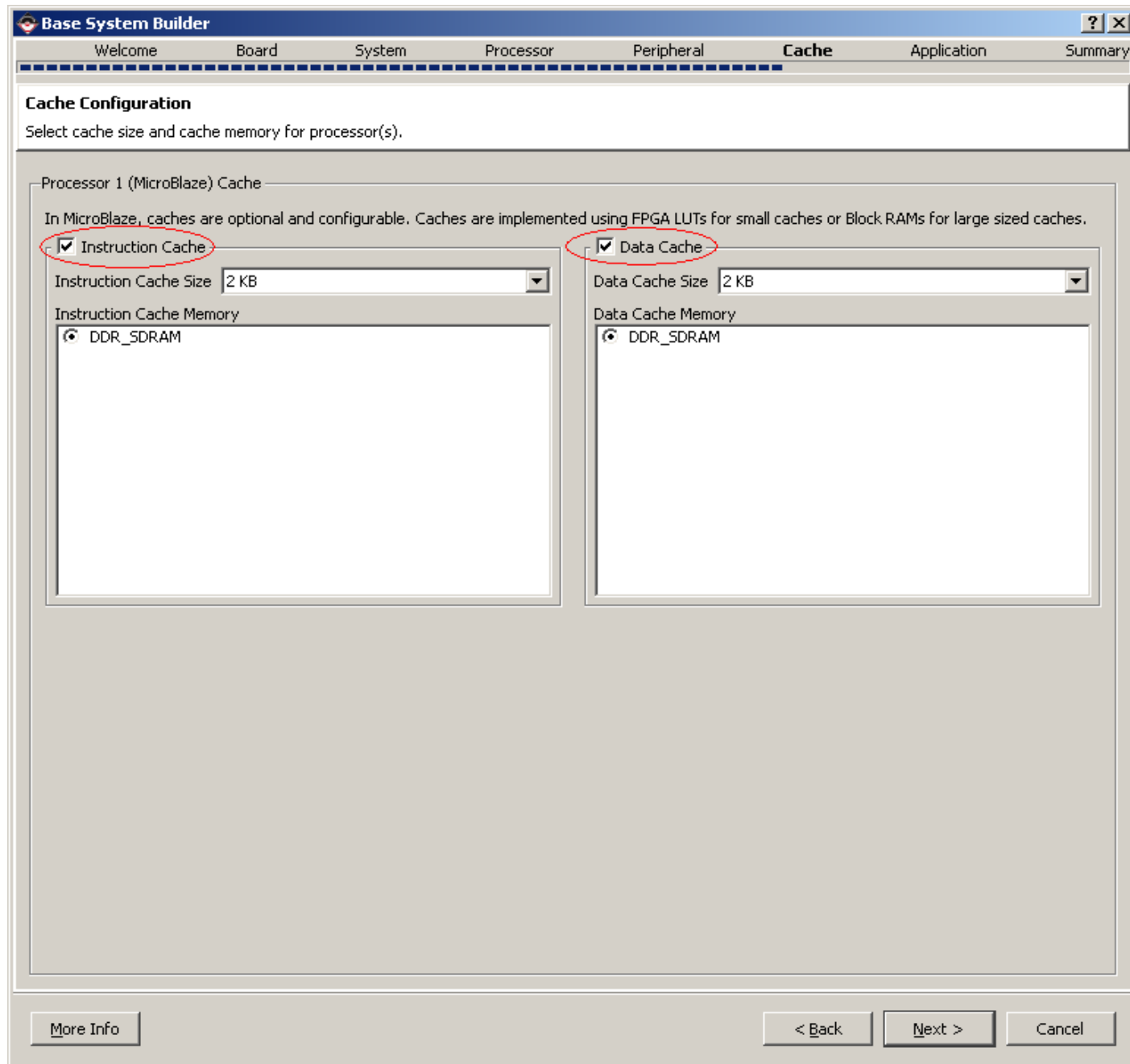
choose Single-Processor System then click Next



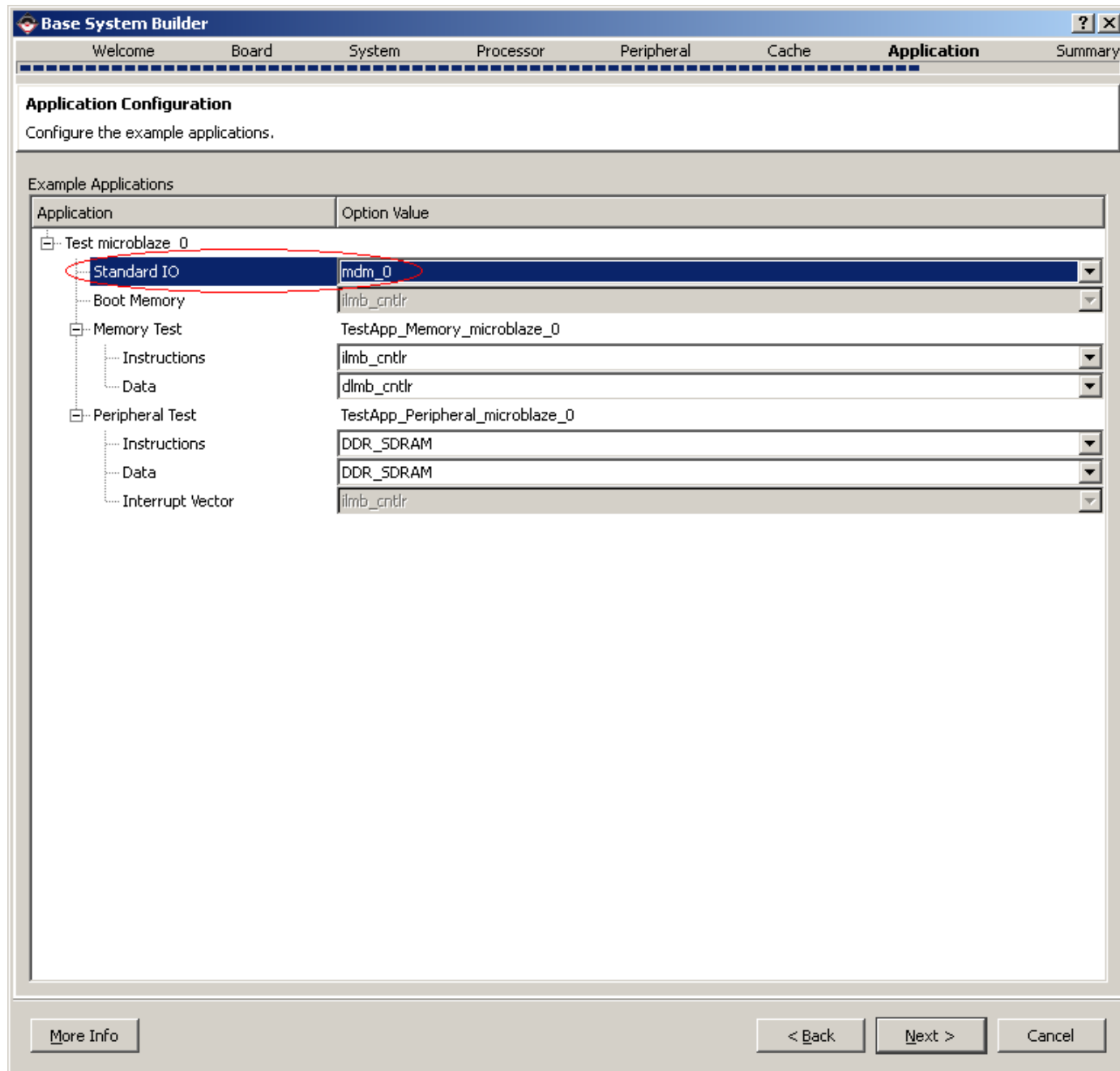
choose default Processor Type, System Clock Frequency (it will be fixed later) and Local Memory size then click Next



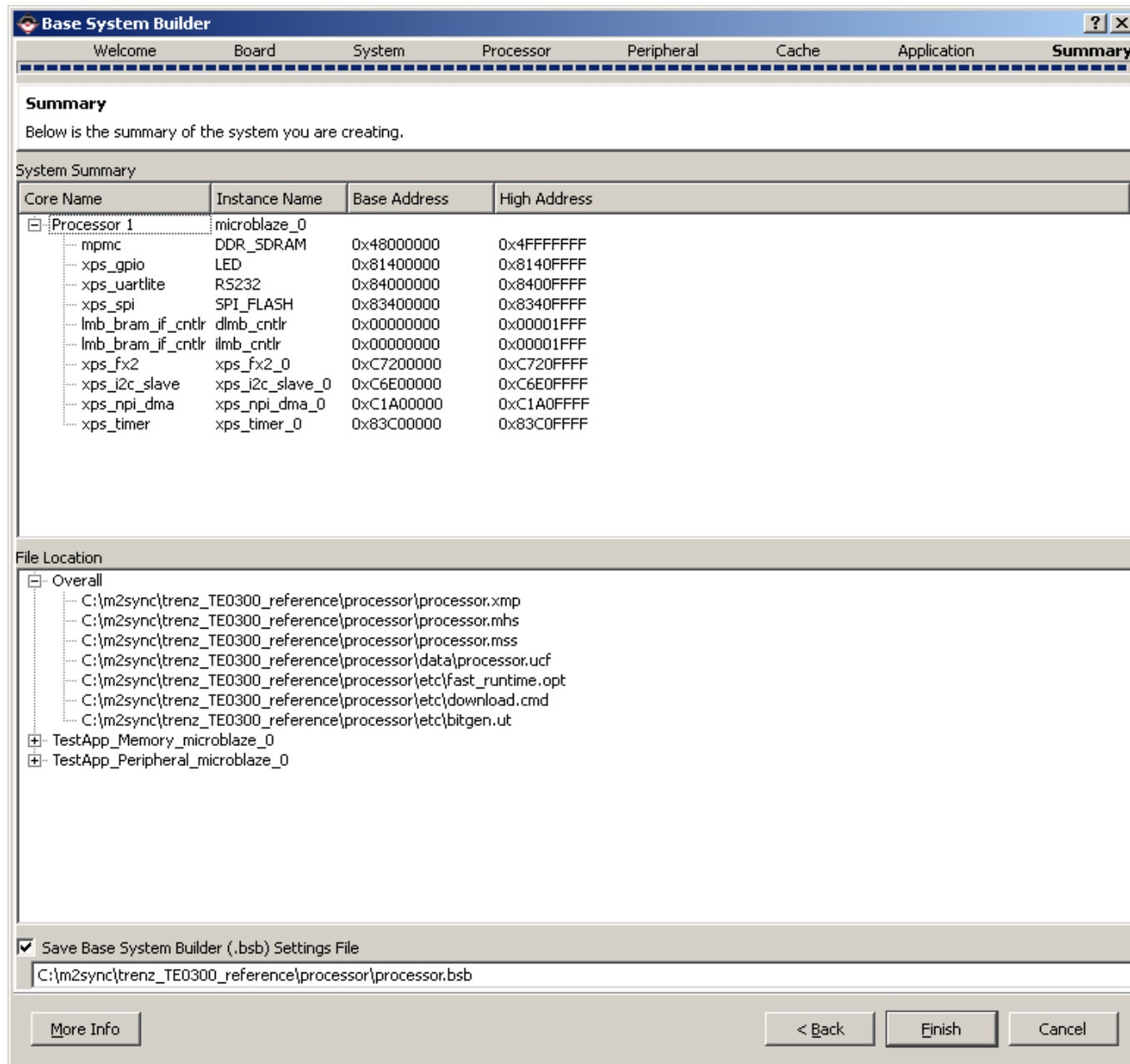
add xps_timer (XilKernel required), correct default
UART speed then click Next



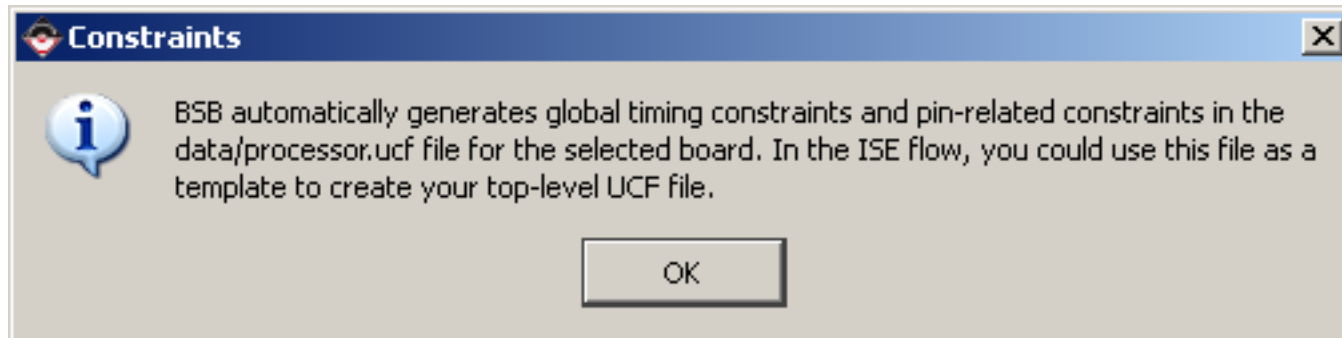
enable Instruction and Data Caches then click Next



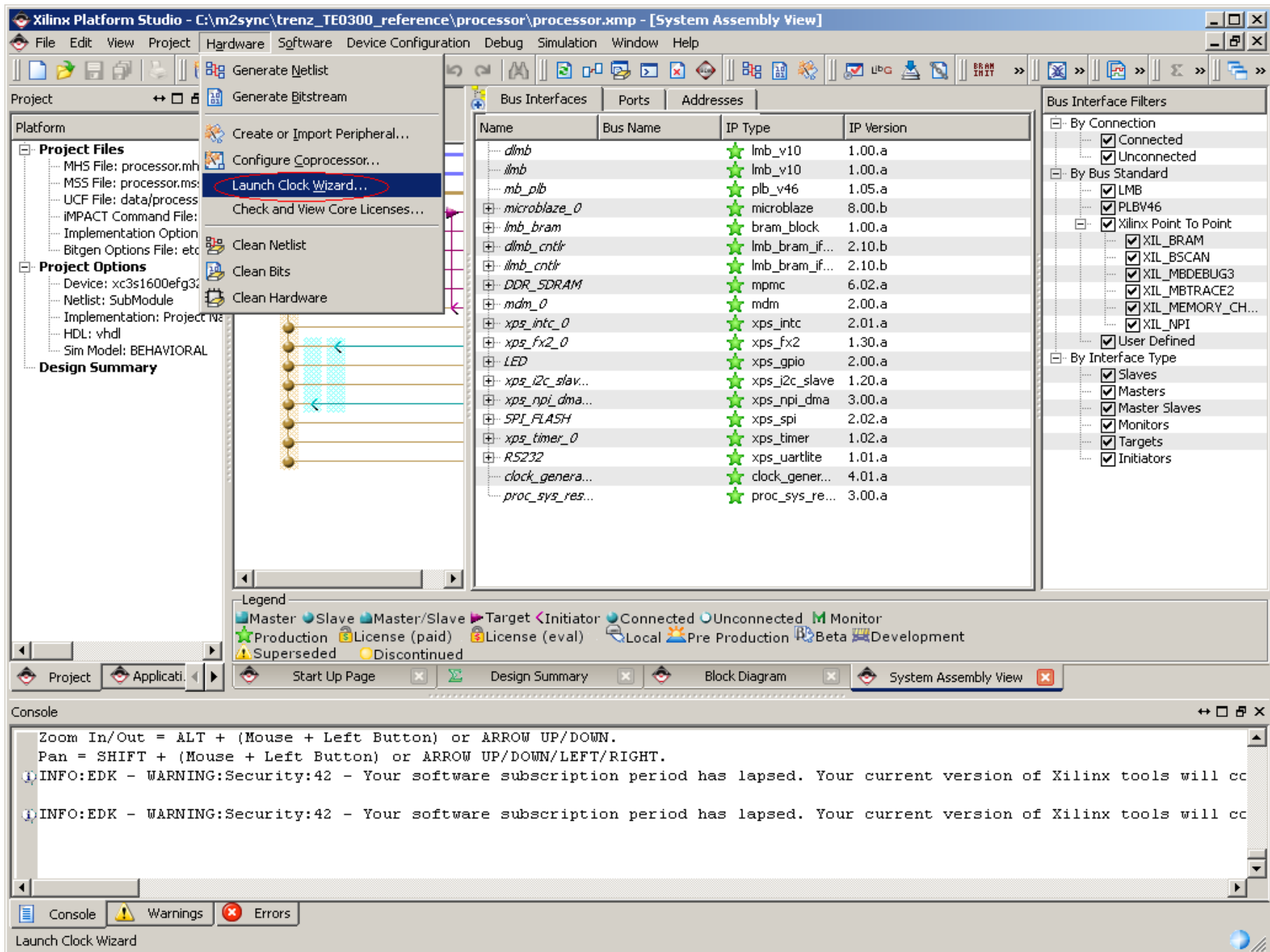
choose mdm_0 as Standard IO then click Next



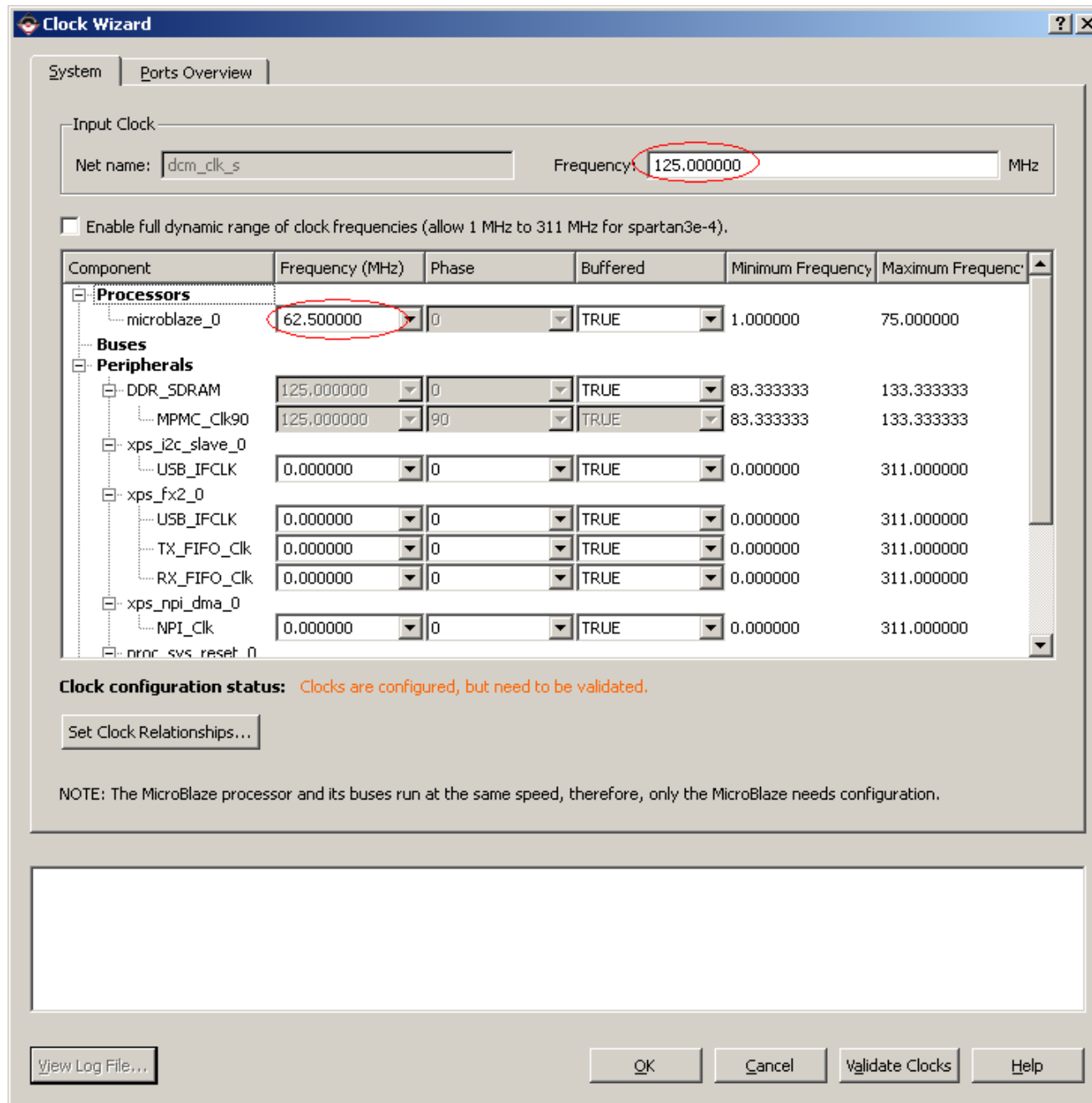
verify created configuration then click Finish



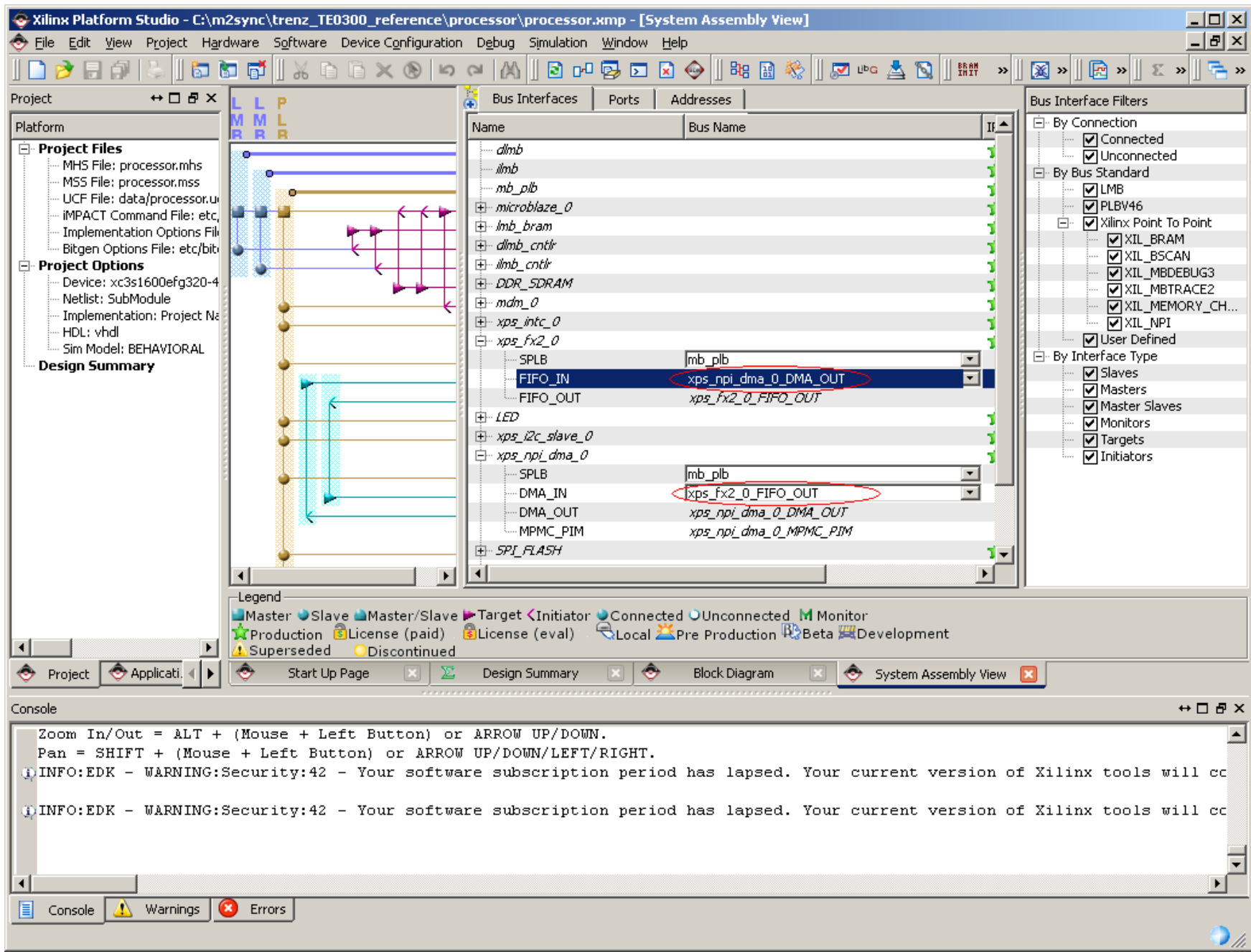
confirm UCF file creation



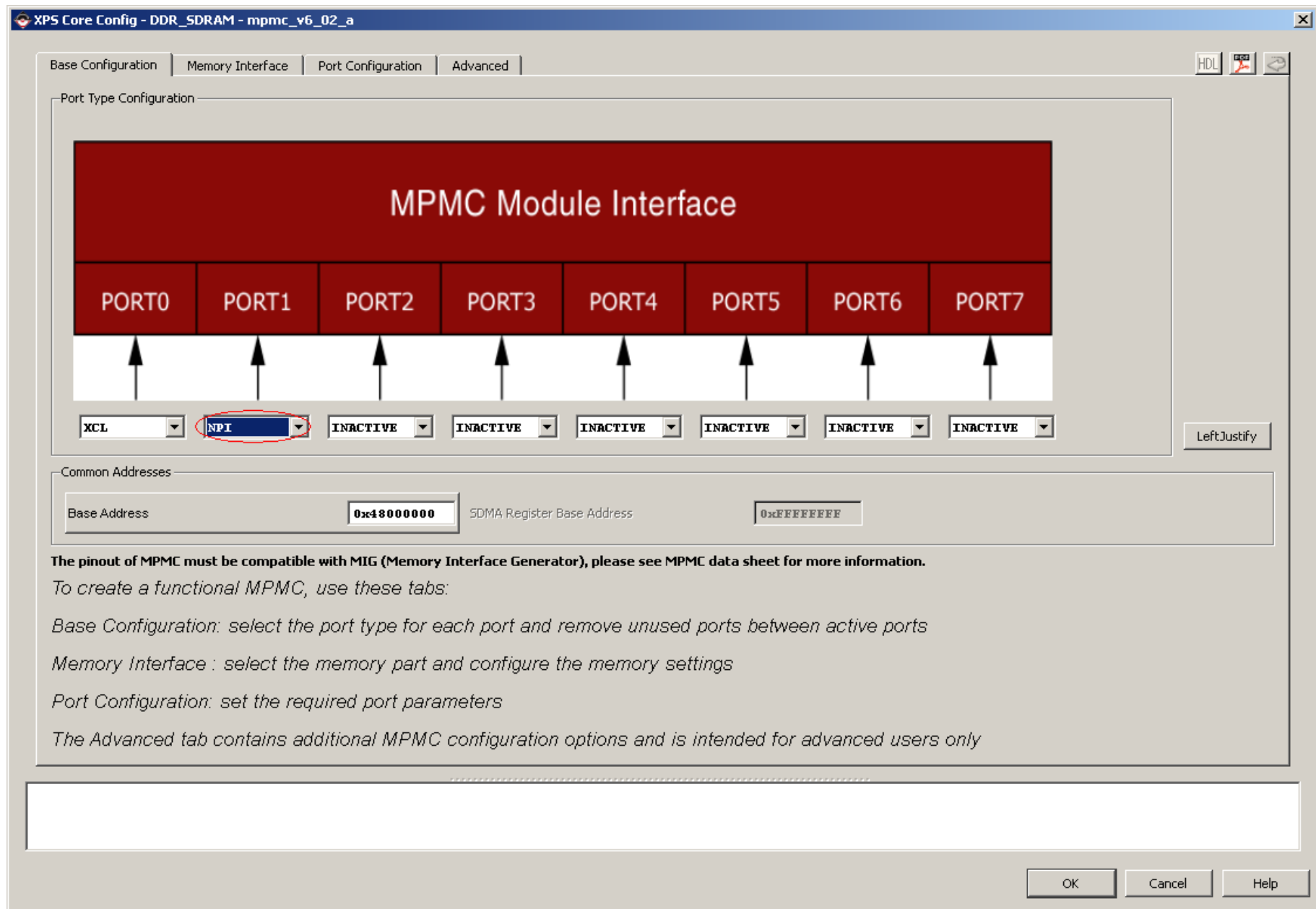
launch Clock Wizard



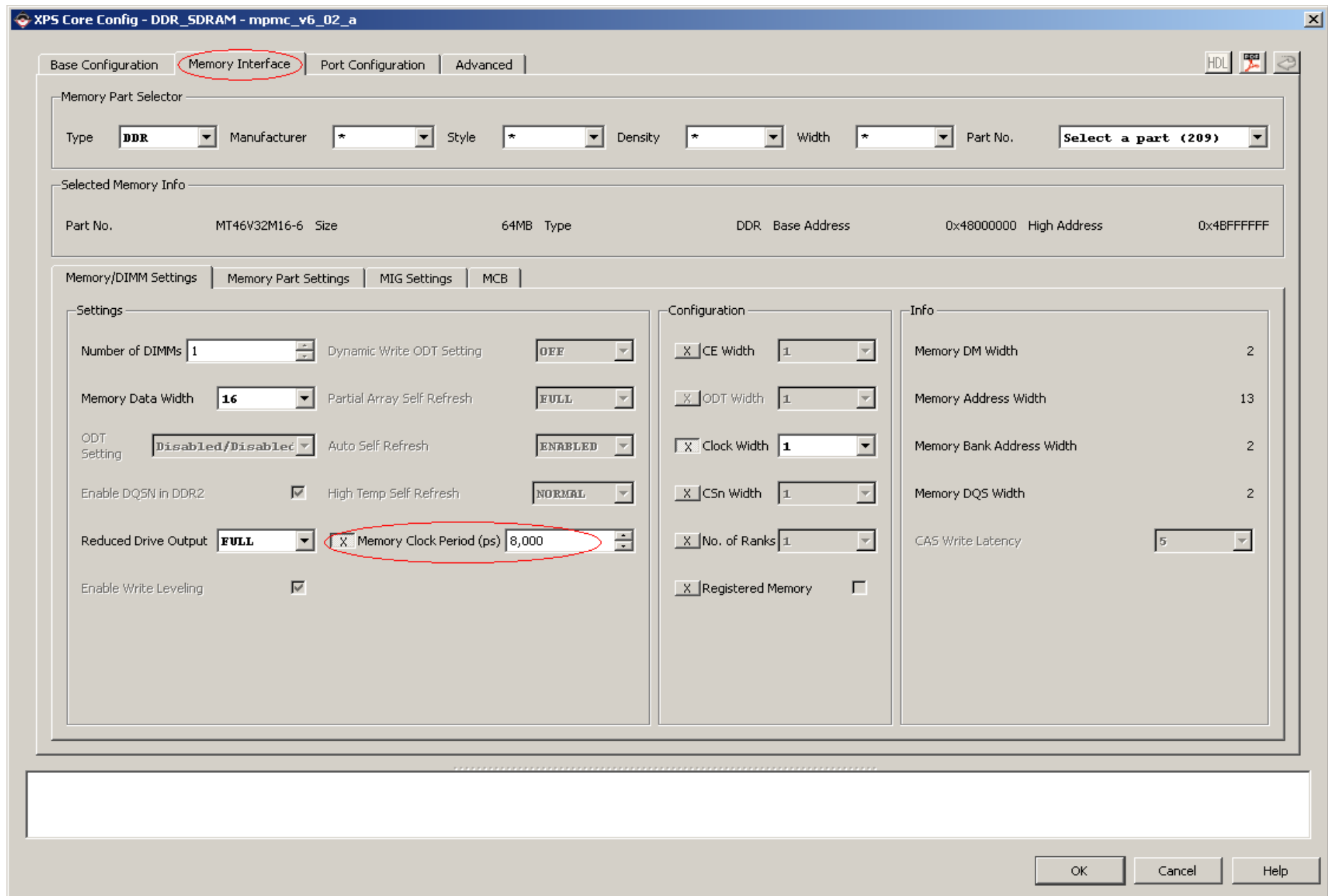
identify Input Clock frequency and choose exactly 1/2 for microblaze_0 then Validate Clocks and OK



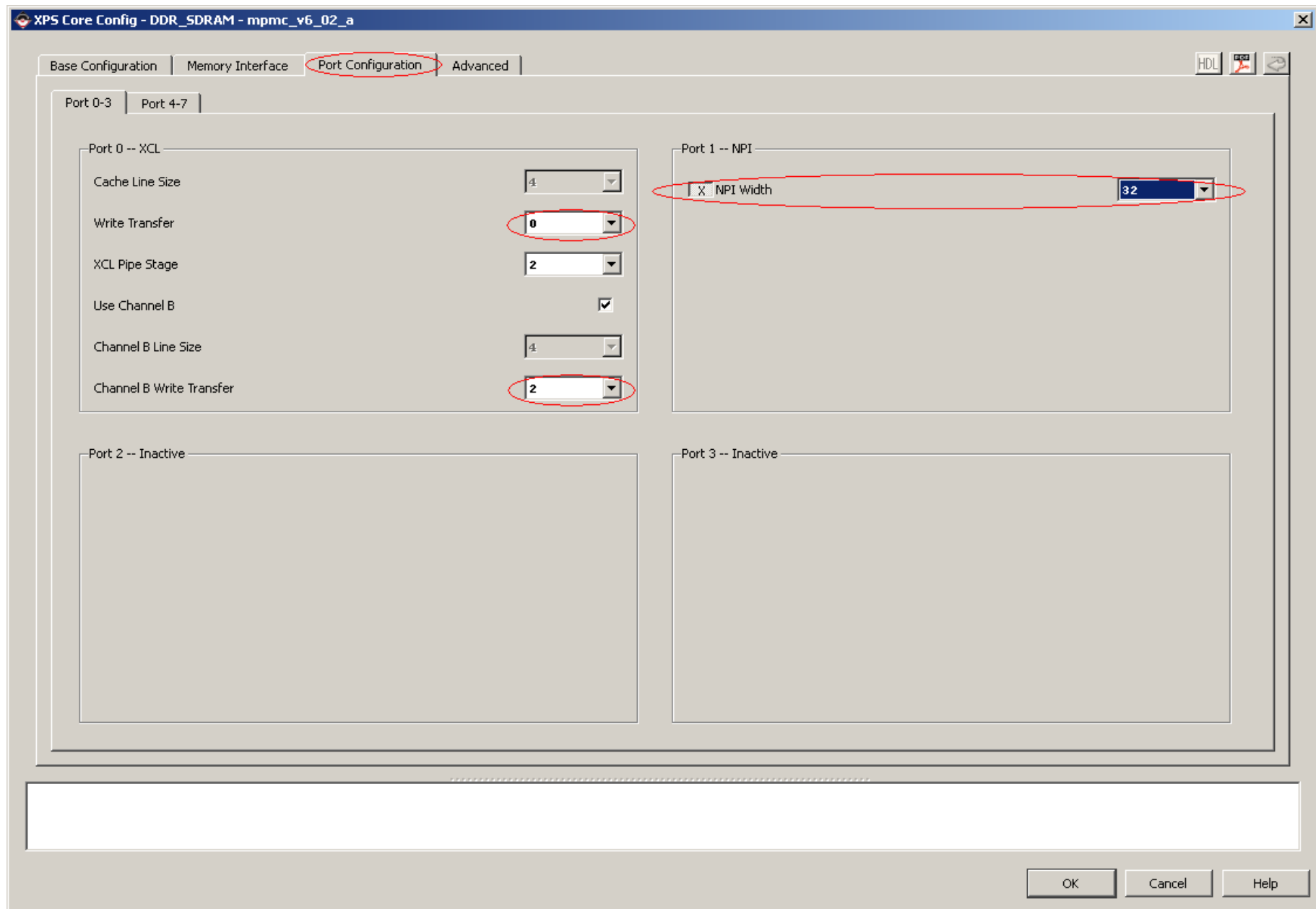
connect np_i_dma and fx2 pcores to each other



double click on DDR_SDRAM pcore and configure NPI port



switch to Memory Interface tab and activate Clock Period (8000 ps for 125Mhz, 10000 ps for 100Mhz)



switch to Port Configuration tab, correct Write Transfers and NPI Width then click OK

Xilinx Platform Studio - C:\m2sync\trenz_TE0300_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project Platform

Project Files

- MHS File: processor.mhs
- MSS File: processor.mss
- UCF File: data/processor.ucf
- IMPACT Command File: etc/
- Implementation Options File
- Bitgen Options File: etc/bit

Project Options

- Device: xc3s1600efg320-4
- Netlist: SubModule
- Implementation: Project Na
- HDL: vhdl
- Sim Model: BEHAVIORAL

Design Summary

Bus Interfaces Ports Addresses

Name	Bus Name	IP Ty
dlmb		★
ilmb		★
mb_plb		★
microblaze_0		★
lmb_bram		★
dlmb_cntlr		★
ilmb_cntlr		★
DDR_SDRAM		★
XCL0	microblaze_0_IXCL	★
XCL0_B	microblaze_0_DXCL	★
MPMC_PIM1	xps_npi_dma_0_MPMC_PIM	★
mdm_0		★
xps_intc_0		★
xps_fx2_0		★
LED		★
xps_i2c_slave_0		★
xps_npi_dma_0		★
SPI_FLASH		★
xps_timer_0		★
RS232		★
clock_generator_0		★
proc_sys_reset_0		★

Bus Interface Filters

- By Connection
 - ☒ Connected
 - ☒ Unconnected
- By Bus Standard
 - ☒ LMB
 - ☒ PLBV46
 - ☒ Xilinx Point To Point
 - ☒ XIL_BRAM
 - ☒ XIL_BSCAN
 - ☒ XIL_MBDEBUG3
 - ☒ XIL_MBTRACE2
 - ☒ XIL_MEMORY_CH...
 - ☒ XIL_NPI
- By Interface Type
 - ☒ Slaves
 - ☒ Masters
 - ☒ Master Slaves
 - ☒ Monitors
 - ☒ Targets
 - ☒ Initiators

Legend

- Master (blue circle)
- Slave (green circle)
- Master/Slave (blue circle with green border)
- Target (purple circle)
- Initiator (pink circle)
- Connected (blue line)
- Unconnected (orange line)
- Monitor (green star)
- Production (yellow star)
- License (paid) (blue star)
- License (eval) (orange star)
- Local (blue star)
- Pre Production (yellow star)
- Beta (blue star)
- Development (green star)
- Superseded (yellow star)
- Discontinued (orange star)

Project Application

Start Up Page Design Summary Block Diagram System Assembly View

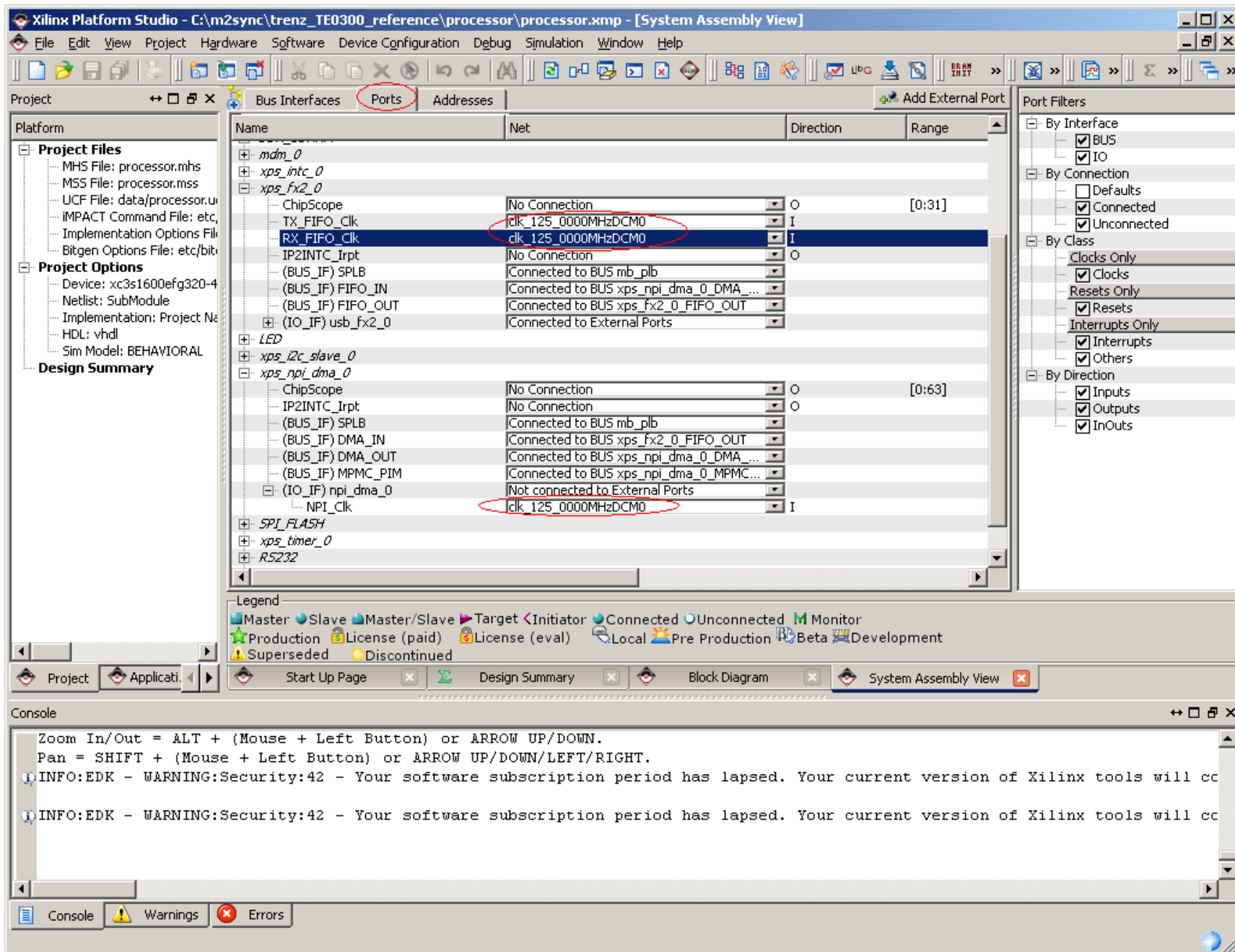
Console

```

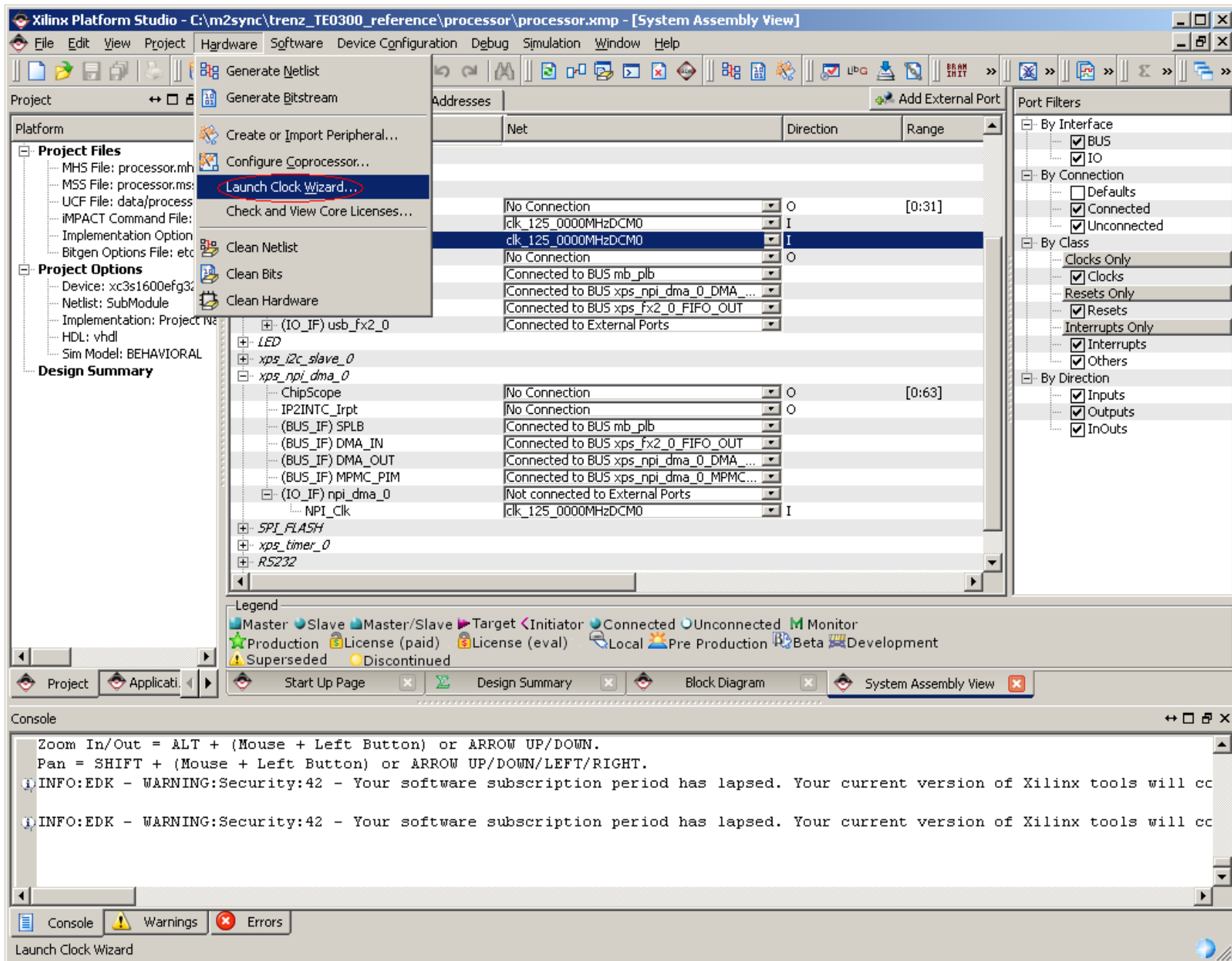
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
  
```

Console Warnings Errors

connect mpmc and npi_dma pcores



switch to Ports tab and assign npi_dma and fx2 clocks



re-launch Clock Wizard

Clock Wizard

System | Ports Overview

Input Clock

Net name: Frequency: MHz

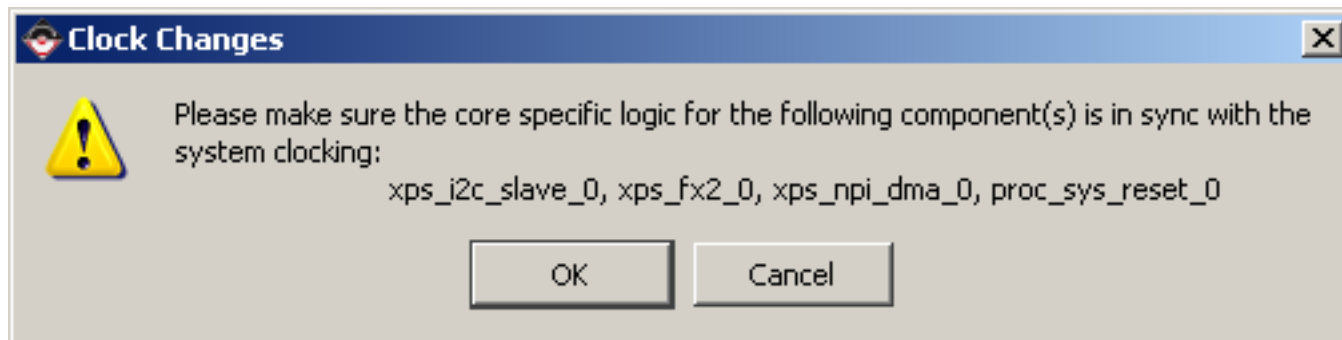
☐ Enable full dynamic range of clock frequencies (allow 1 MHz to 311 MHz for spartan3e-4).

Component	Frequency (MHz)	Phase	Buffered	Minimum Frequency	Maximum Frequency
Processors					
microblaze_0	62.500000	0	TRUE	1.000000	75.000000
Buses					
Peripherals					
DDR_SDRAM	125.000000	0	TRUE	83.333333	133.333333
MPMC_Clk90	125.000000	90	TRUE	83.333333	133.333333
xps_i2c_slave_0					
USB_IFCLK	0.000000	0	TRUE	0.000000	311.000000
xps_fx2_0					
USB_IFCLK	0.000000	0	TRUE	0.000000	311.000000
TX_FIFO_Clk	125.000000	0	TRUE	0.000000	311.000000
RX_FIFO_Clk	125.000000	0	TRUE	0.000000	311.000000
xps_npi_dma_0					
NPI_Clk	125.000000	0	TRUE	0.000000	311.000000

Clock configuration status: Clocks are configured, but need to be validated.

NOTE: The MicroBlaze processor and its buses run at the same speed, therefore, only the MicroBlaze needs configuration.

re-validate clocks then click OK



confirm Clock Changes

Xilinx Platform Studio - C:\m2sync\trenz_TE0300_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project Bus Interfaces Ports **Addresses** Generate Addresses

Platform

Project Files

- MHS File: processor.mhs
- MSS File: processor.mss
- UCF File: data/processor.ucf
- IMPACT Command File: etc/processor.impact
- Implementation Options File: etc/processor.implementation_options
- Bitgen Options File: etc/processor.bitgen_options

Project Options

- Device: xc3s1600efg320-4
- Netlist: SubModule
- Implementation: Project Name
- HDL: vhdl
- Sim Model: BEHAVIORAL

Design Summary

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address Map							
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	dlmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	ilmb	<input type="checkbox"/>
DDR_SDRAM	C_MPMC_BASEA...	0x44000000	0x47FFFFFF	64M	XCL0:XCL0_B	microblaze_0_IXCL	<input type="checkbox"/>
LED	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
xps_timer_0	C_BASEADDR	0x83C00000	0x83C0FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
RS232	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
xps_npi_dma_0	C_BASEADDR	0xC1A00000	0xC1A0FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
xps_i2c_slave_0	C_BASEADDR	0xC6E00000	0xC6E0FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
xps_fx2_0	C_BASEADDR	0xC7200000	0xC720FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>

Legend

- Master Slave Master/Slave Target Initiator Connected Unconnected Monitor
- Production License (paid) License (eval) Local Pre Production Beta Development
- Superseded Discontinued

Project Appli... Start Up Page Design Summary Block Diagram System Assembly View

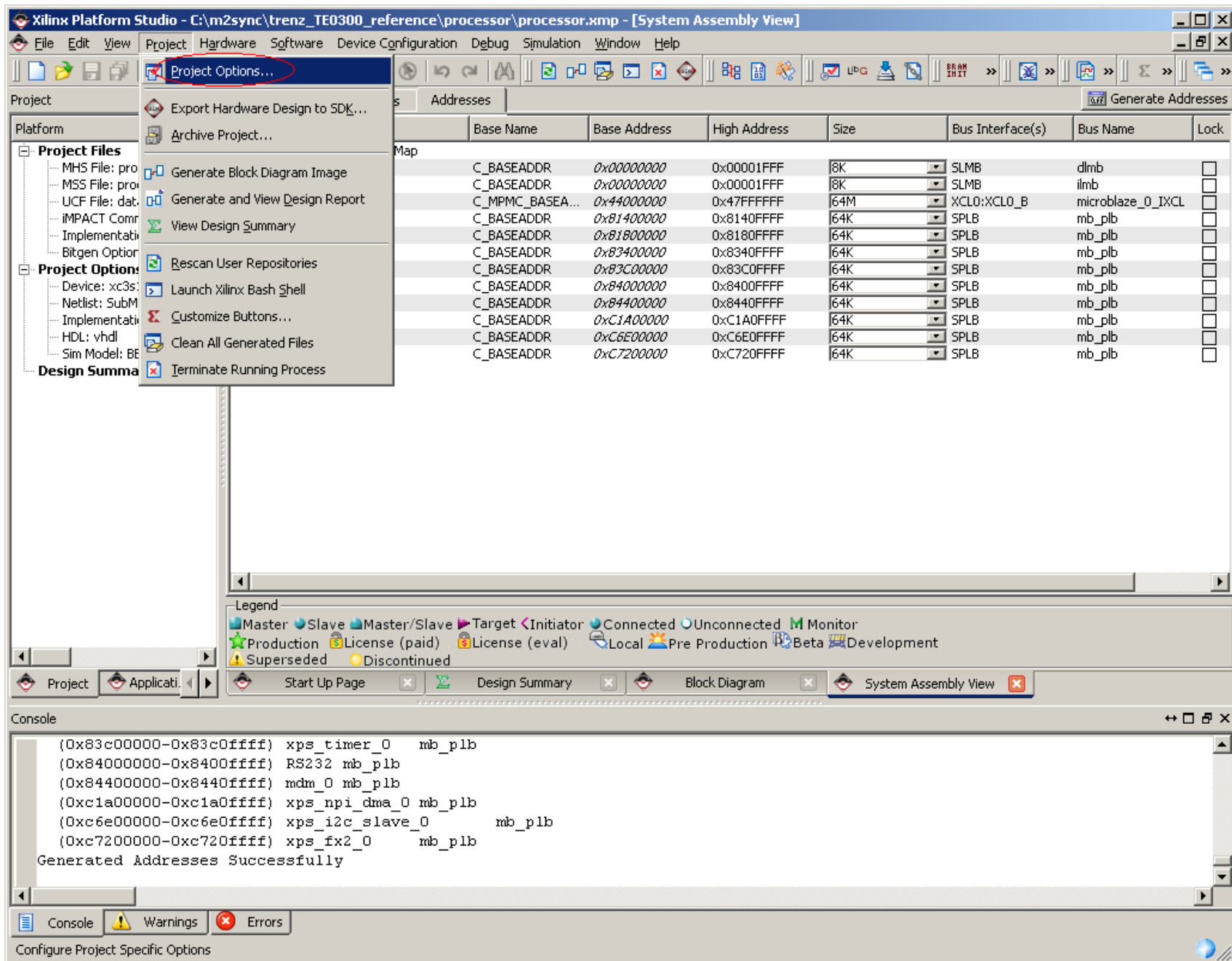
Console

```

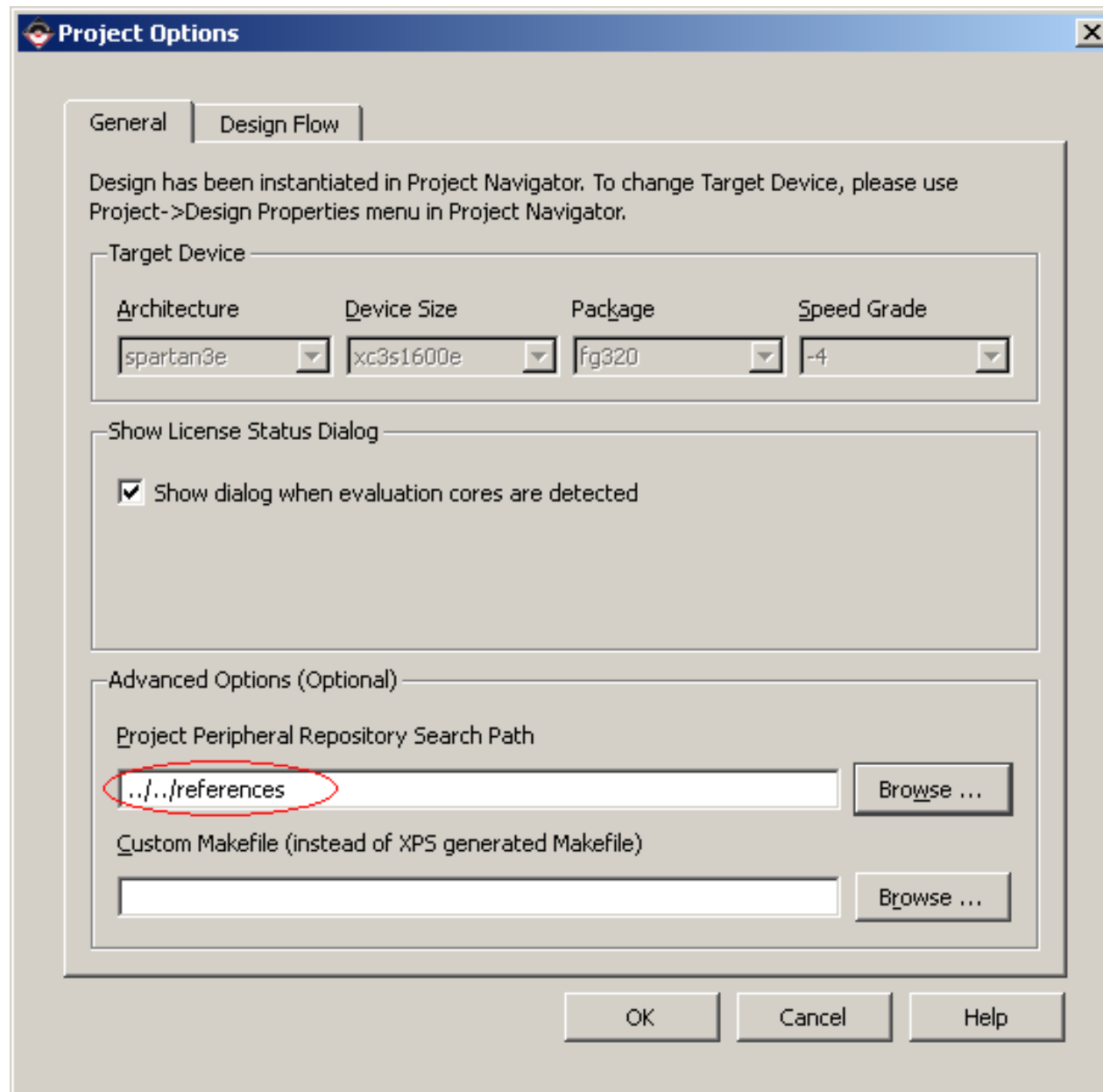
(0x83c00000-0x83c0ffff) xps_timer_0 mb_plb
(0x84000000-0x8400ffff) RS232 mb_plb
(0x84400000-0x8440ffff) mdm_0 mb_plb
(0xc1a00000-0xc1a0ffff) xps_npi_dma_0 mb_plb
(0xc6e00000-0xc6e0ffff) xps_i2c_slave_0 mb_plb
(0xc7200000-0xc720ffff) xps_fx2_0 mb_plb
Generated Addresses Successfully
  
```

Console Warnings Errors

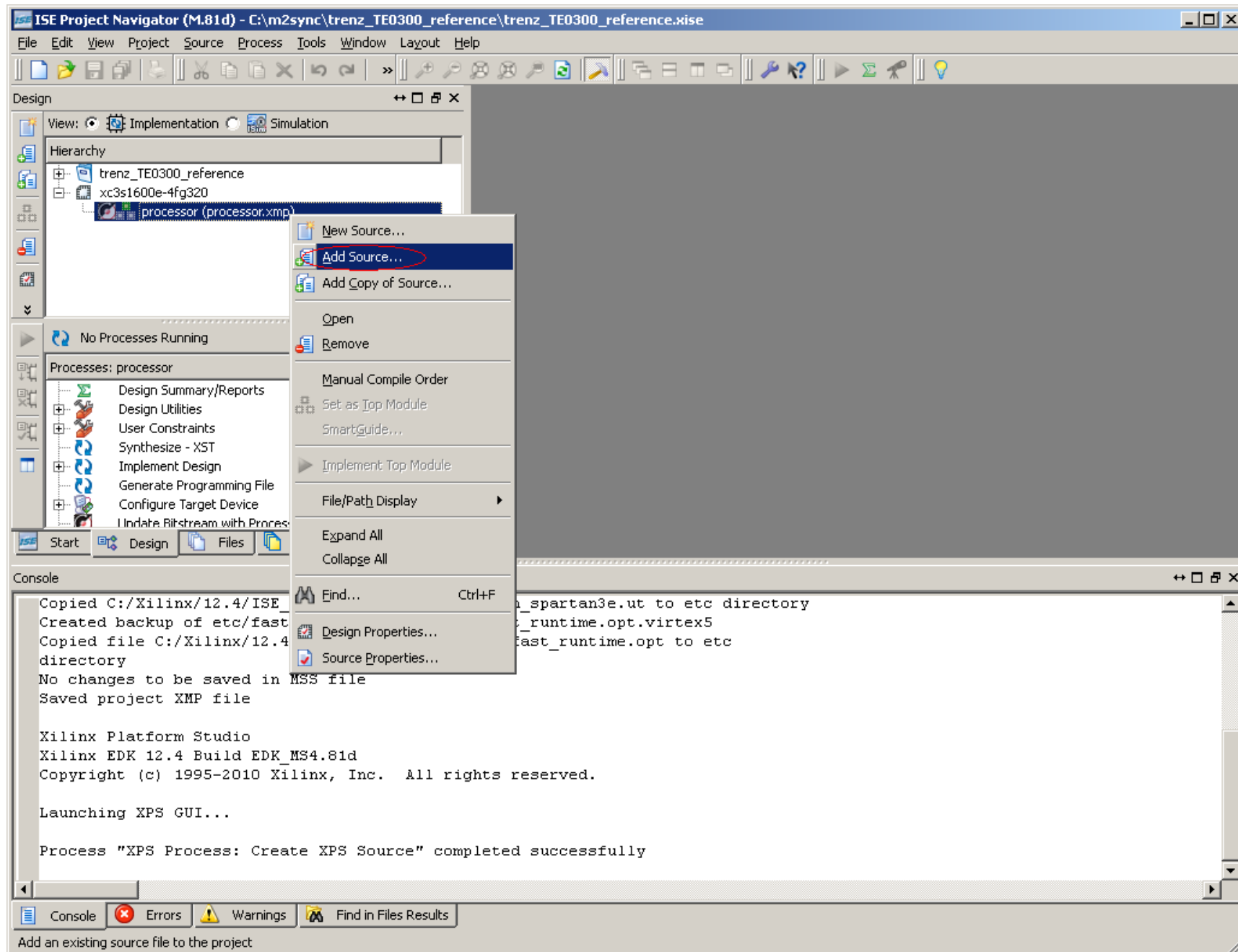
switch to Addresses tab and re-generate addresses



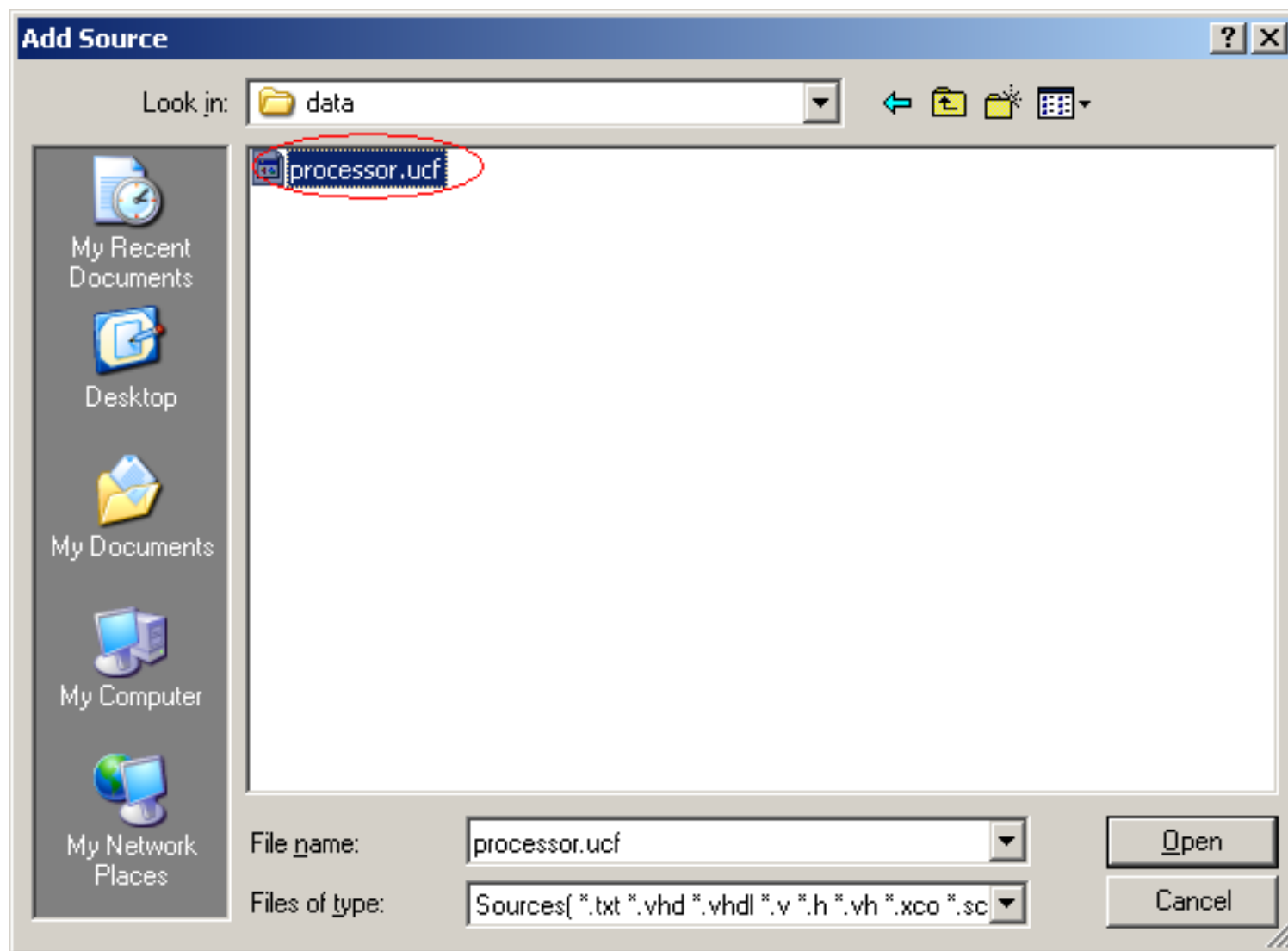
launch Project Options



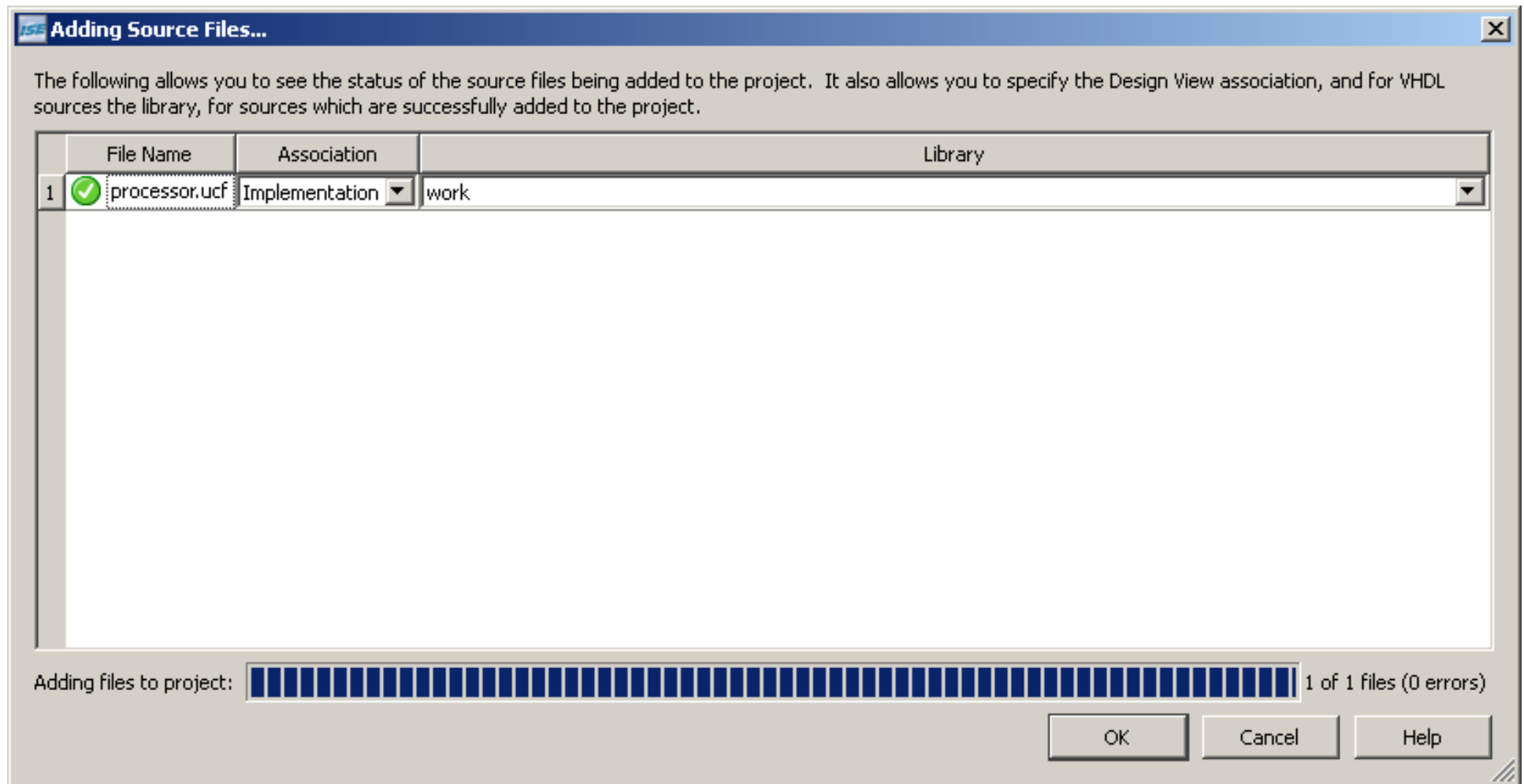
provide path to the private pcores (npi_dma, fx2, i2c_slave) then click OK



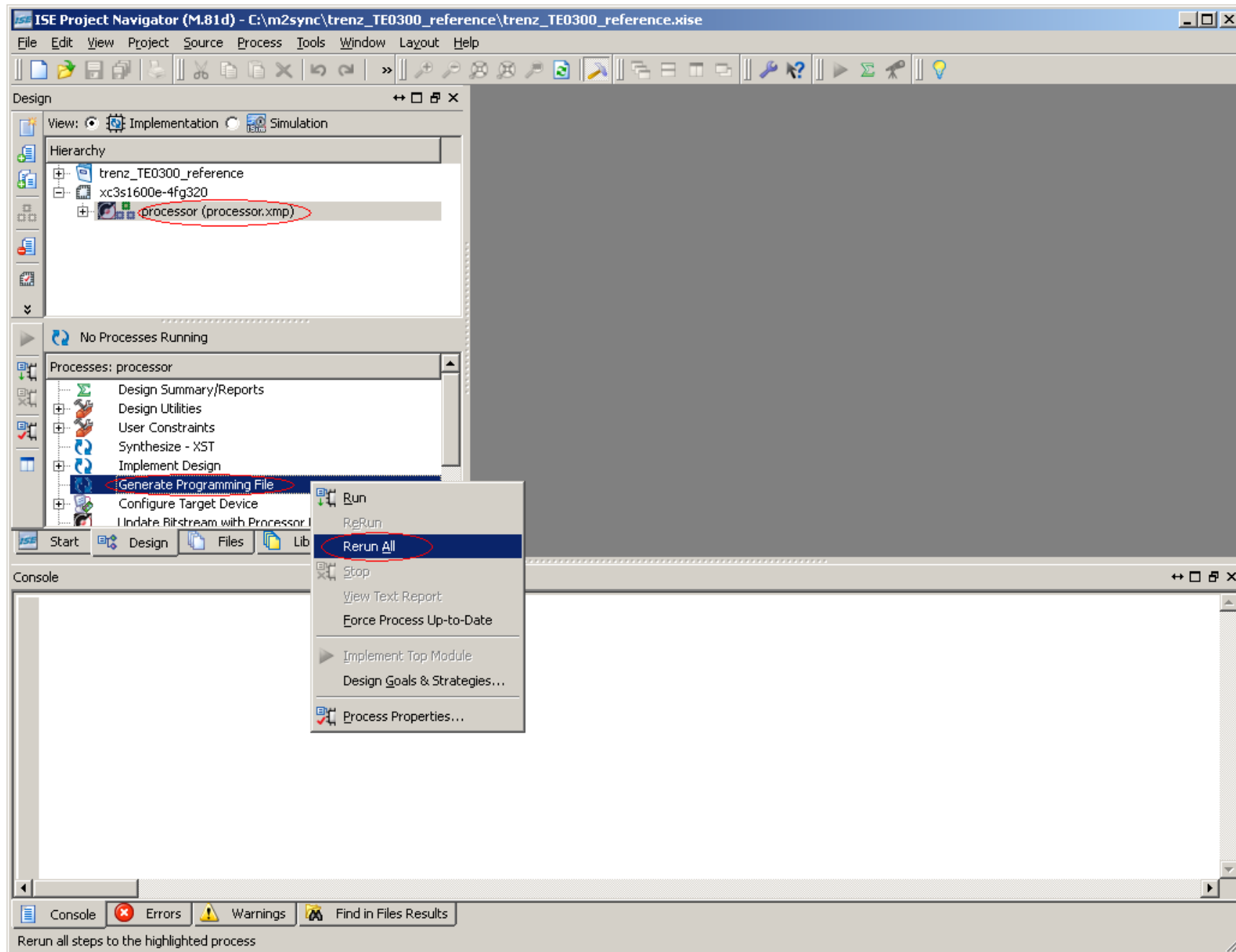
return to ISE Project Navigator and add Source



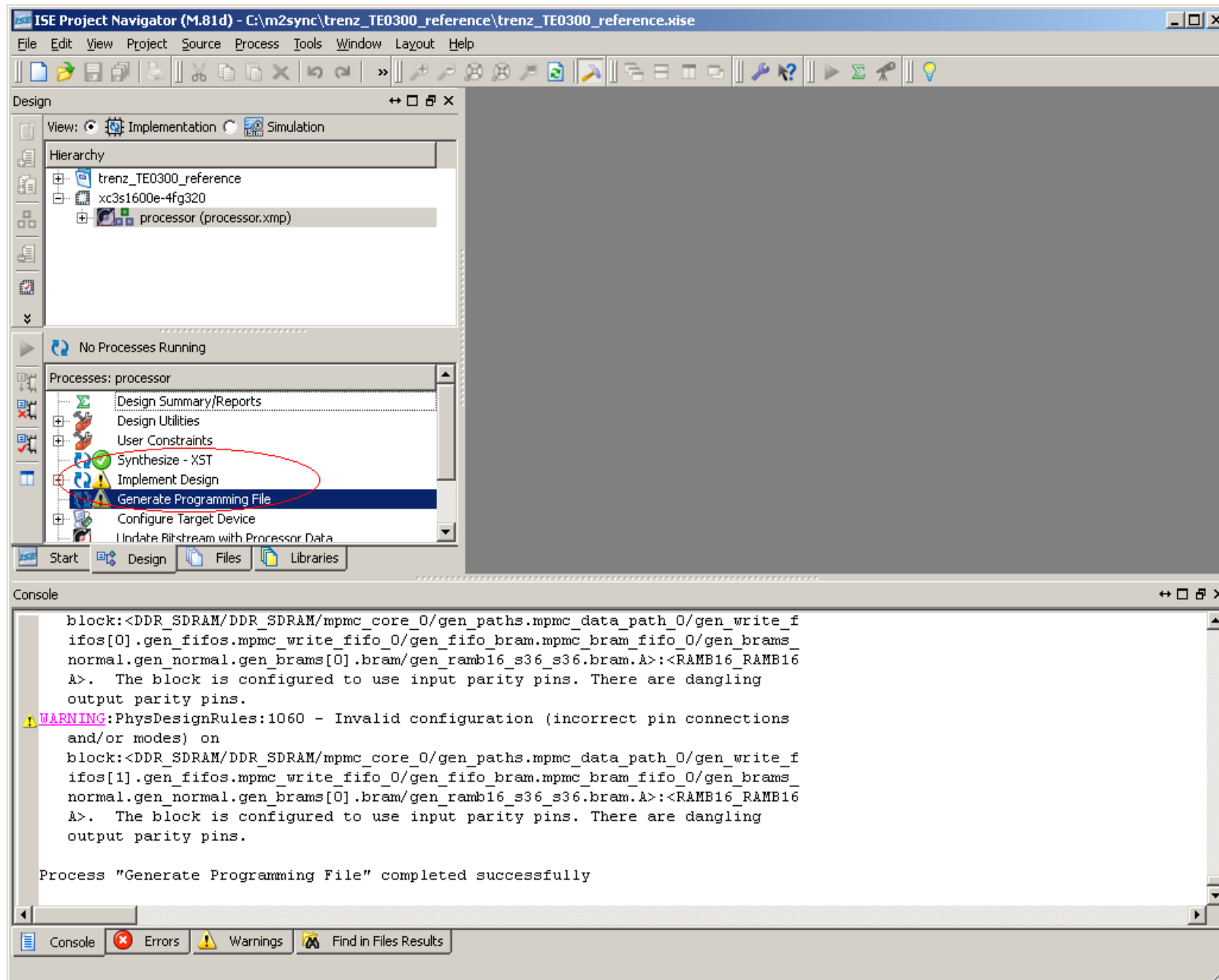
choose processor.ucf from processor/data/ subfolder
then click Open



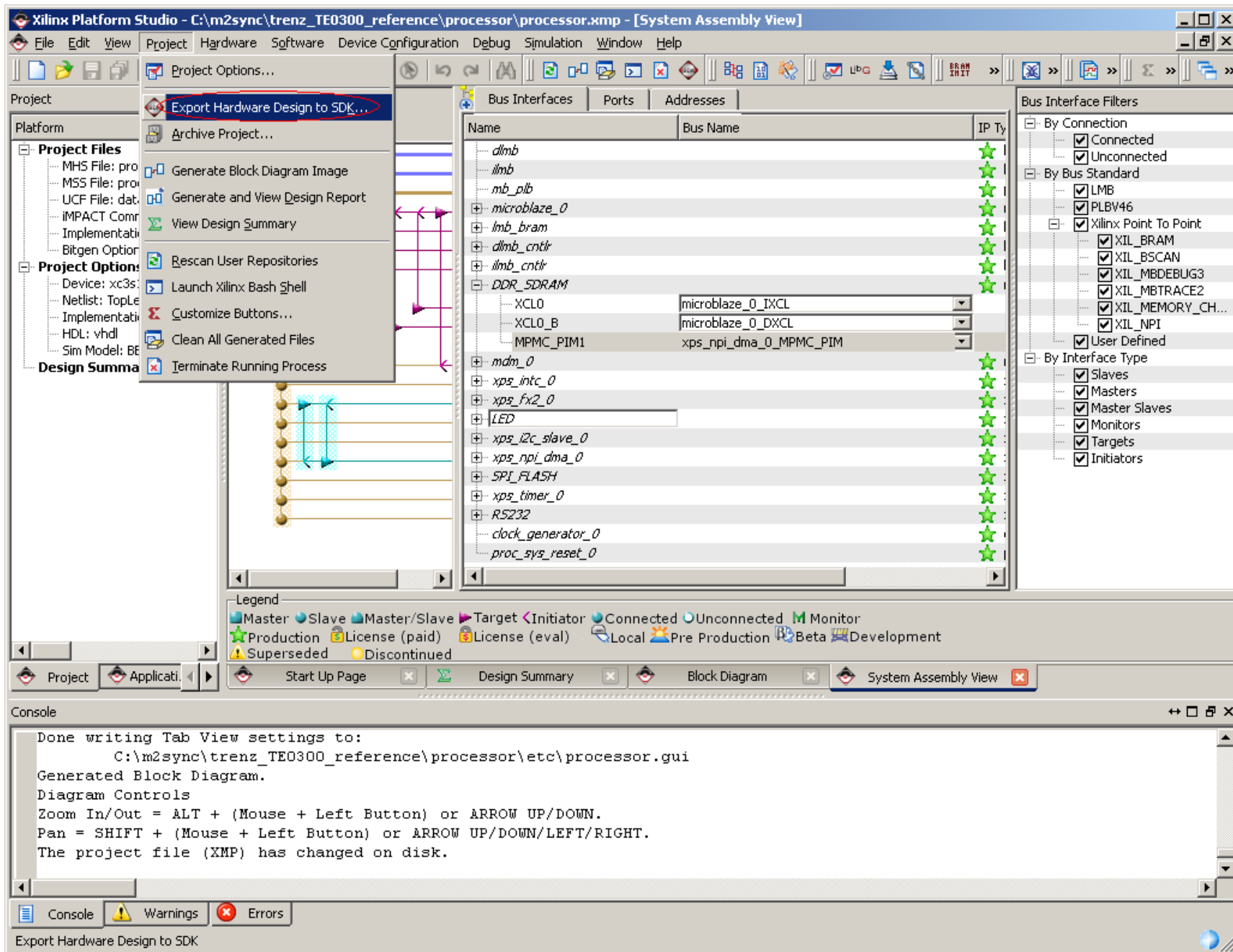
confirm adding Source File by clicking OK



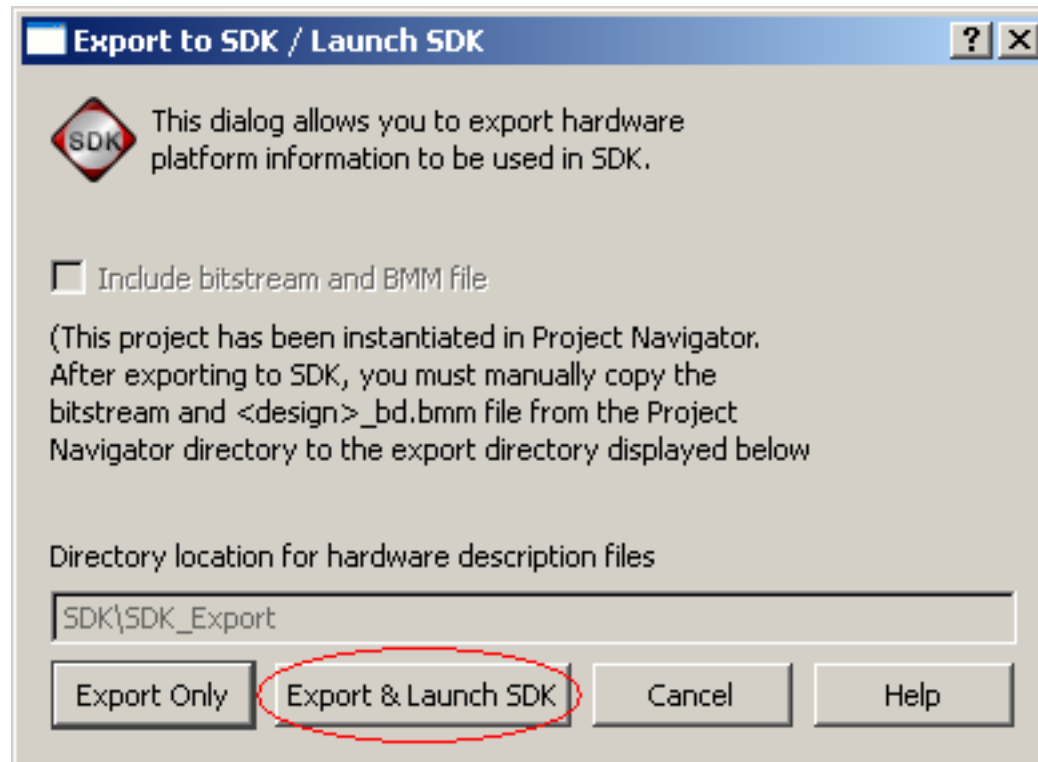
step on processor.xmp, choose Generate Programming File and click Rerun All



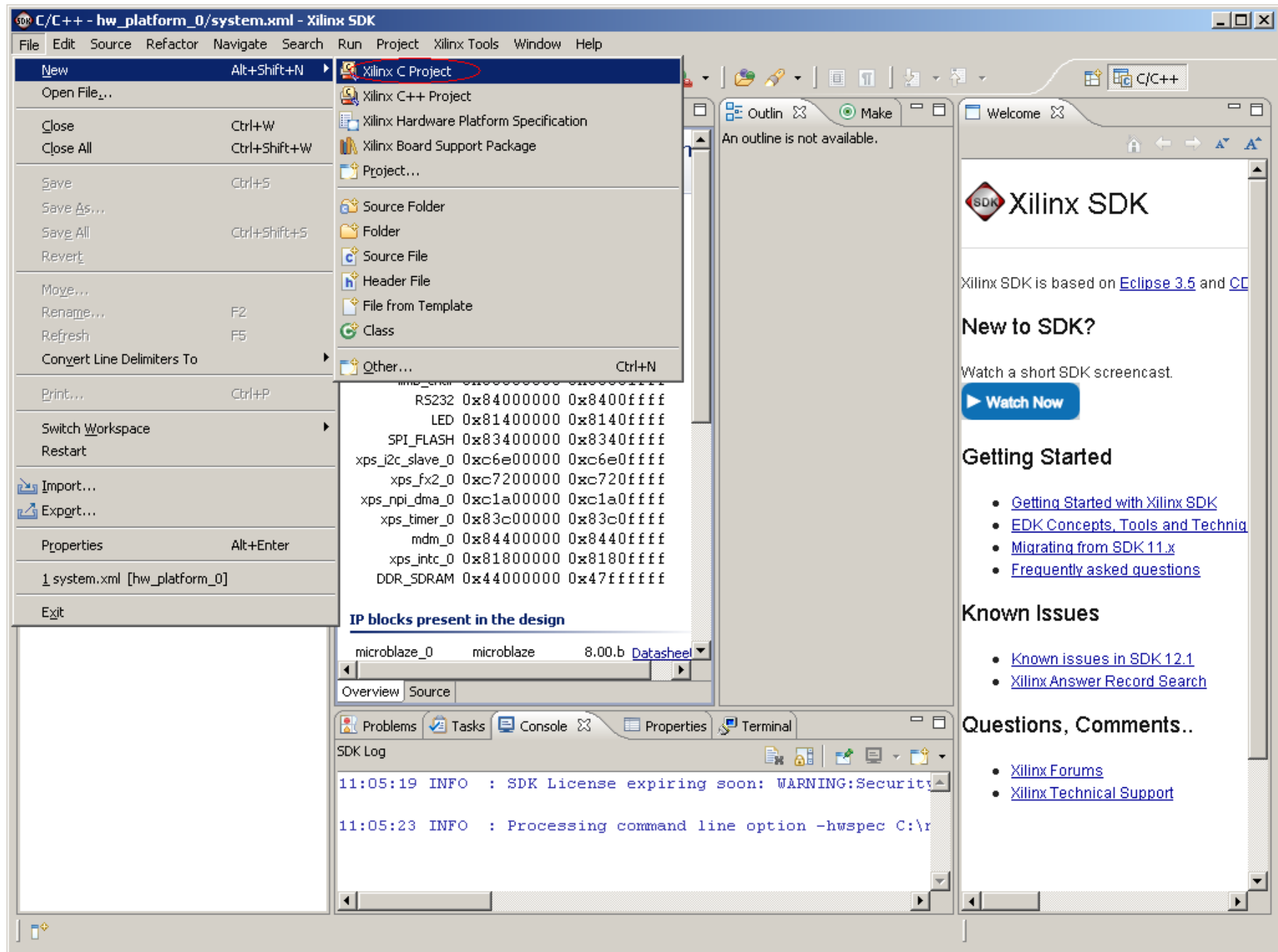
confirm generation success and return to Xilinx
Platform Studio



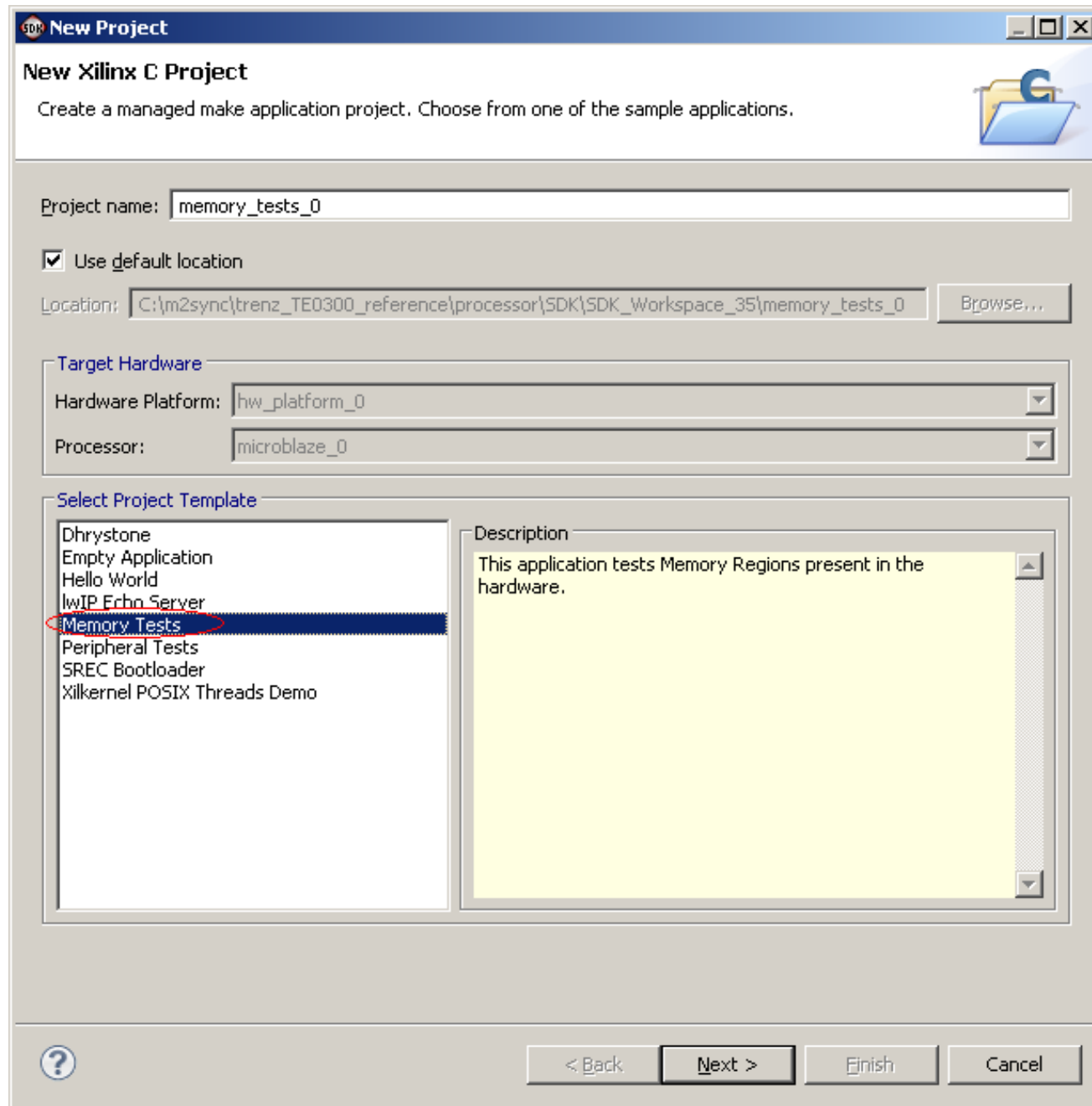
choose from menu Export Hardware Design to SDK



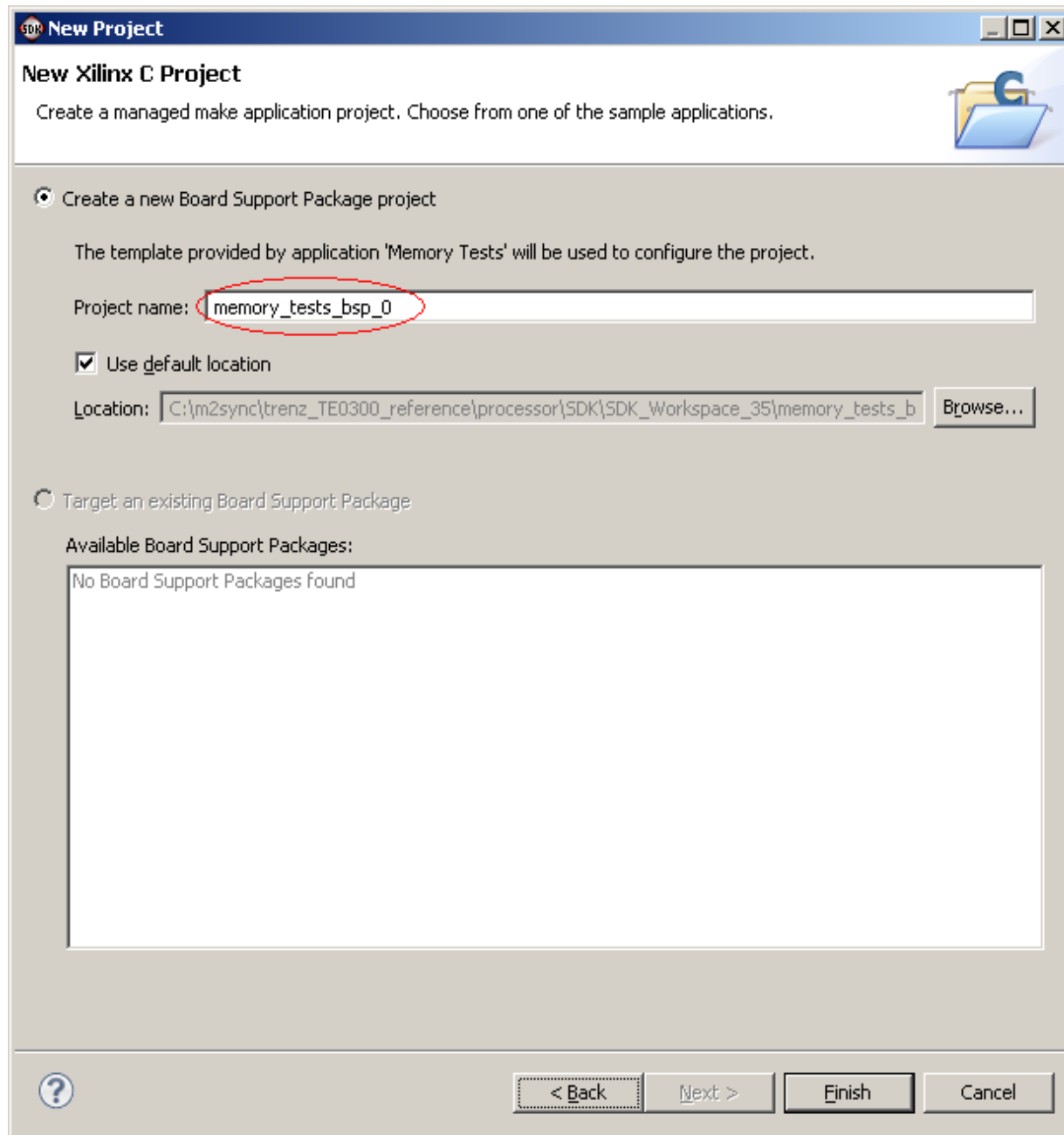
because Xilinx SDK isn't running yet, choose Export & Launch SDK button



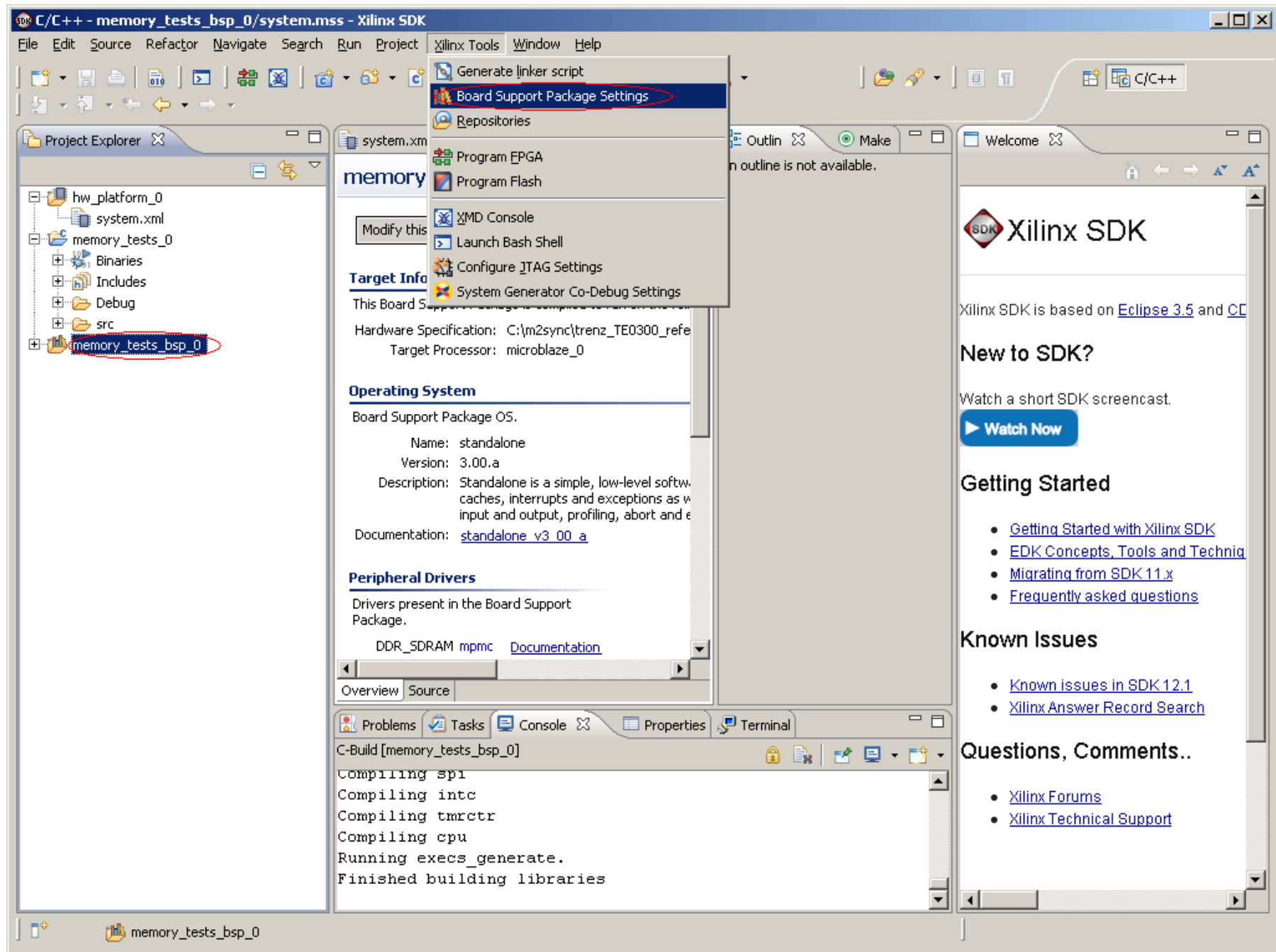
from SDK menu choose to create New Xilinx C Project



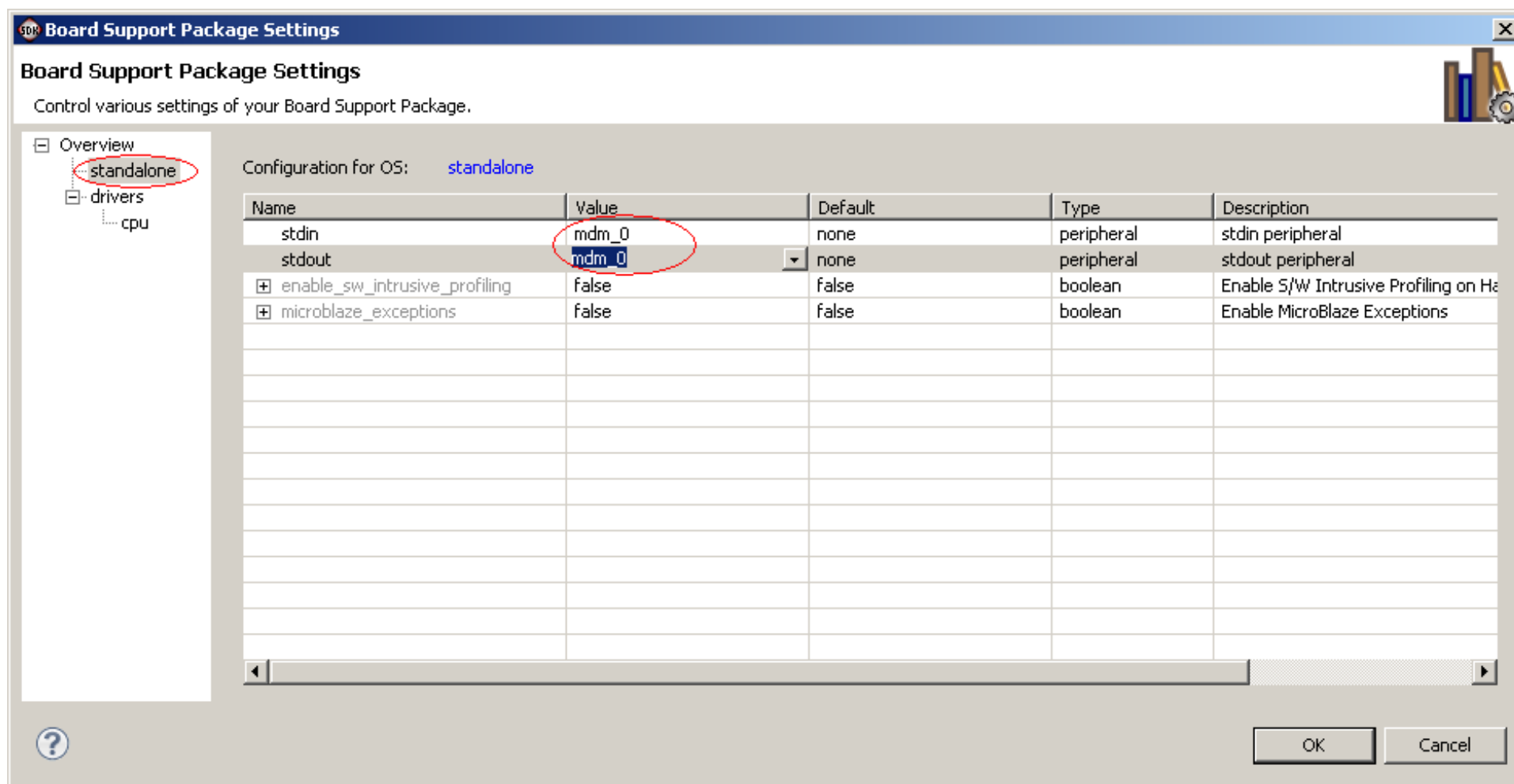
choose Memory Tests template and click Next



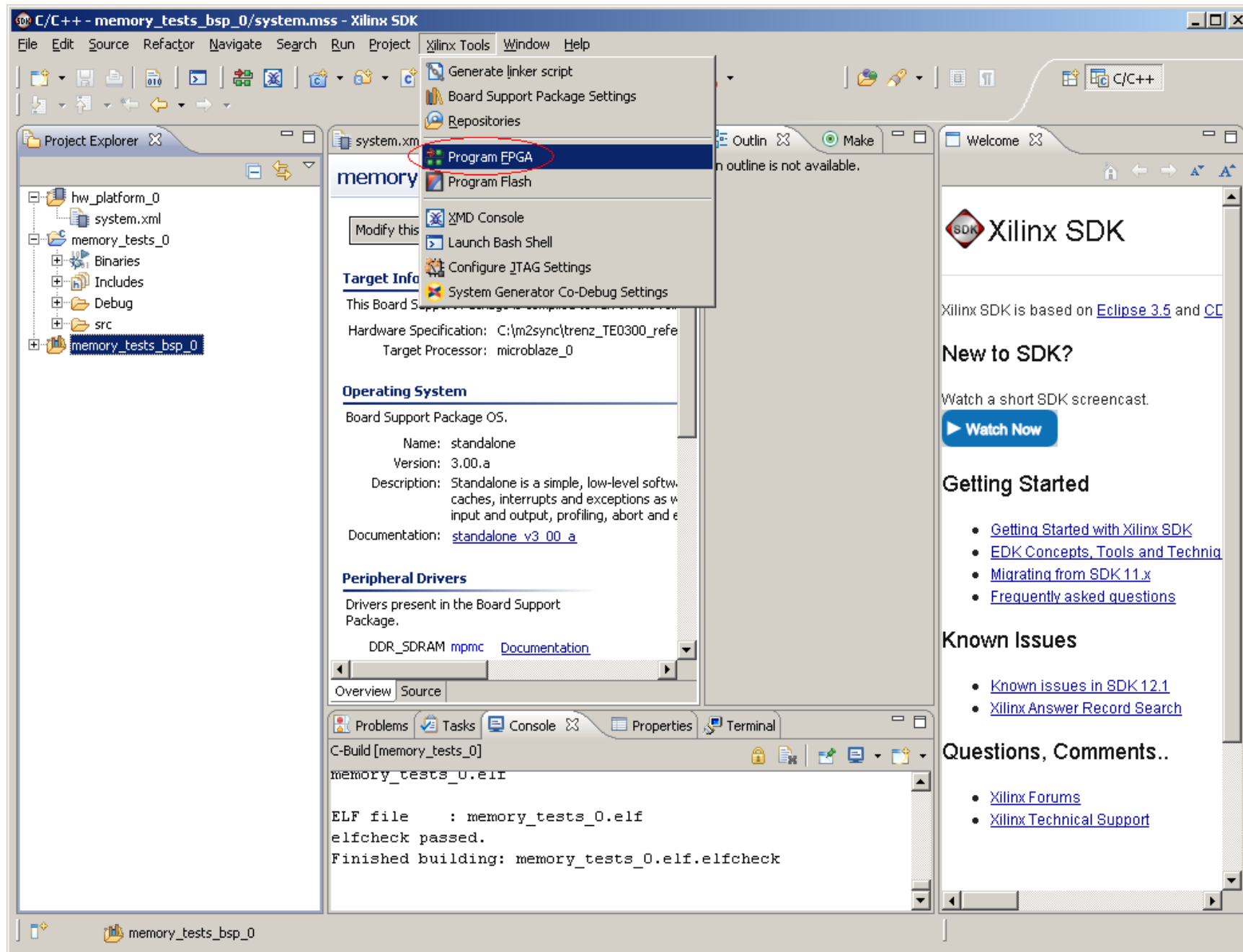
keep default BSP project name
memory_tests_bsp_0 and click Finish



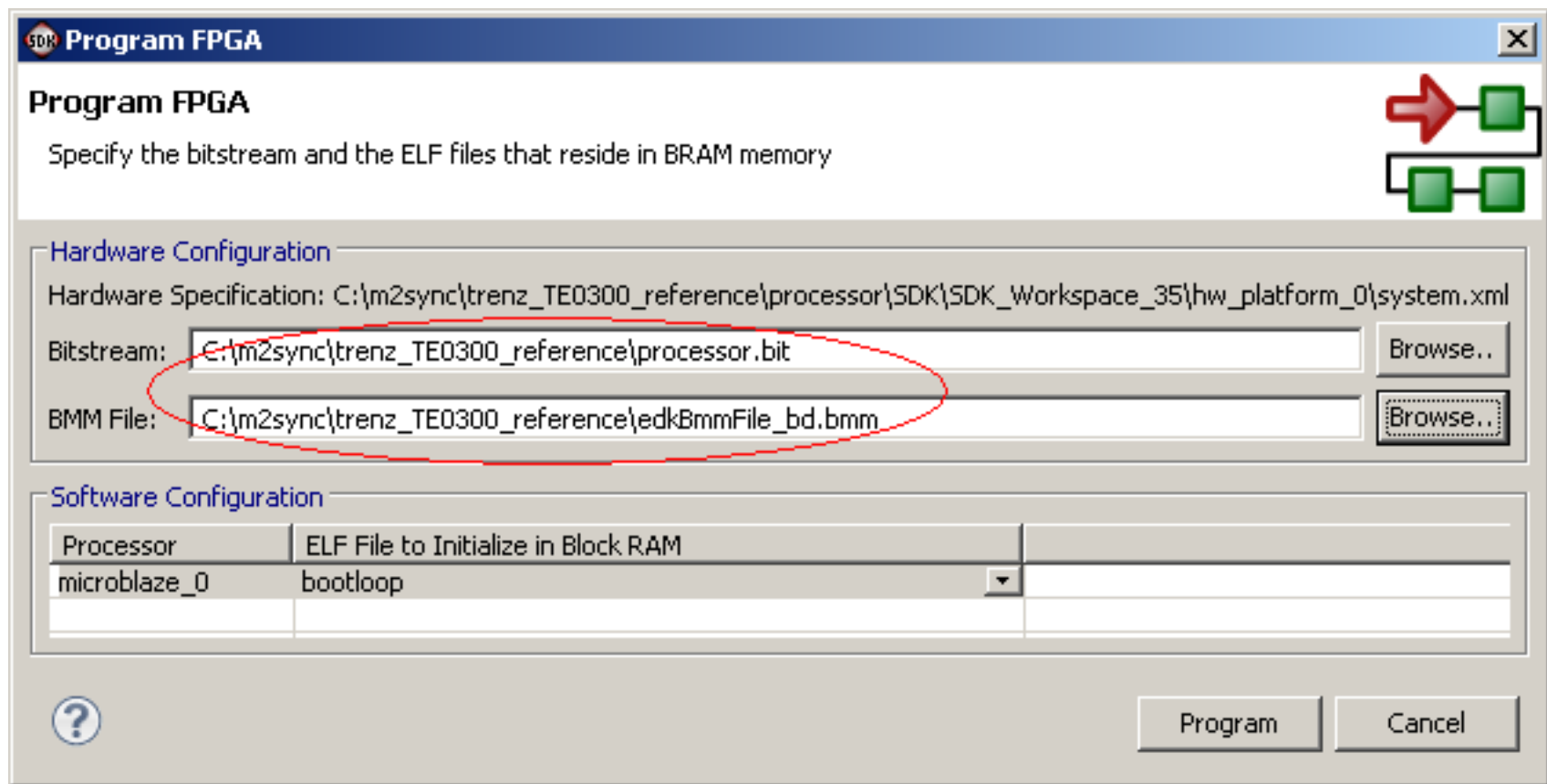
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



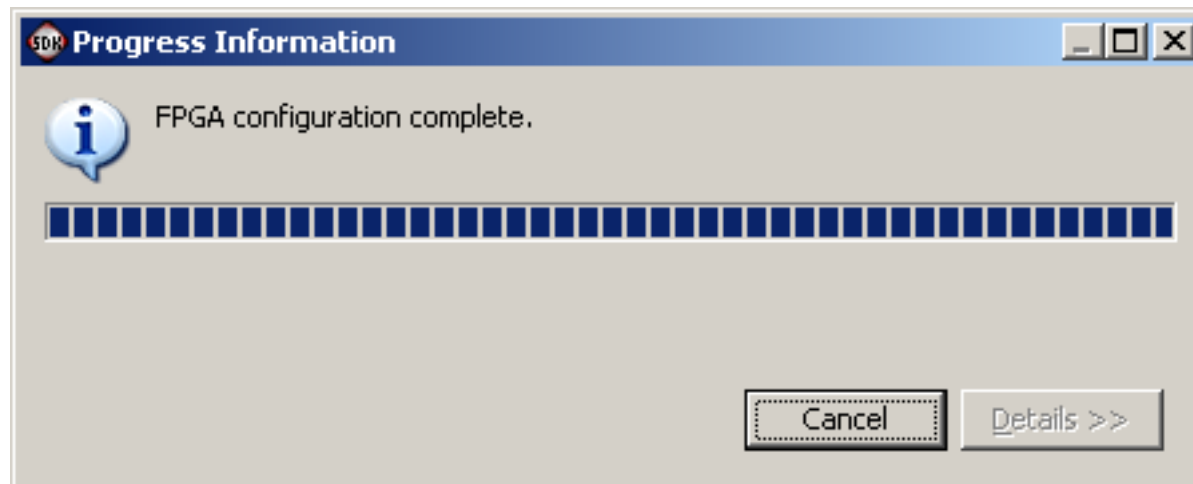
from standalone section apply mdm_0 to stdin and
stdout then click OK



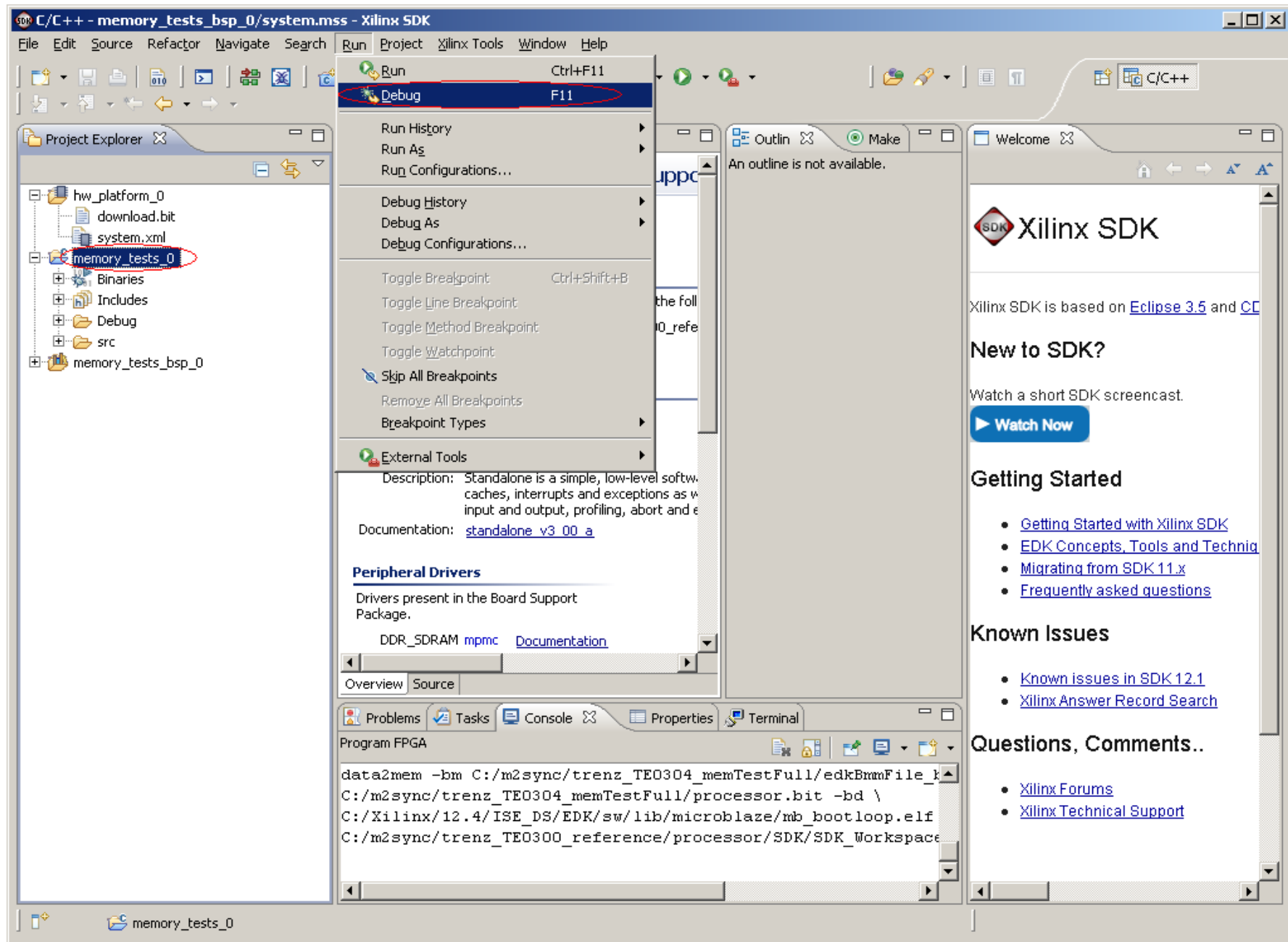
connect the prototype board TE0300 and choose
Program FPGA from menu



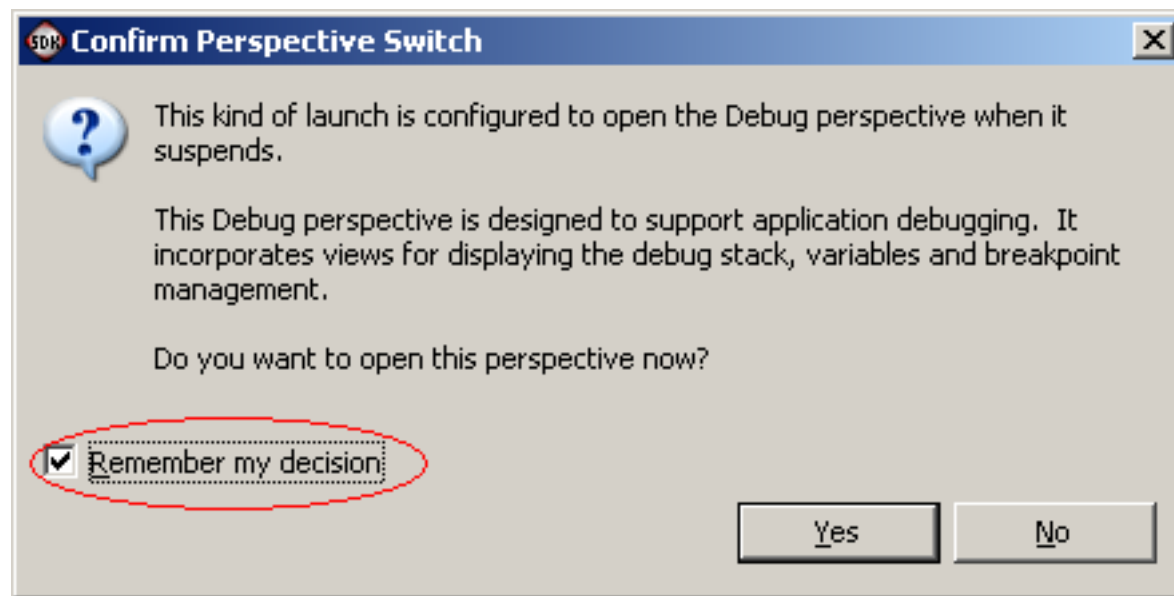
provide correct Bistream and BMM files then click
Program



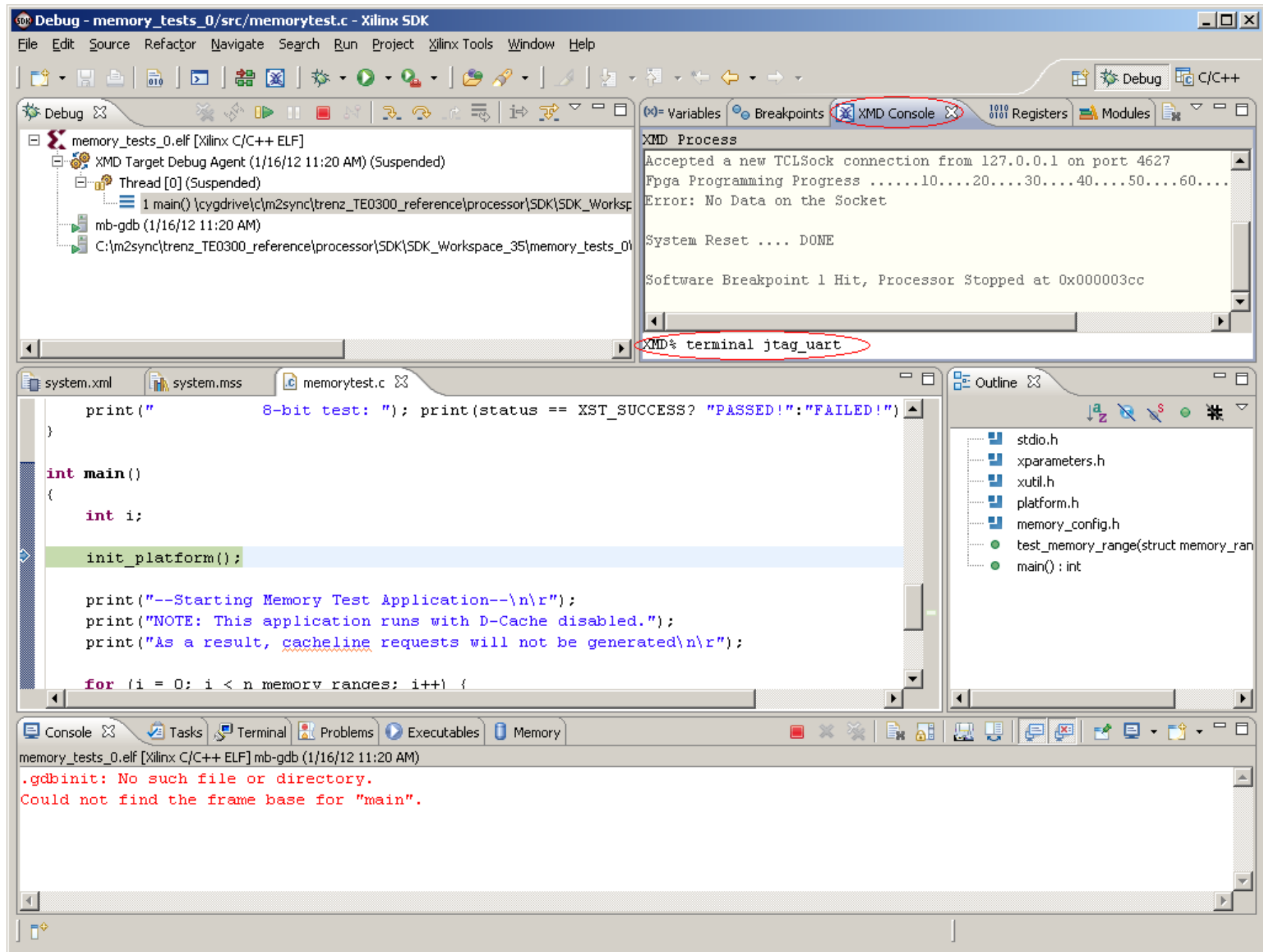
wait for FPGA programming completion



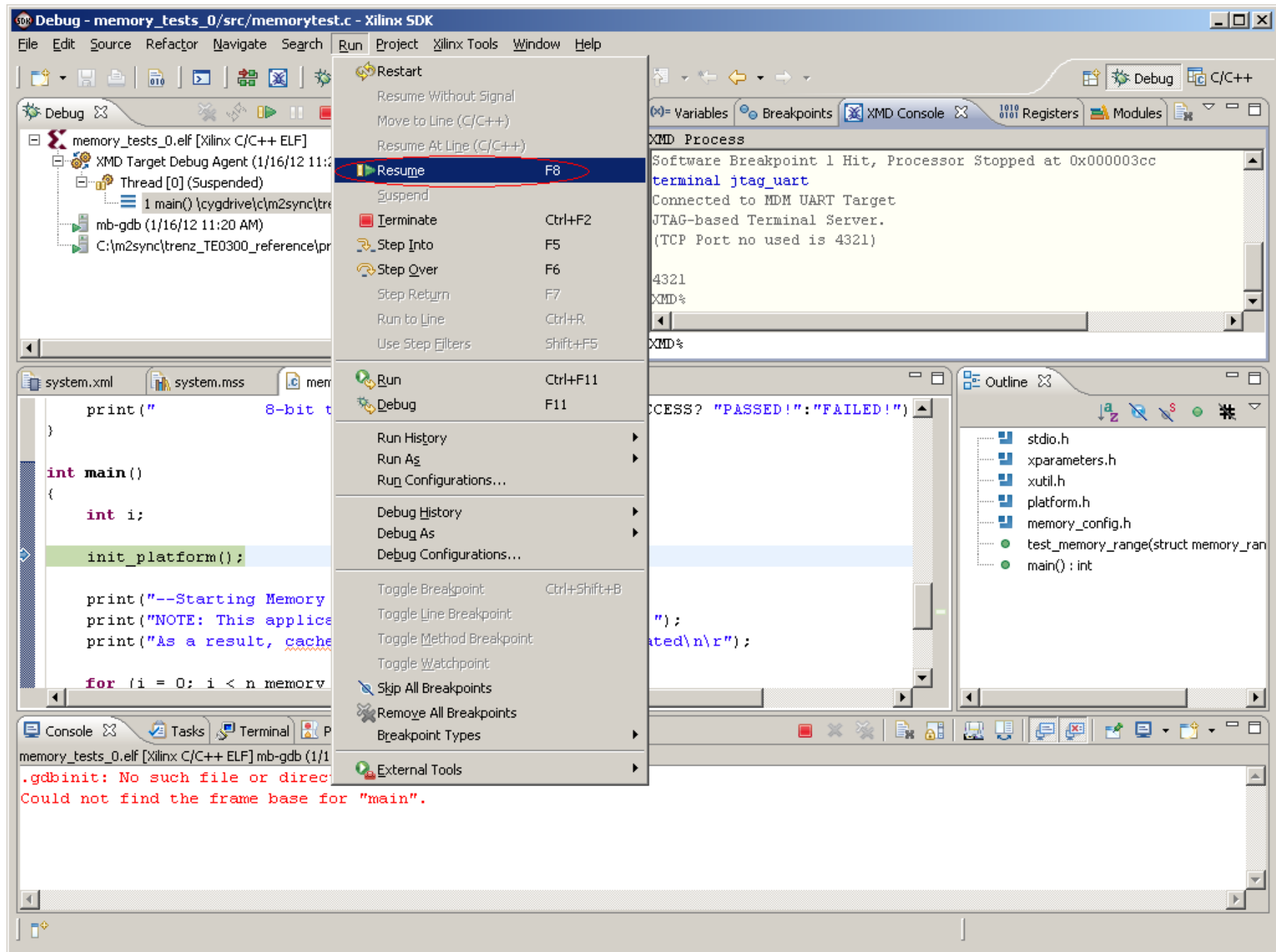
step on memory_tests_0 application and choose
Debug menu



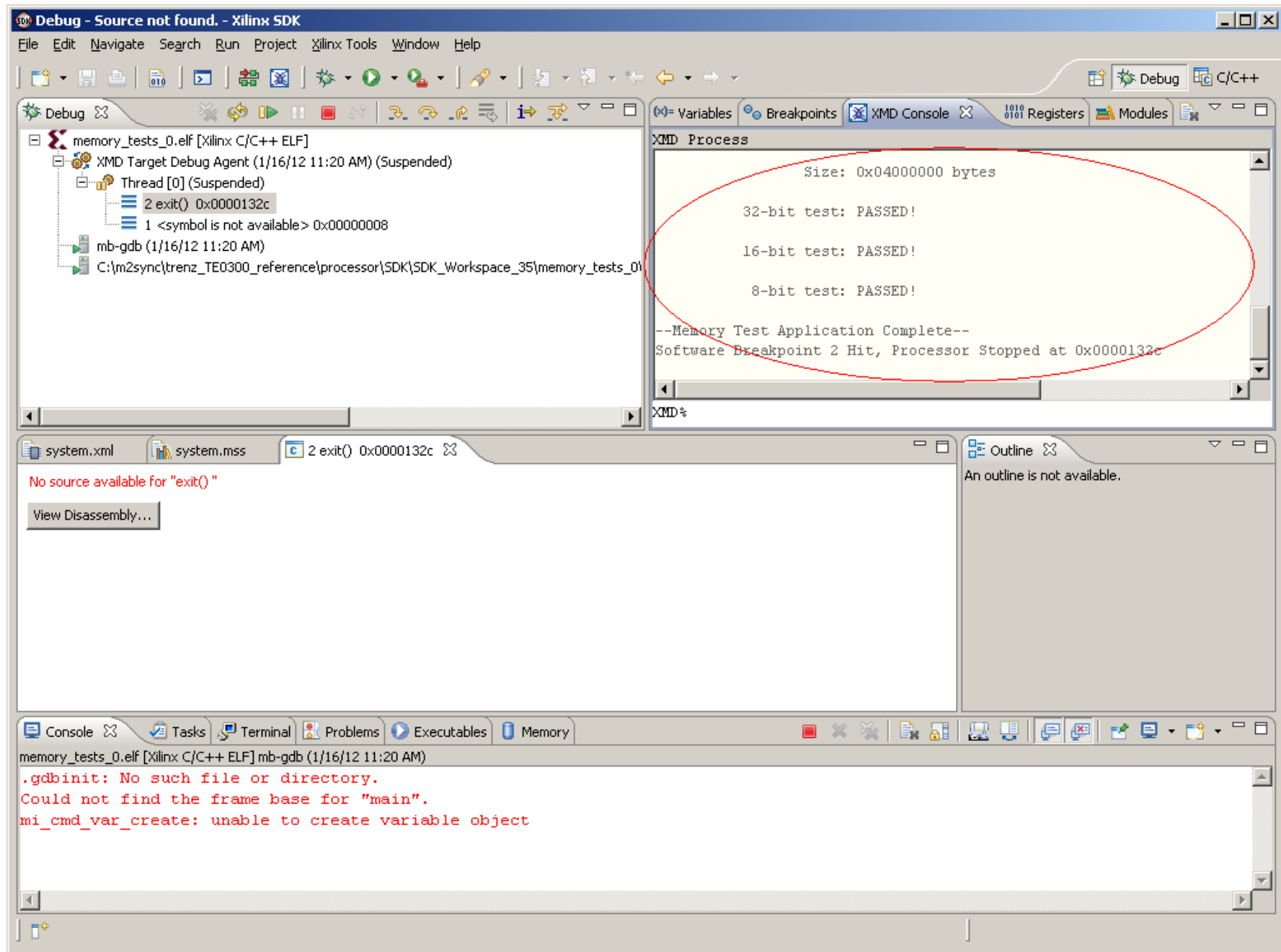
choose remember decision and confirm switching to Debug design by clicking Yes button



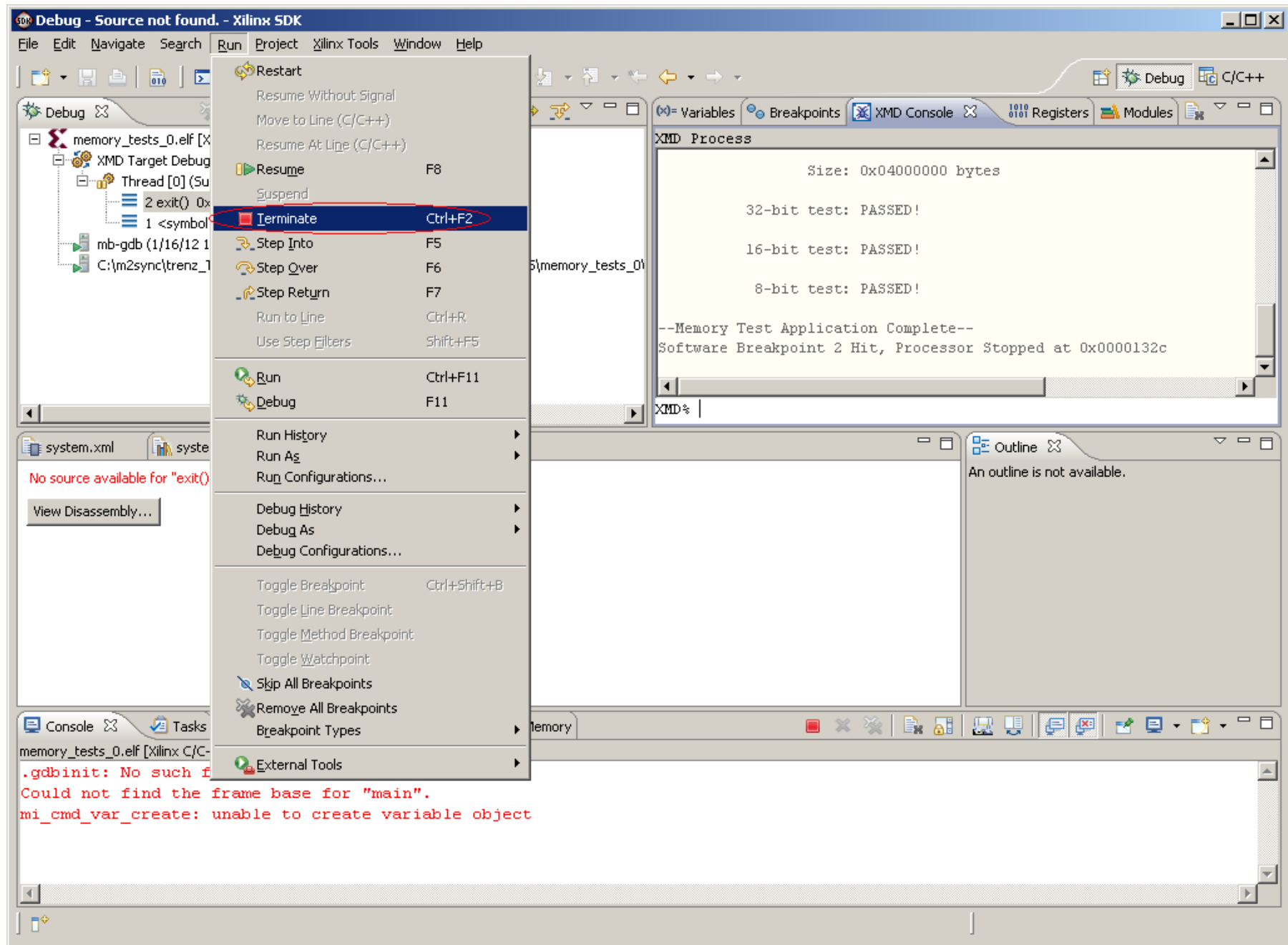
switch to XMD Console tab and type command
"terminal jtag_uart"



resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application

TE0300 board configuration complete

external memory configuration
confirmed with test application