

TE0600 platform

reference project creation sequence
PLB bus based

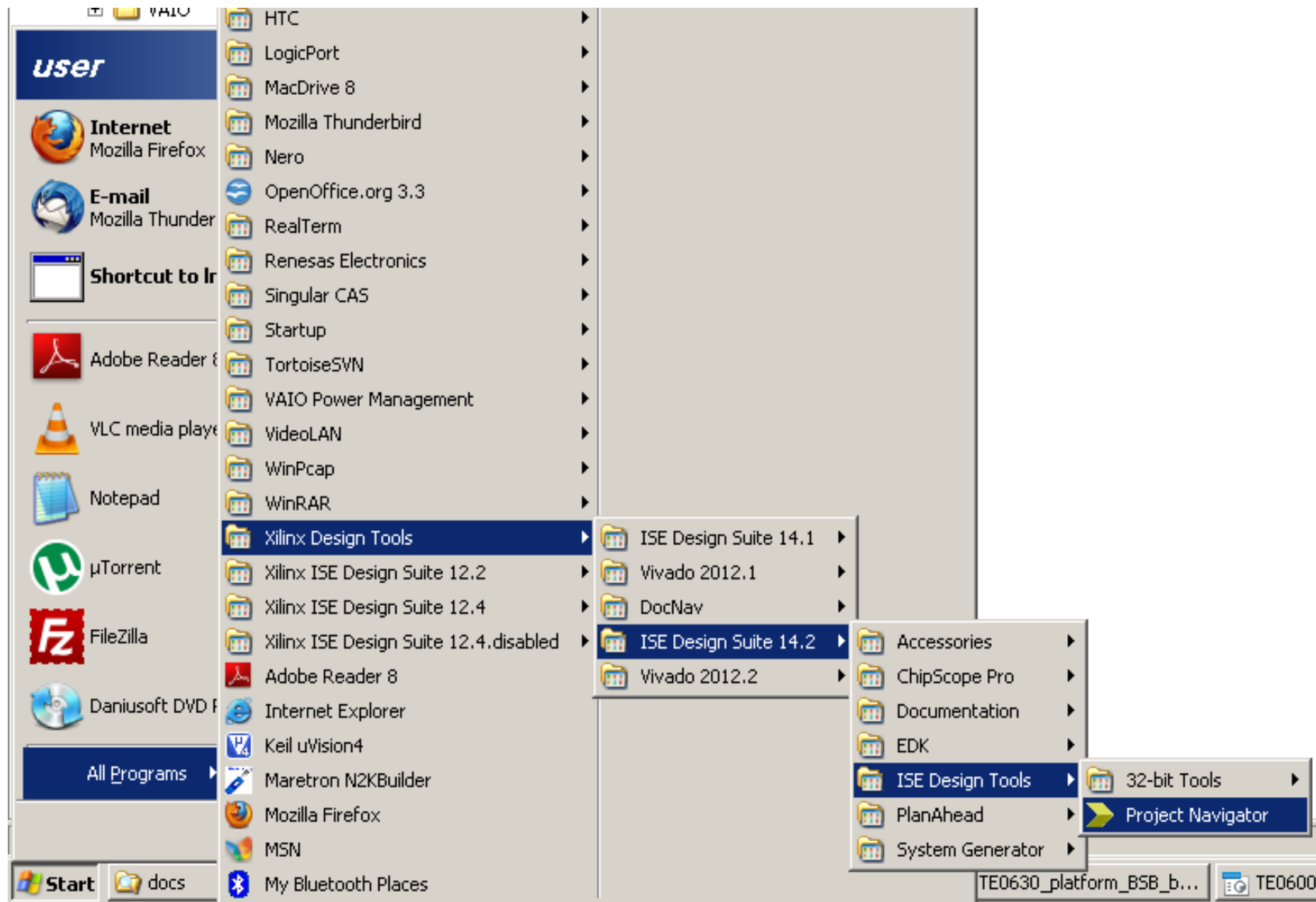
Special Note:

Make sure BSB files are copied into
`\Xilinx\14.2\ISE_DS\EDK\data\board`

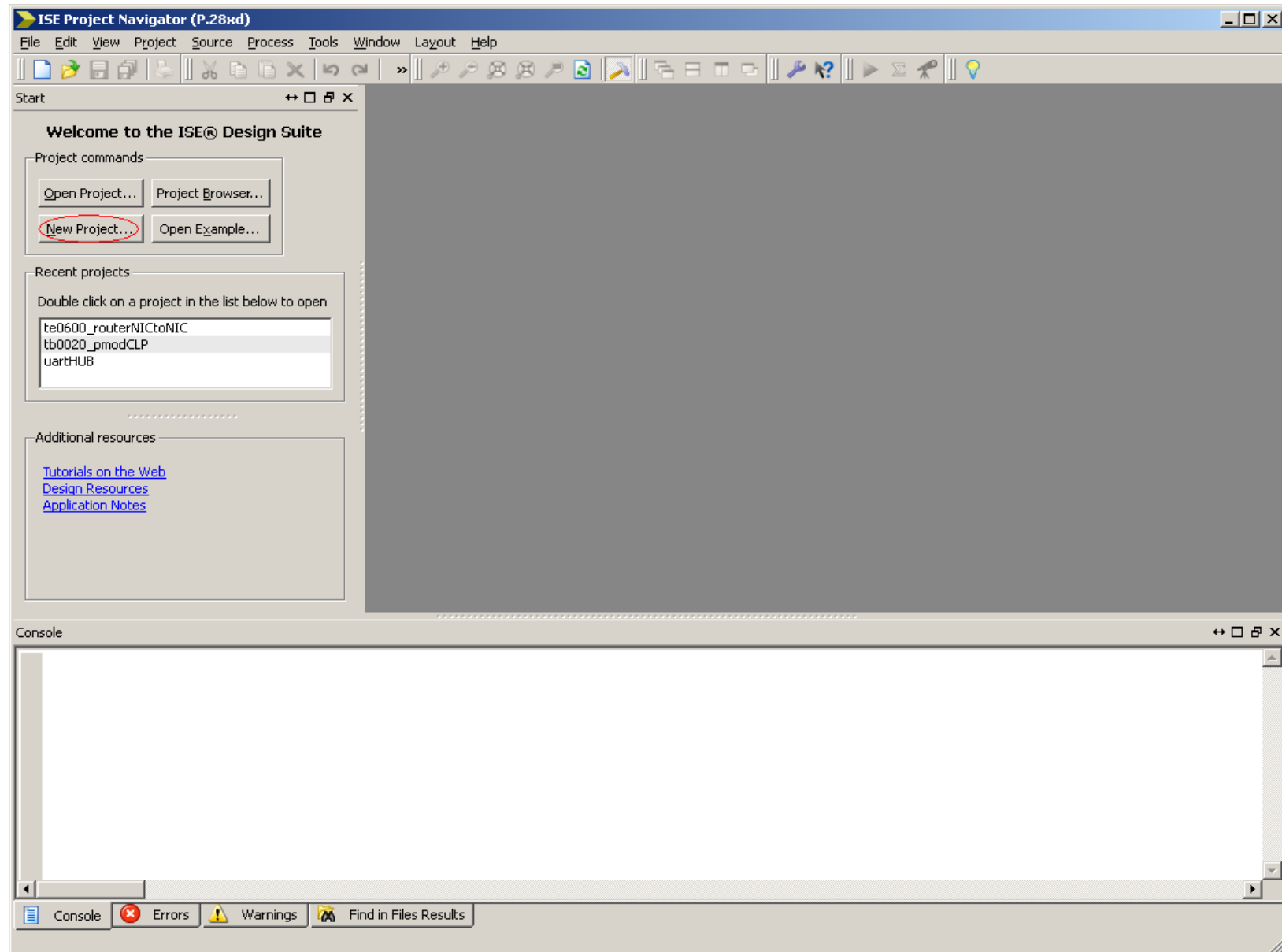
Make sure private pcores are copied into
`\Xilinx\14.2\ISE_DS\EDK\data\wizards\BsbCores\pcores`

Before running this manual

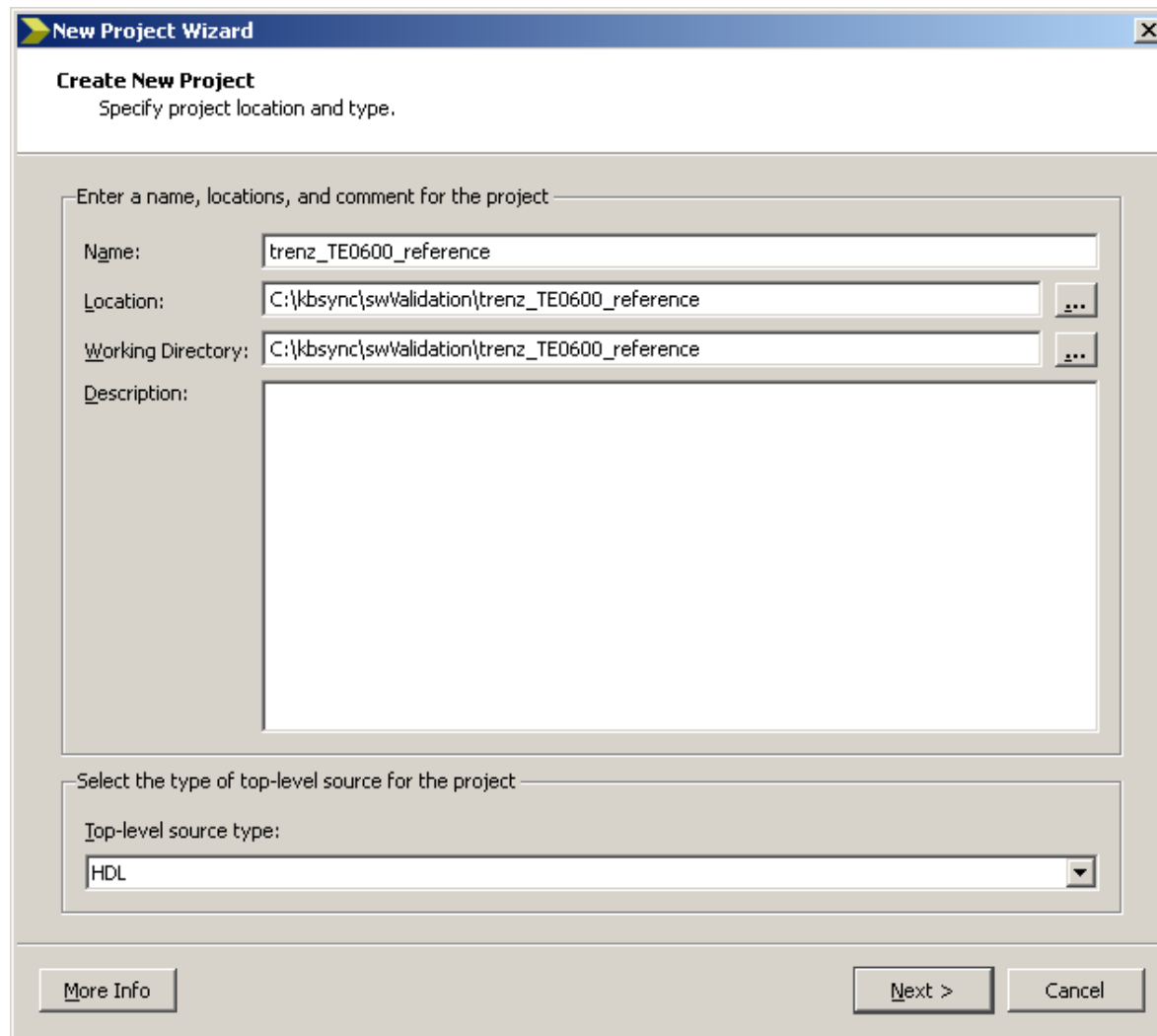
start Xilinx ISE 14 Project Navigator



click button to create a new project



choose project name, then click Next



The image shows a 'New Project Wizard' dialog box with a blue title bar and a close button. The main area is titled 'Create New Project' with the instruction 'Specify project location and type.' Below this, there is a section 'Enter a name, locations, and comment for the project' containing four fields: 'Name' (filled with 'trenz_TE0600_reference'), 'Location' (filled with 'C:\kbsync\swValidation\trenz_TE0600_reference'), 'Working Directory' (filled with 'C:\kbsync\swValidation\trenz_TE0600_reference'), and 'Description' (empty). Each of the first three fields has a browse button (three dots) to its right. Below this section is another section 'Select the type of top-level source for the project' with a 'Top-level source type' dropdown menu currently set to 'HDL'. At the bottom, there are three buttons: 'More Info', 'Next >', and 'Cancel'.

New Project Wizard

Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name: trenz_TE0600_reference

Location: C:\kbsync\swValidation\trenz_TE0600_reference

Working Directory: C:\kbsync\swValidation\trenz_TE0600_reference

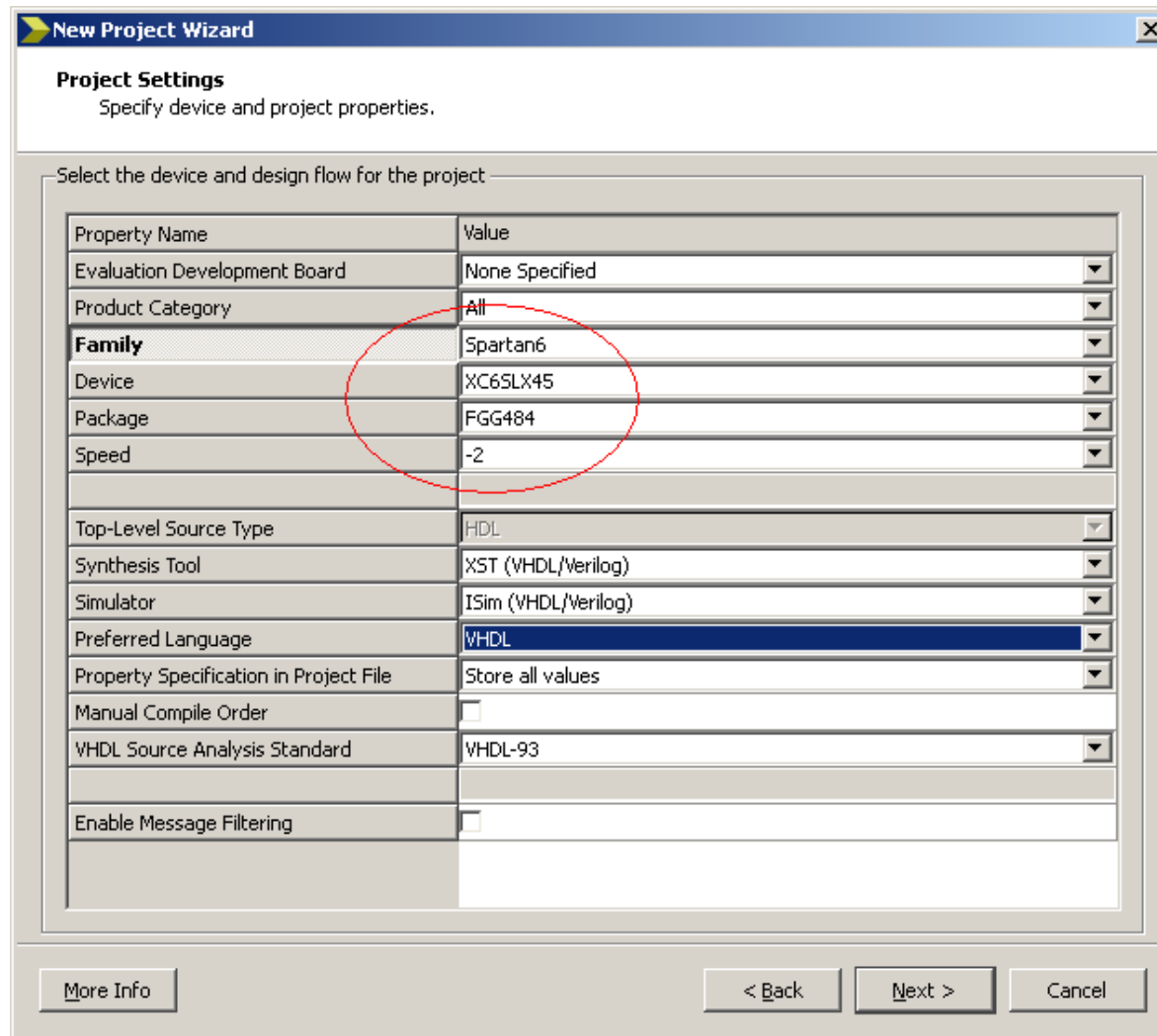
Description:

Select the type of top-level source for the project

Top-level source type:
HDL

More Info Next > Cancel

provide correct Family, Device, Package and Speed,
then click Next

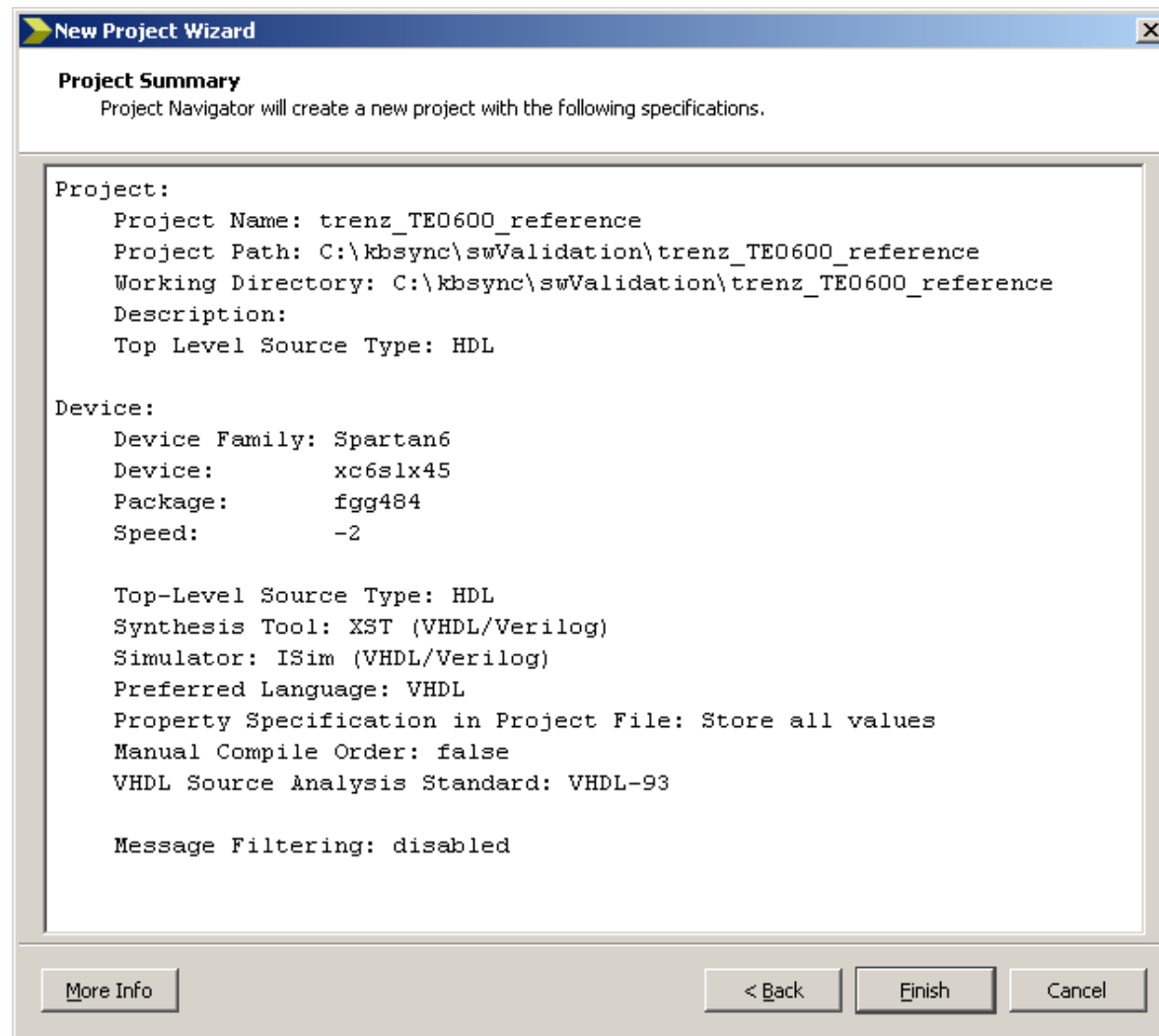


The image shows the 'New Project Wizard' dialog box, specifically the 'Project Settings' step. The title bar reads 'New Project Wizard' with a close button. Below the title bar, the section is labeled 'Project Settings' with the instruction 'Specify device and project properties.' The main area is titled 'Select the device and design flow for the project'. It contains a table of properties with dropdown menus for most values. A red circle highlights the 'Family', 'Device', 'Package', and 'Speed' rows. The 'Family' is set to 'Spartan6', 'Device' to 'XC6SLX45', 'Package' to 'FGG484', and 'Speed' to '-2'. Other properties include 'Evaluation Development Board' (None Specified), 'Product Category' (All), 'Top-Level Source Type' (HDL), 'Synthesis Tool' (XST (VHDL/Verilog)), 'Simulator' (ISim (VHDL/Verilog)), 'Preferred Language' (VHDL), 'Property Specification in Project File' (Store all values), 'Manual Compile Order' (unchecked), 'VHDL Source Analysis Standard' (VHDL-93), and 'Enable Message Filtering' (unchecked). At the bottom, there are three buttons: 'More Info', '< Back', and 'Next >', and a 'Cancel' button.

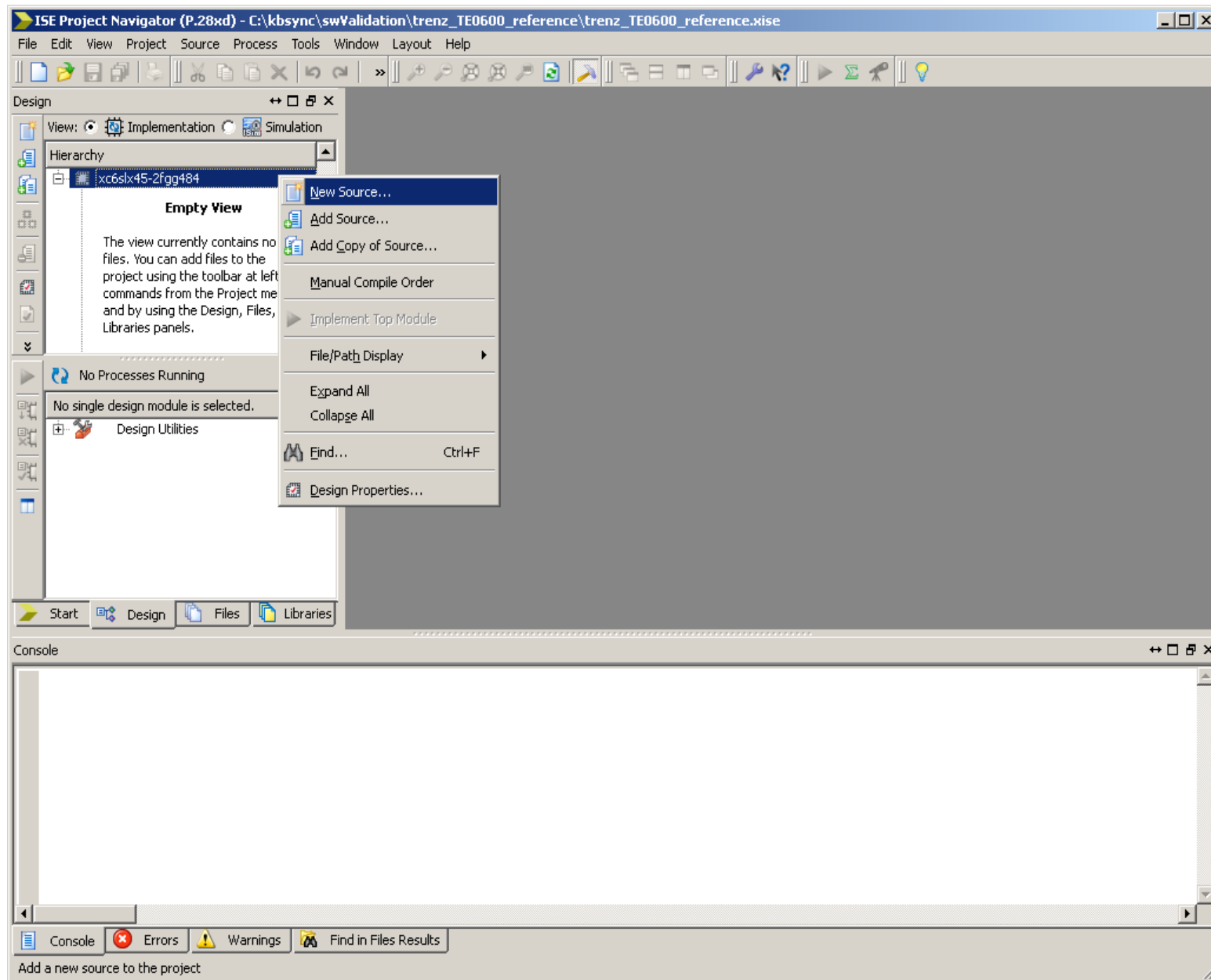
Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan6
Device	XC6SLX45
Package	FGG484
Speed	-2
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

More Info < Back Next > Cancel

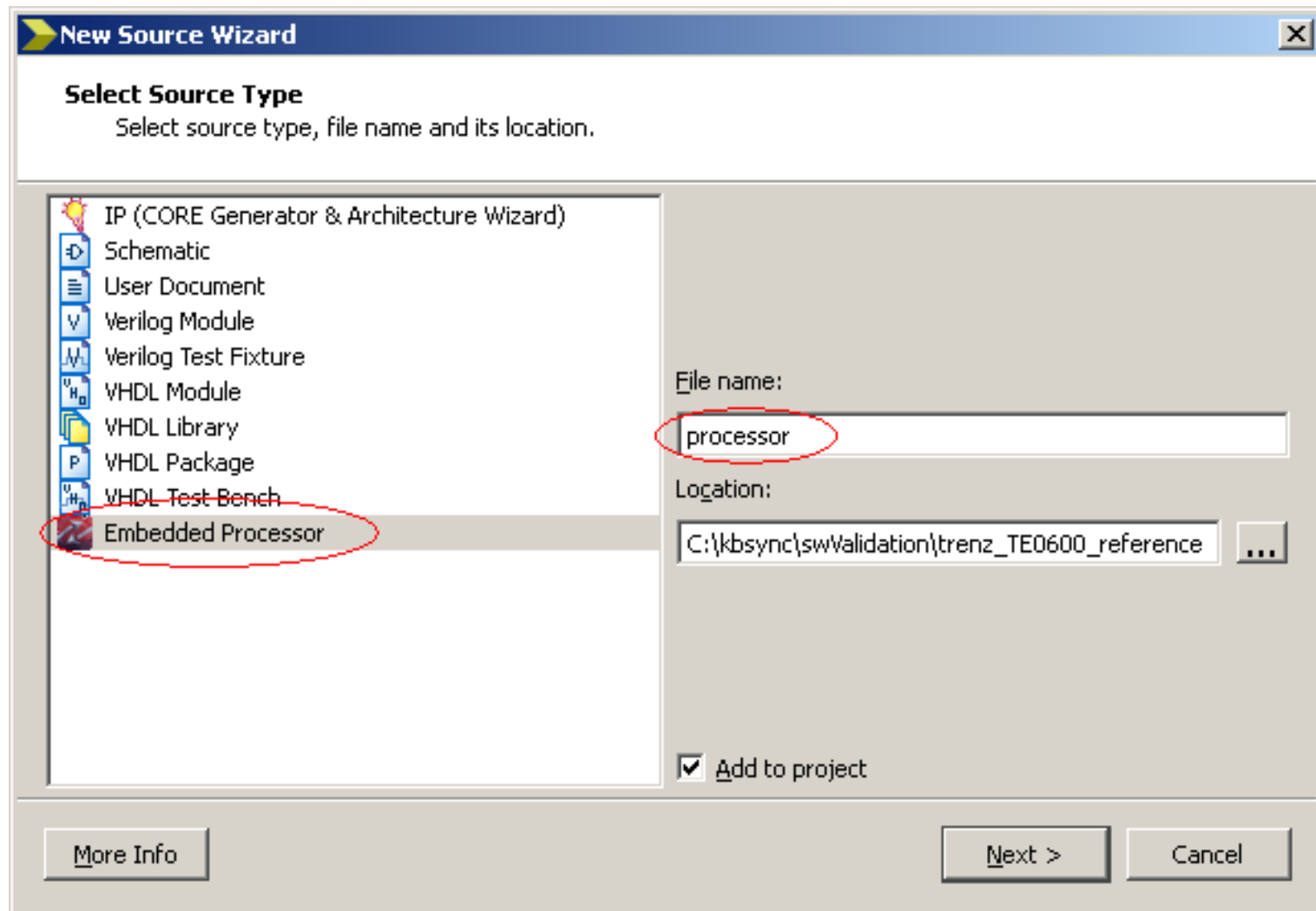
verify configuration and click Finish



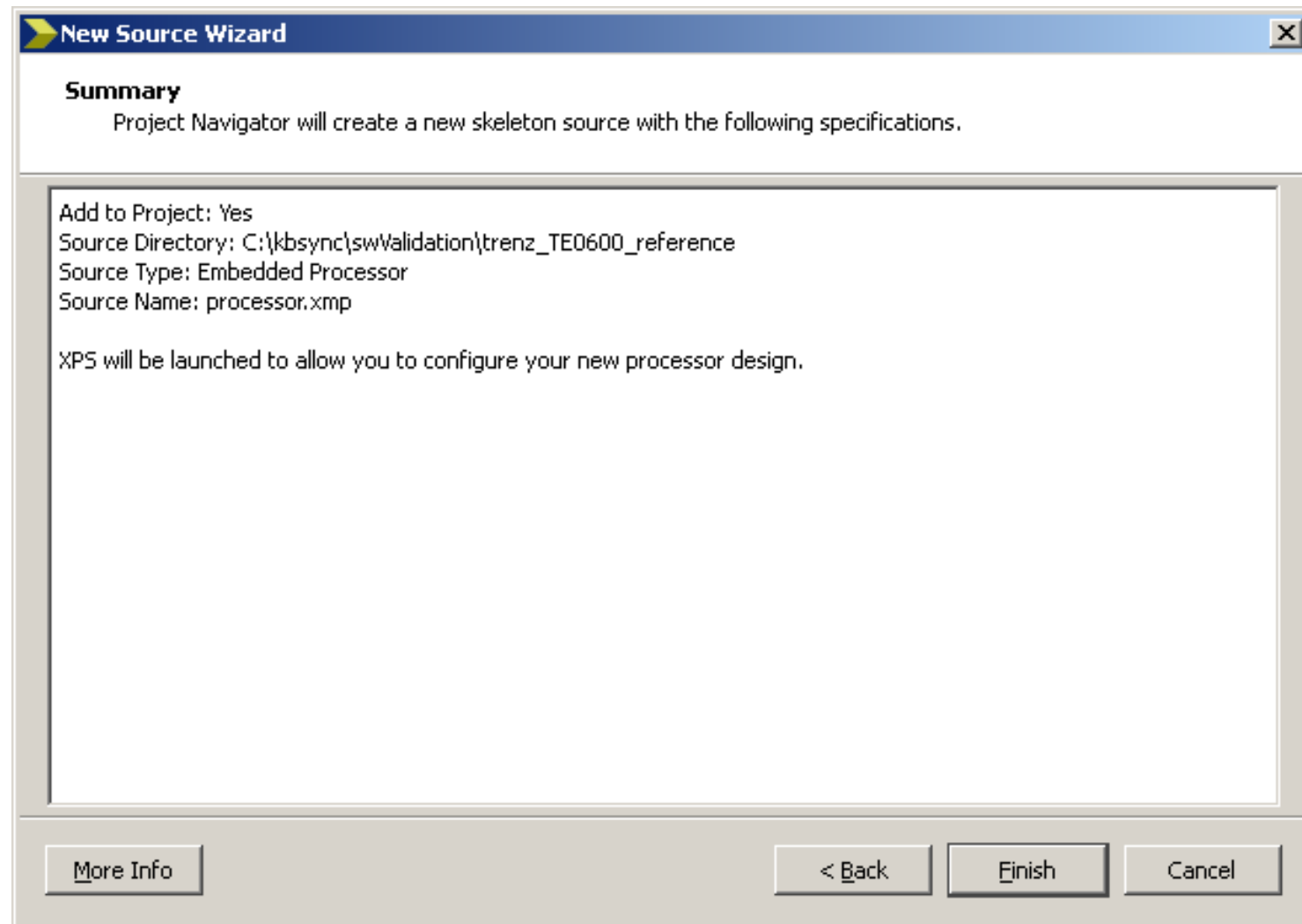
right button menu to add New Source



choose Embedded Processor, provide File name
then click Next



verify configuration then click Finish



Double click on processor.xmp

processor Project Status

Project File:	trenz_TE0600_reference.xise	Parser Errors:	No Errors
Module Name:	processor	Implementation State:	New
Target Device:	xc6slx45-2fgg484	• Errors:	
Product Version:	ISE 14.2	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:		• Final Timing Score:	

XPS Reports

Report Name	Generated	Errors	Warnings	Infos
Platgen Log File				
Simgen Log File				
BitInit Log File				
System Log File	Fri Aug 31 13:19:20 2012			

Design Properties

- ☐ Enable Message Filtering
- ☐ Optional Design Summary Contents
- ☐ Show Clock Report
- ☐ Show Failing Constraints
- ☐ Show Warnings
- ☐ Show Errors

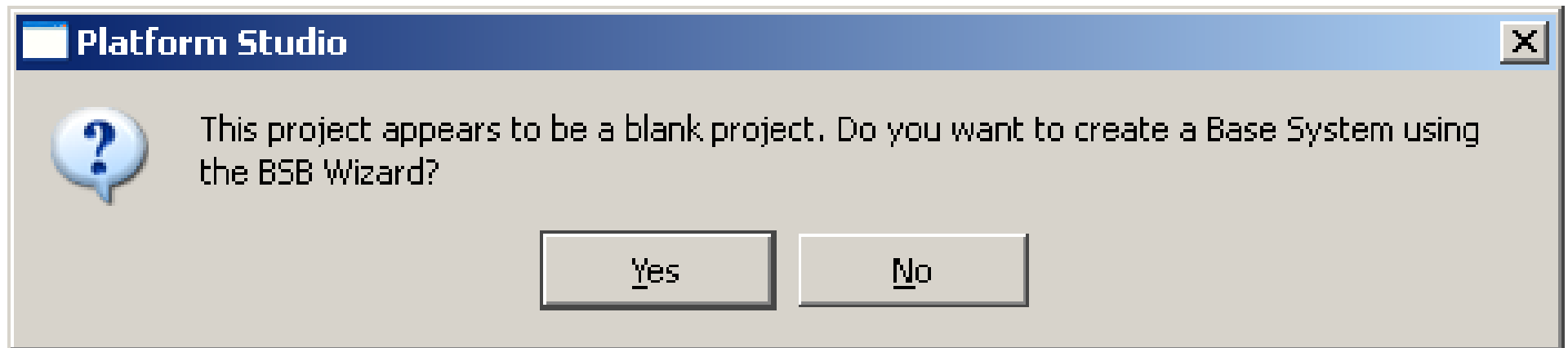
Console

```
Launching XPS GUI...

Process "XPS Process: Create XPS Source" completed successfully
Launching Design Summary/Report Viewer...

INFO: XMP source processor.xmp may not be referenced by your design.
To implement this design either include the instantiation template in your top level design
or run the Generate Top HDL Source process, which will automatically create a top level HDL
which references this design. Use of Generate Top HDL Source is recommended if you want to
implement or analyze your processor design without any additional logic.
```

confirm Yes to launch BSB Wizard



choose PLB system

Create New XPS Project Using BSB Wizard

New Project:

Project File:

Select an Interconnect Type:

☒ AXI System

AXI is an interface standard recently adopted by Xilinx as the standard interface used for all current and future versions of Xilinx IP and tool flows. Details on AXI can be found in the AXI Reference Guide on xilinx.com.

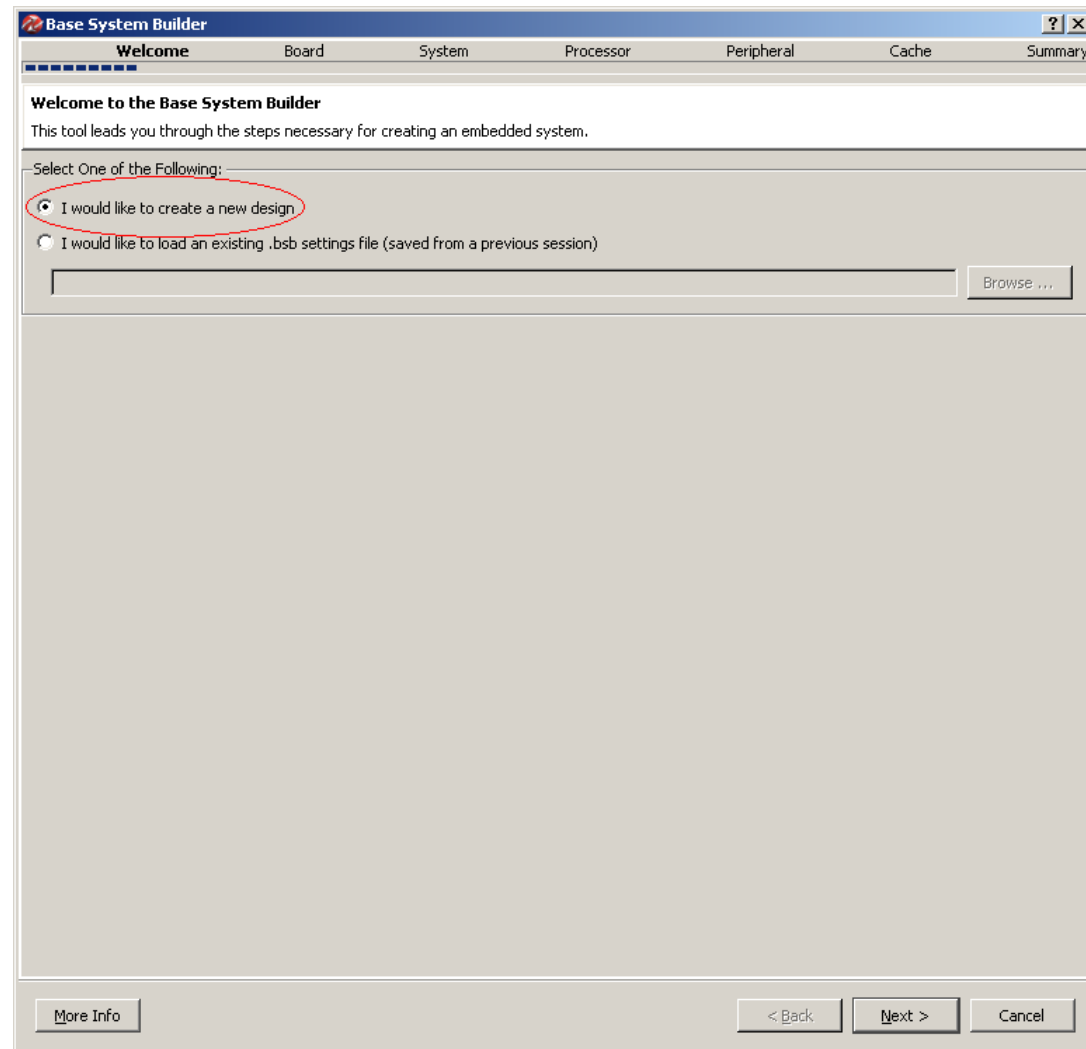
☒ PLB System

PLB is the legacy bus standard used by Xilinx that supports current FPGA families, including Spartan6 and Virtex6. PLB IP will not support newer FPGA families, so is not recommend for new designs that may migrate to future FPGA families. Details on PLB can be found in the PLBv46 Interface Simplifications document on xilinx.com.

Select Existing .bsb Settings File(saved from previous session):

Set Project Peripheral Repository Search Path:

choose create new design then click Next



choose correct Vendor, Name and Revision then
click Next

Base System Builder

Welcome **Board** System Processor Peripheral Cache Summary

Board Selection
Select a target development board.

Board

☒ I would like to create a system for the following development board

Board Vendor: Trenz

Board Name: Spartan-6 LX FPGA micromodule LX45 with carrier board

Board Revision: 1

☐ I would like to create a system for a custom board

Board Information

Architecture: spartan6 Device: xc6slx45 Package: fgg484 Speed Grade: -2

☐ Use Stepping

Reset Polarity: Active High

Related Information

[Vendor's Website](#)

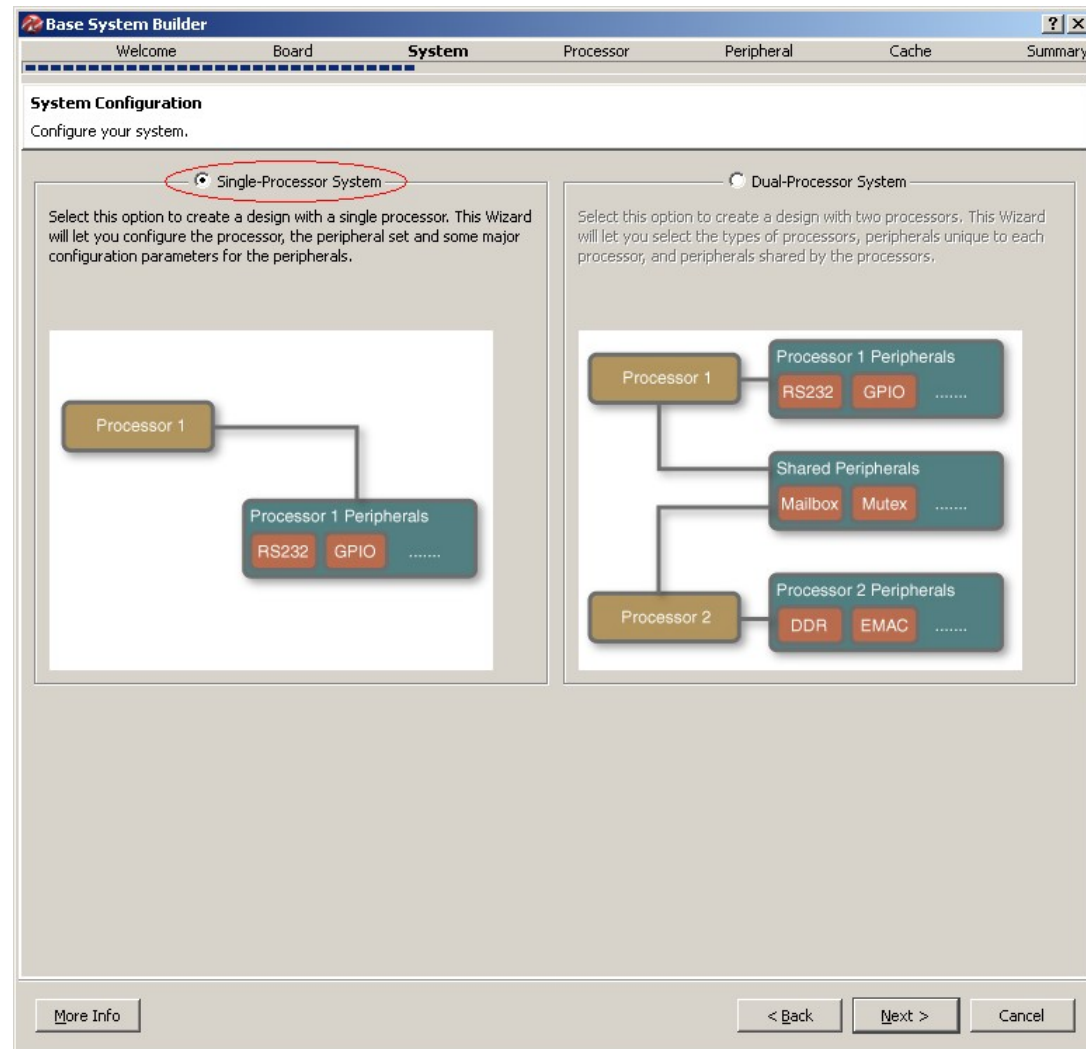
[Vendor's Contact Information](#)

[Third Party Board Definition Files Download Website](#)

Trenz Electronic GigaBee XC6SLX series are industrial-grade FPGA micromodules integrating a leading-edge Xilinx Spartan-6 LX FPGA, gigabit Ethernet transceiver (physical layer), two independent banks of 16-bit-wide 128 MByte DDR3 SDRAM, 8 Mbyte SPI Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors. Placed on TE0603 carrier board.

More Info < Back Next > Cancel

choose Single-Processor System then click Next



choose default Processor Type, System Clock Frequency (half of the reference) and Local Memory size (32 Kb)
then click Next

Base System Builder

Welcome Board System **Processor** Peripheral Cache Summary

Processor Configuration
Configure the processor(s).

Reference Clock Frequency 125.00 MHz

Processor 1 Configuration

Processor Type MicroBlaze

System Clock Frequency 62.50 MHz

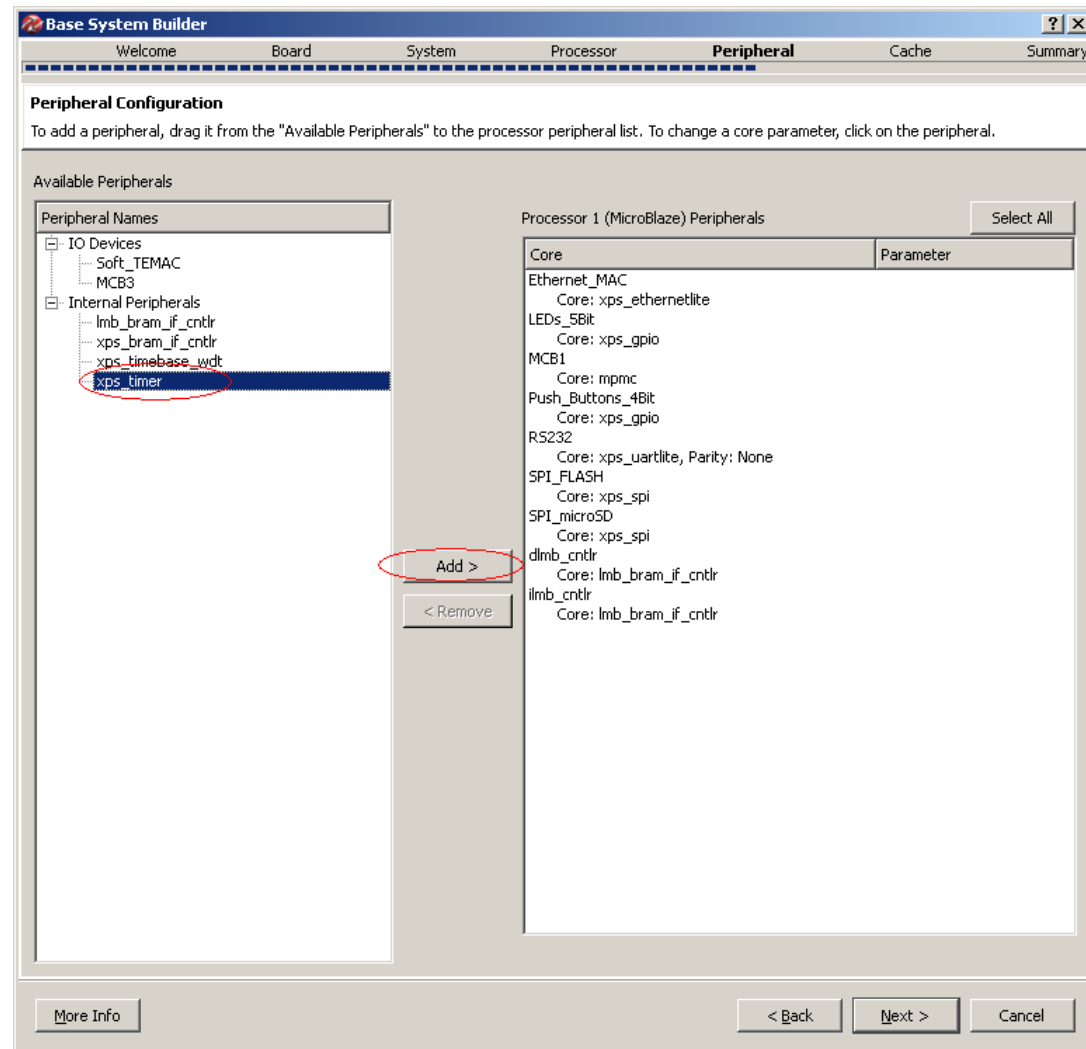
Local Memory 32 KB

Debug Interface On-Chip HW Debug Module

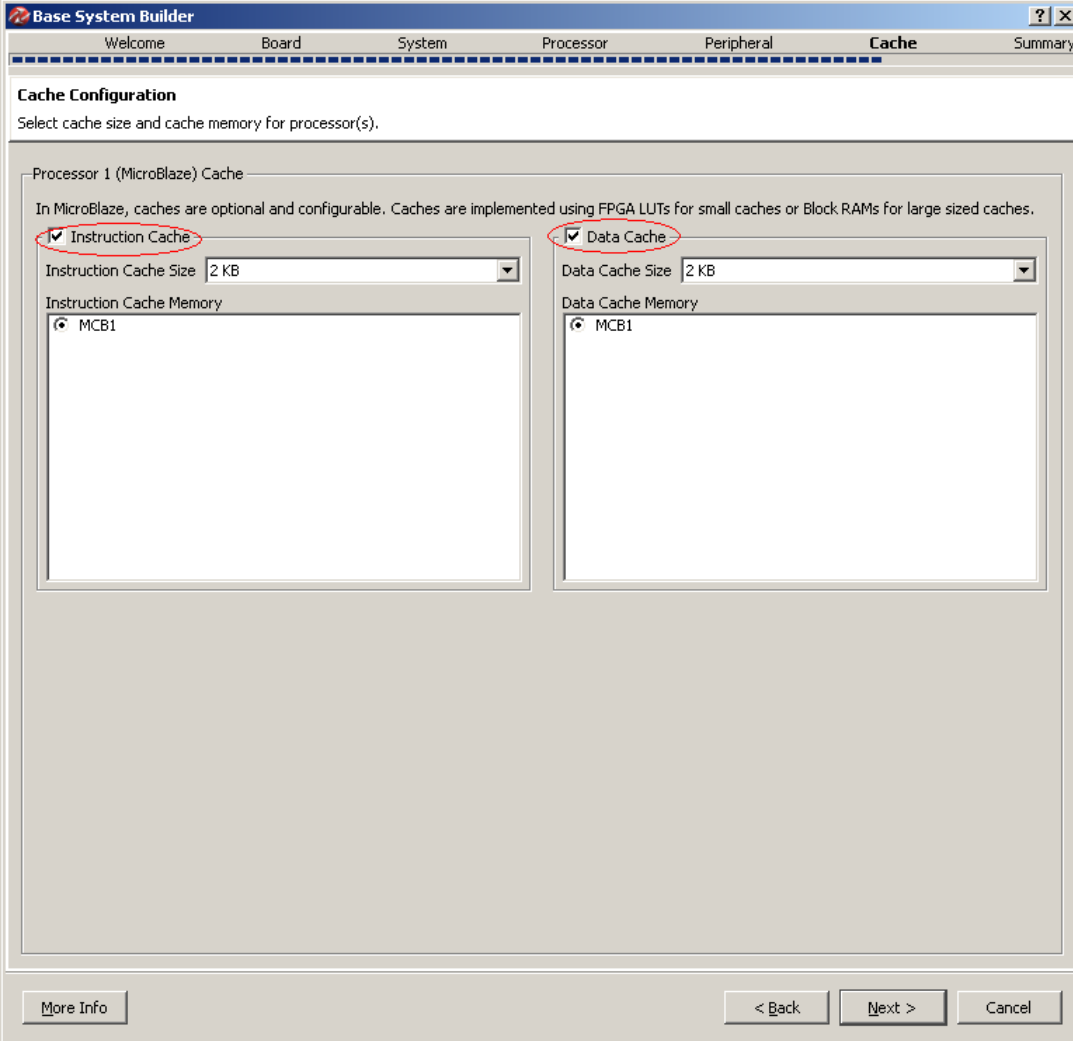
☐ Enable Floating Point Unit

More Info < Back Next > Cancel

add xps_timer (XilKernel required), then click Next



enable Instruction and Data Caches then click Next



The image shows the 'Cache Configuration' window in the 'Base System Builder' application. The window has a title bar with the application name and standard window controls. Below the title bar is a tabbed interface with tabs for 'Welcome', 'Board', 'System', 'Processor', 'Peripheral', 'Cache', and 'Summary'. The 'Cache' tab is currently selected. The main content area is titled 'Cache Configuration' and contains the instruction: 'Select cache size and cache memory for processor(s)'. Below this, there is a section for 'Processor 1 (MicroBlaze) Cache'. A note states: 'In MicroBlaze, caches are optional and configurable. Caches are implemented using FPGA LUTs for small caches or Block RAMs for large sized caches.' There are two columns of configuration options. The left column is for the 'Instruction Cache' and the right column is for the 'Data Cache'. Both columns have a checked checkbox at the top, a 'Cache Size' dropdown menu set to '2 KB', and a 'Cache Memory' list box containing 'MCB1'. At the bottom of the window, there are three buttons: 'More Info', '< Back', and 'Next >', followed by a 'Cancel' button.

Base System Builder

Welcome Board System Processor Peripheral **Cache** Summary

Cache Configuration

Select cache size and cache memory for processor(s).

Processor 1 (MicroBlaze) Cache

In MicroBlaze, caches are optional and configurable. Caches are implemented using FPGA LUTs for small caches or Block RAMs for large sized caches.

☒ Instruction Cache

Instruction Cache Size 2 KB

Instruction Cache Memory

- MCB1

☒ Data Cache

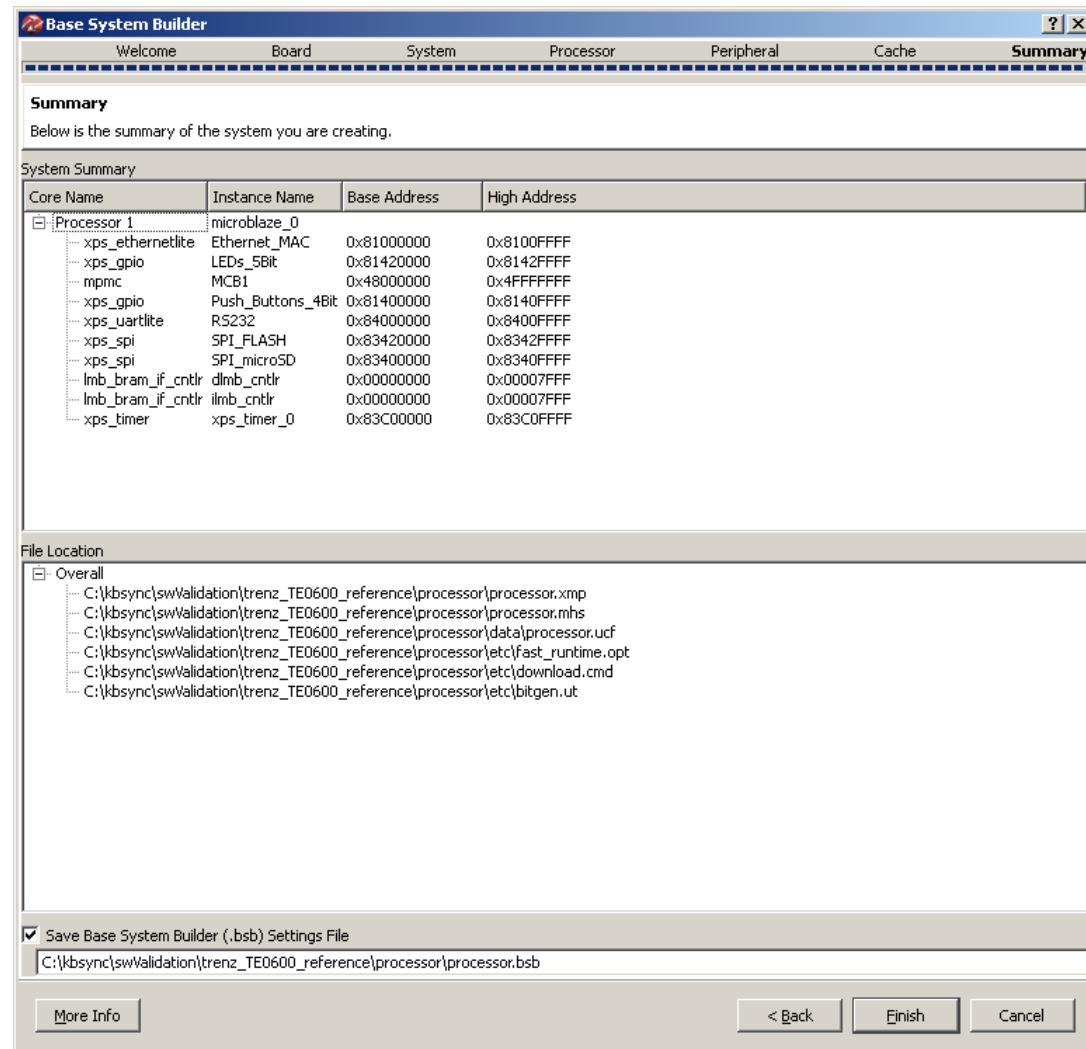
Data Cache Size 2 KB

Data Cache Memory

- MCB1

More Info < Back Next > Cancel

verify created configuration then click Finish



Verify singlewire pcore availability

Xilinx Platform Studio (EDK_P.28xd) - C:\kbsync\swValidation\trenz_TE0600_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Debug Window Help

Project: Platform

- Project Files
 - MHS File: processor.mhs
 - UCF File: C:\kbsync\swValidation\trenz_TE0600_reference\proces
 - Elf Files
- Project Options
 - Device: xc6slx45fgg484-2
 - Netlist: SubModule
 - Implementation: Project Navigator
 - HDL: vhdl
- Design Summary

Bus Interfaces

Name	Bus Name	IP Type	IP Version
dlmb		★ lmb_v10	2.00.b
ilmb		★ lmb_v10	2.00.b
mb_plb		★ plb_v46	1.05.a
microblaze_0		★ microblaze	8.40.a
lmb_bram		★ bram_block	1.00.a
dlmb_cntlr		★ lmb_bram_if...	3.10.a
ilmb_cntlr		★ lmb_bram_if...	3.10.a
MCB1		★ mpmc	6.06.a
mdm_0		★ mdm	2.10.a
xps_intc_0		★ xps_intc	2.01.a
plb_singlewire_0		★ plb_onewire	1.00.a
Ethernet_MAC		★ xps_etherne...	4.00.a
LEDs_5Bit		★ xps_gpio	2.00.a
Push_Buttons_4Bit		★ xps_gpio	2.00.a
SPI_FLASH		★ xps_spi	2.02.a
SPI_microSD		★ xps_spi	2.02.a
xps_timer_0		★ xps_timer	1.02.a
RS232		★ xps_uartlite	1.02.a
clock_generator_0		★ clock_gener...	4.03.a
proc_sys_reset_0		★ proc_sys_re...	3.00.a

Legend

- Master (blue circle), Slave (green circle), Master/Slave (yellow circle), Target (red circle), Initiator (purple circle)
- Connected (blue circle), Unconnected (green circle), Monitor (green circle)
- Production (green star), License (paid) (yellow star), License (eval) (blue star), Local (blue star), Pre Production (blue star), Beta (blue star), Development (blue star)
- Superseded (yellow triangle), Discontinued (yellow circle)

Console

```
(0x84000000-0x8400ffff) RS232 mb_plb
(0x84400000-0x8440ffff) mdm_0 mb_plb
(0xc2600000-0xc260ffff) plb_singlewire_0 mb_plb
```

launch Project Options

Xilinx Platform Studio (EDK P.28xd) - C:\kbsync\swValidation\trenz_TE0600_reference\processor\processor.xmp - [System Assembly View]

Project Options...

- Design Rule Check Ctrl+Shift+D
- Export Hardware Design to SDK...
- Archive Project...
- Generate Block Diagram Image (Obsolete)
- Open Graphical Design View
- Generate and View Design Report
- View Design Summary
- Run Version Migration
- Rescan User Repositories
- Launch Xilinx Shell
- Customize Buttons...
- Clean All Generated Files
- Terminate Running Process

Bus Interfaces

Name	Bus Name	IP Type	IP Version
dmb		lmb_v10	2.00.b
ilmb		lmb_v10	2.00.b
mb_plb		plb_v46	1.05.a
microblaze_0		microblaze	8.40.a
lmb_bram		bram_block	1.00.a
dmb_cntlr		lmb_bram_if...	3.10.a
ilmb_cntlr		lmb_bram_if...	3.10.a
MCB1		mpmc	6.06.a
mdm_0		mdm	2.10.a
xps_intc_0		xps_intc	2.01.a
Ethernet_MAC		xps_etherne...	4.00.a
LEDs_5Bit		xps_gpio	2.00.a
Push_Buttons_4Bit		xps_gpio	2.00.a
SPI_FLASH		xps_spi	2.02.a
SPI_microSD		xps_spi	2.02.a
xps_timer_0		xps_timer	1.02.a
RS232		xps_uartlite	1.02.a
clock_generator_0		clock_gener...	4.03.a
proc_sys_reset_0		proc_sys_re...	3.00.a

Legend

- Master (blue circle)
- Slave (green circle)
- Master/Slave (yellow circle)
- Target (red circle)
- Initiator (blue circle)
- Connected (blue circle)
- Unconnected (green circle)
- Monitor (green circle)
- Production (green star)
- License (paid) (yellow star)
- License (eval) (orange star)
- Local (blue star)
- Pre Production (blue star)
- Beta (blue star)
- Development (blue star)
- Superseded (yellow triangle)
- Discontinued (yellow circle)

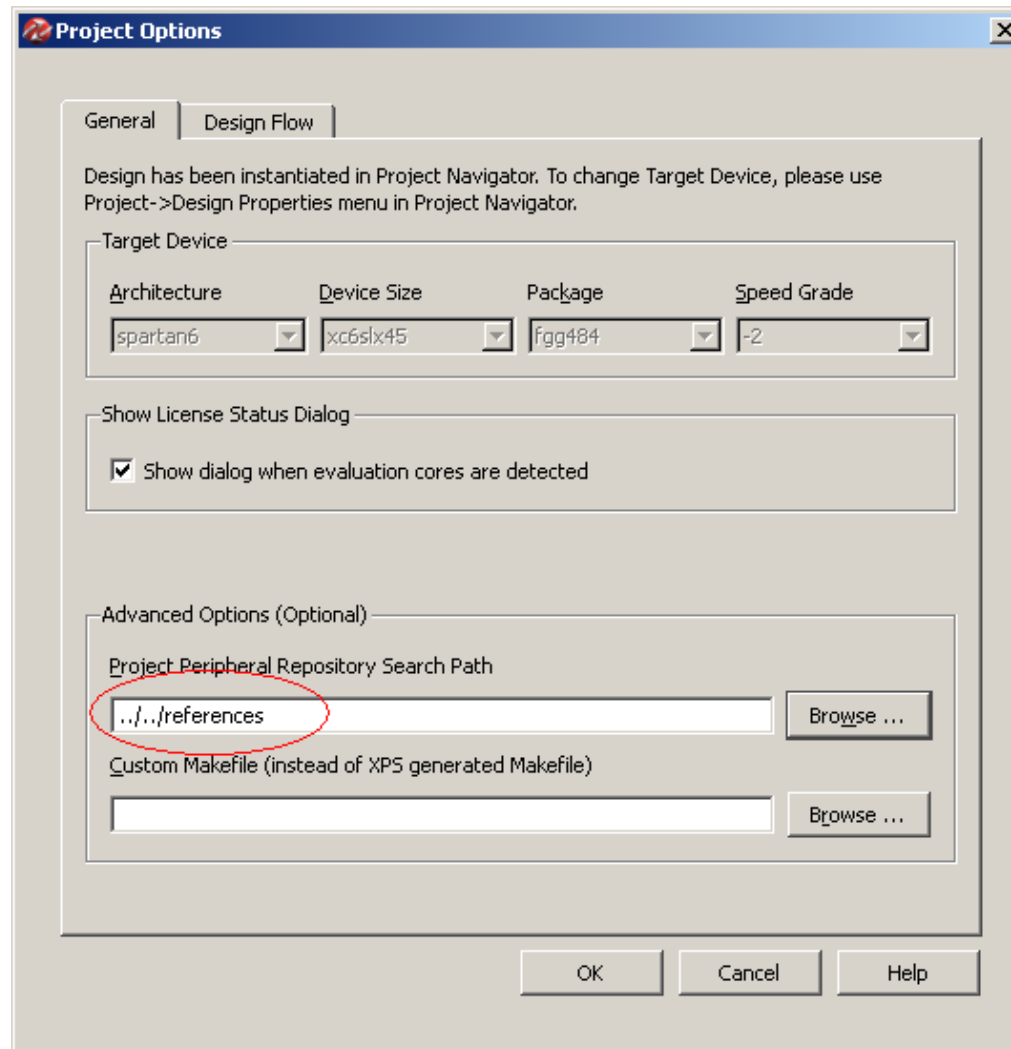
Console

```

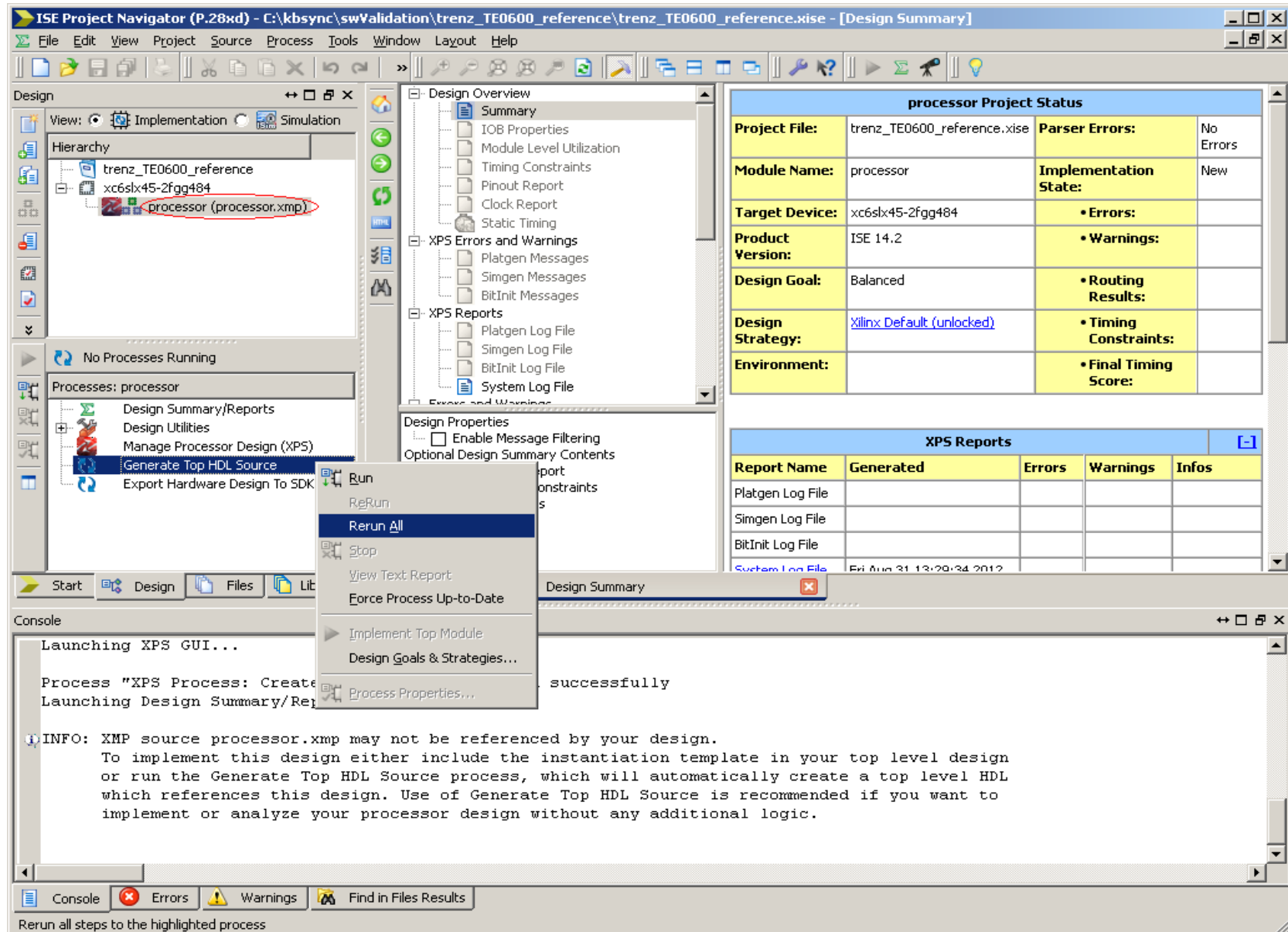
(0x83c00000-0x83c0ffff) xps_timer_0 mb_plb
(0x84000000-0x8400ffff) RS232 mb_plb
(0x84400000-0x8440ffff) mdm_0 mb_plb
  
```

Configure Project Specific Options

provide path to the private pcores (singlewire)
then click OK



return to ISE Project Navigator, step on
cessor.xmp and generate TOP HDL Source



step on processor.xmp, choose Generate Programming File and click Rerun All

ISE Project Navigator (P.28xd) - C:\kbsync\swValidation\trenz_TE0600_reference\trenz_TE0600_reference.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
 - IOB Properties
 - Module Level Utilization
 - Timing Constraints
 - Pinout Report
 - Clock Report
 - Static Timing
- XPS Errors and Warnings
 - Platgen Messages
 - Simgen Messages
 - BitInit Messages
- XPS Reports
 - Platgen Log File
 - Simgen Log File
 - BitInit Log File
 - System Log File

Design Properties

- ☐ Enable Message Filtering
- ☐ Optional Design Summary Contents
- ☐ Show Clock Report
- ☐ Show Failing Constraints

processor Project Status

Project File:	trenz_TE0600_reference.xise	Parser Errors:	No Errors
Module Name:	processor_top	Implementation State:	New
Target Device:	xc6slx45-2fgg484	• Errors:	
Product Version:	ISE 14.2	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:		• Final Timing Score:	

XPS Reports

Report Name	Generated	Errors	Warnings	Infos
Platgen Log File				
Simgen Log File				
BitInit Log File				
System Log File				

Processes: processor_top - STRUCTURE

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

Run

- ReRun
- Rerun All
- Stop
- View Text Report
- Force Process Up-to-Date
- Implement Top Module
- Design Goals & Strategies...
- Process Properties...

Console

```
Inserting wrapper level ...
Writing (stub) BMM ...
Writing top-level HDL ...

Total run time: 7.00 seconds
INFO:HDLCompiler:1061 - Parsing VHDL file "C:/kbsync/swValidation/trenz_TE0600_reference/processor/processor_top.vhd" into
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Process "XPS Process: Generate Top HDL Source" completed successfully
```

Rerun all steps to the highlighted process

confirm generation success and return to Xilinx Platform Studio

The screenshot displays the Xilinx ISE Project Navigator interface. The title bar indicates the project is 'trenz_TE0600_reference' and the 'Design Summary (Programming File Generated)' window is active. The left pane shows the project hierarchy with 'processor_top - STRUCTURE' selected. The bottom-left pane shows the 'Processes' list, where 'Generate Programming File' is highlighted. The bottom-right pane shows the console output, which includes the command used to generate the programming file and a confirmation message: 'Process "Generate Programming File" completed successfully'.

processor Project Status (08/31/2012 - 15:17:23)

Project File:	trenz_TE0600_reference.xise	Parser Errors:	No Errors
Module Name:	processor_top	Implementation State:	Programming File Generated
Target Device:	xc6slx45-2fgg484	•Errors:	No Errors
Product Version:	ISE 14.2	•Warnings:	208 Warnings (107 new)
Design Goal:	Balanced	•Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	All Constraints Met
Environment:	System Settings	•Final Timing Score:	0 (Timing Report)

XPS Reports

Report Name	Generated	Errors	Warnings	Infos
Platgen Log File	Fri Aug 31 13:38:56 2012	0	0	69 Infos (2)

Checking platform address map ...

Initializing Memory...

Running Data2Mem with the following command:

```
data2mem -bm "implementation/processor_bd" -p xc6slx45fgg484-2 -bt "implementation/processor.bit" -bd "bootloops/microblaze_0.elf" tag microblaze_0 -o b implementation/download.bit
```

Memory Initialization completed successfully.

Process "Generate Programming File" completed successfully

choose from menu Export Hardware Design to SDK with bitstream

The screenshot shows the Xilinx ISE Project Navigator interface. The 'Design' tab is active, displaying the 'processor_top - STRUCTURE (processor_top.vh)' and 'processor_i - processor (processor.xmp)'. The 'Design Overview' pane on the right lists various reports, including 'XPS Errors and Warnings', 'XPS Reports', and 'Design Properties'. The 'Console' pane at the bottom shows the output of the 'Generate Programming File' process, which completed successfully. A context menu is open over the 'Export Hardware Design to SDK with Bitstream' option in the 'Design Utilities' pane.

processor Project Status (08/31/2012 - 15:17:23)

Project File:	trenz_TE0600_reference.xise	Parser Errors:	No Errors
Module Name:	processor_top	Implementation State:	Programming File Generated
Target Device:	xc6slx45-2fgg484	•Errors:	No Errors
Product Version:	ISE 14.2	•Warnings:	208 Warnings (107 new)
Design Goal:	Balanced	•Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	All Constraints Met
Environment:	System Settings	•Final Timing Score:	0 (Timing Report)

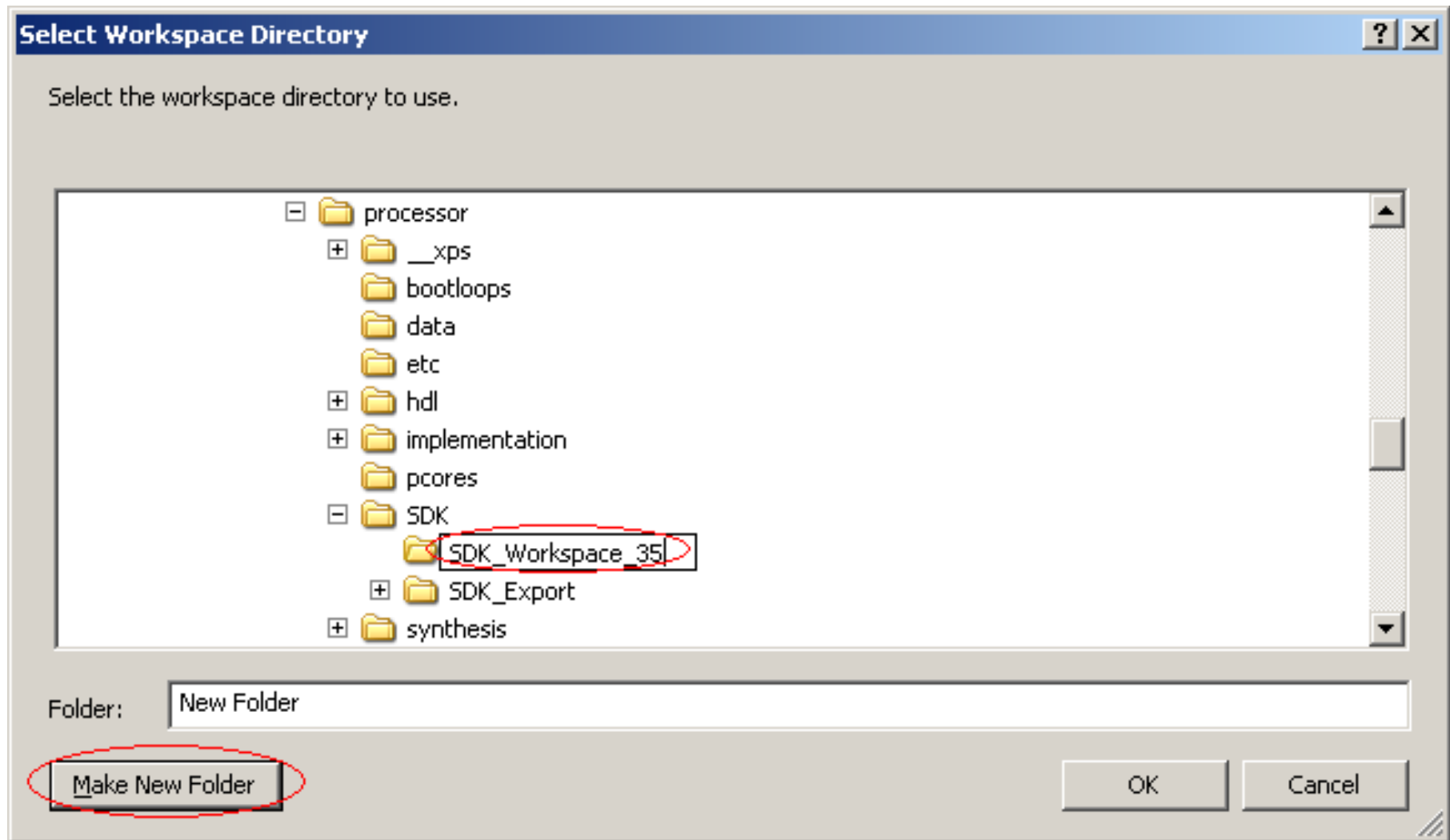
XPS Reports

Report Name	Generated	Errors	Warnings	Infos
Platgen Log File	Fri Aug 31 13:38:56 2012	0	0	69 Infos (2 new)

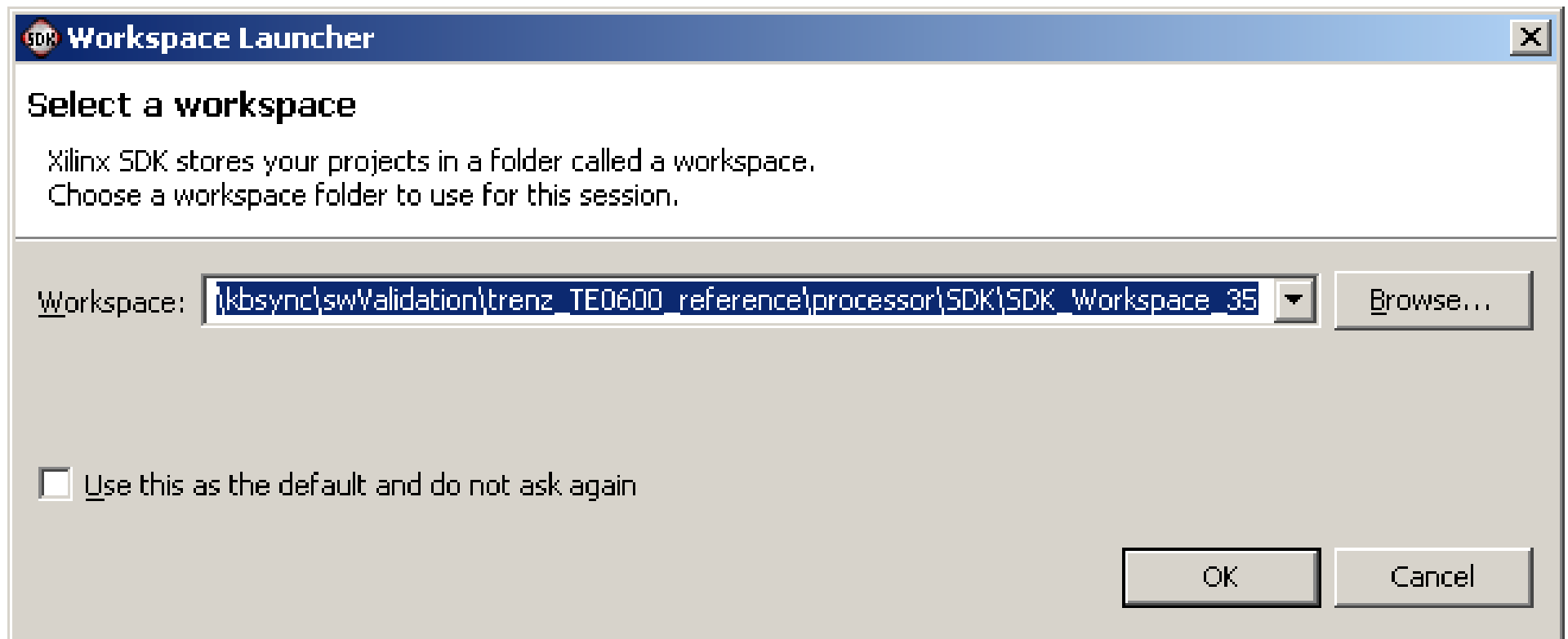
Console

```
Checking platform address map ...  
Initializing Memory...  
Running Data2Mem with the following  
data2mem -bm "implementation/processor_top.vh" -bd "bootloops/microblaze_0.elf" tag  
microblaze_0 -o b implementation/download.bit  
Memory Initialization completed successfully.  
  
Process "Generate Programming File" completed successfully
```

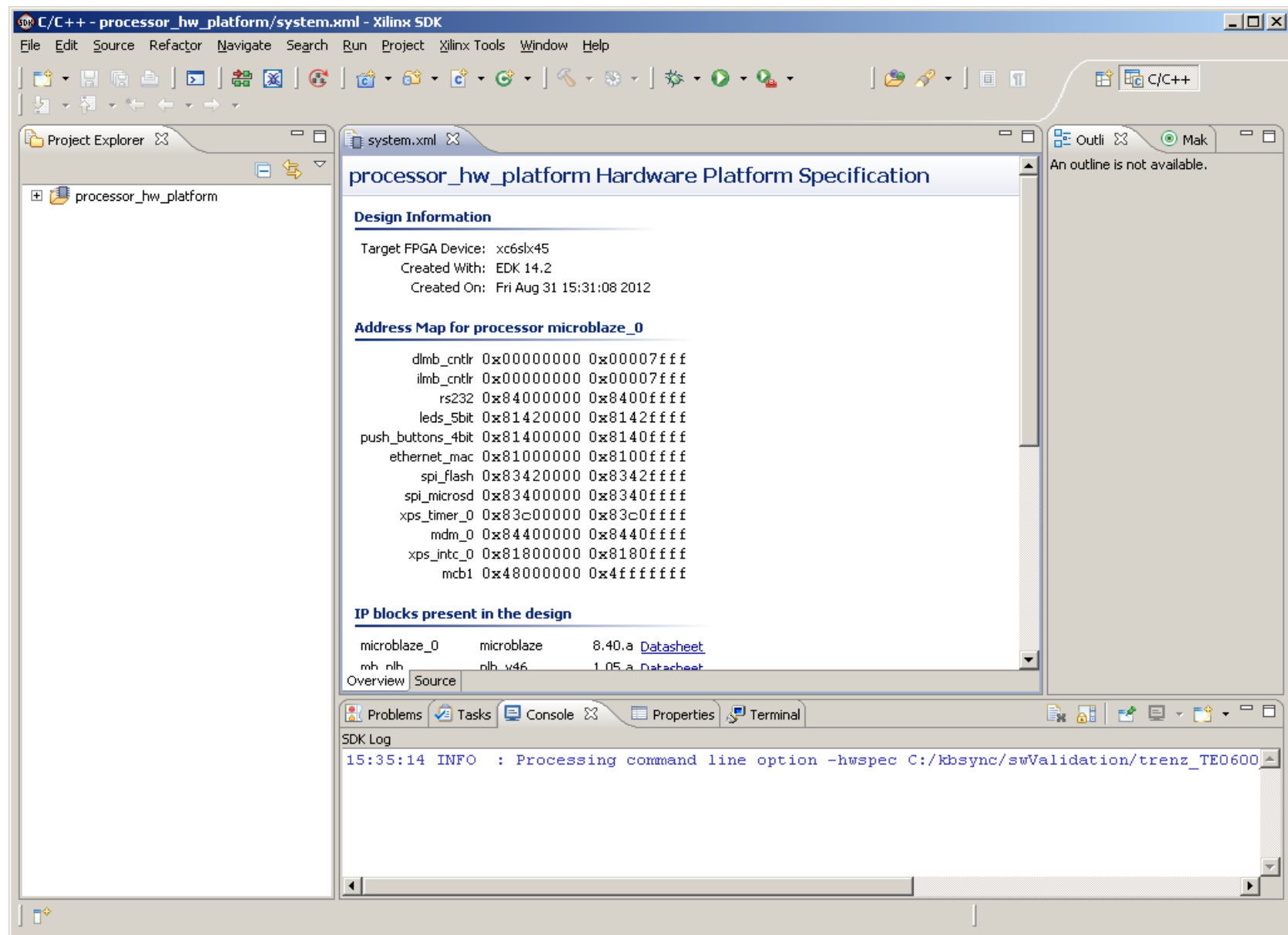
Create workspace working folder



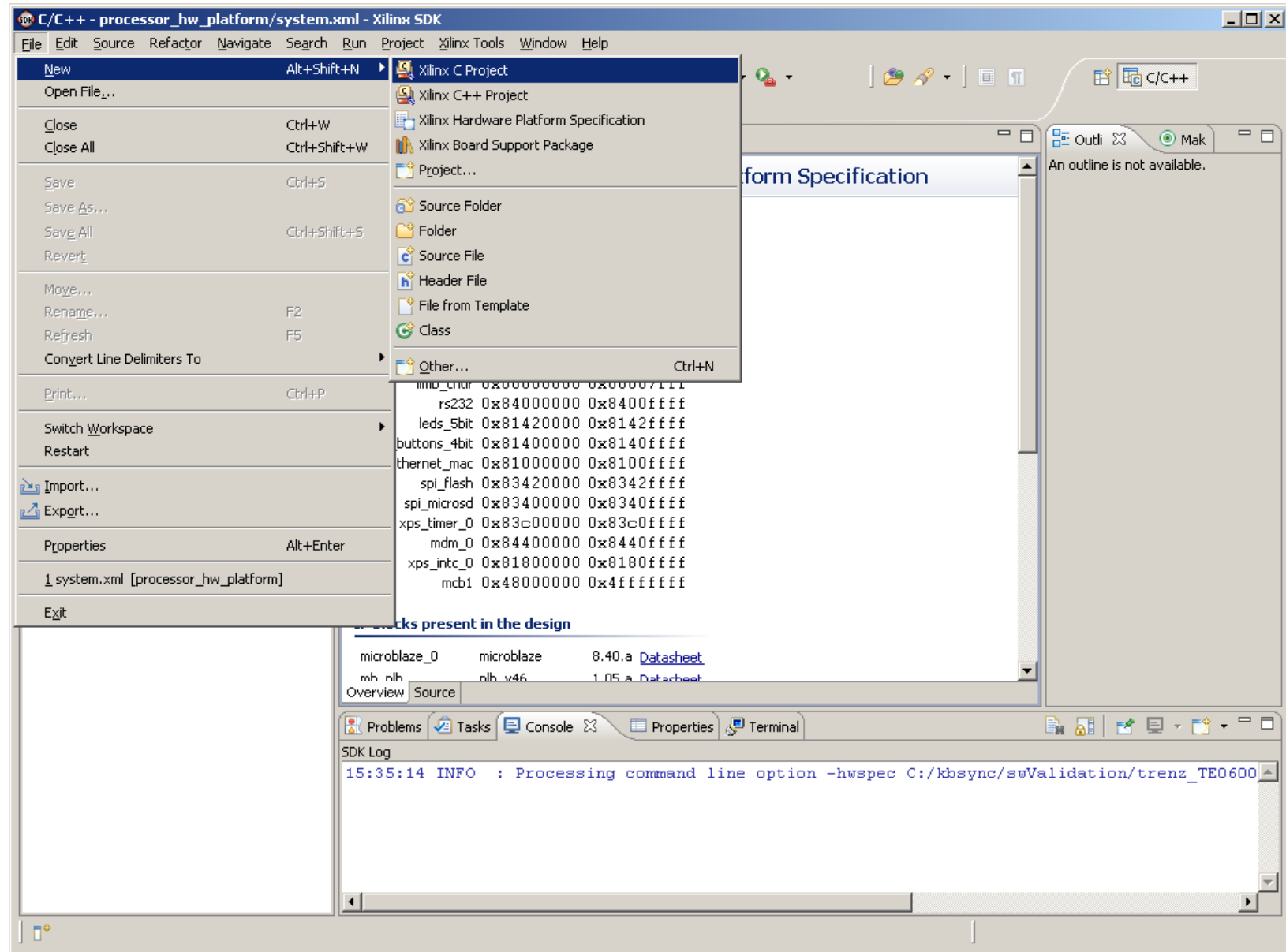
Confirm workspace location



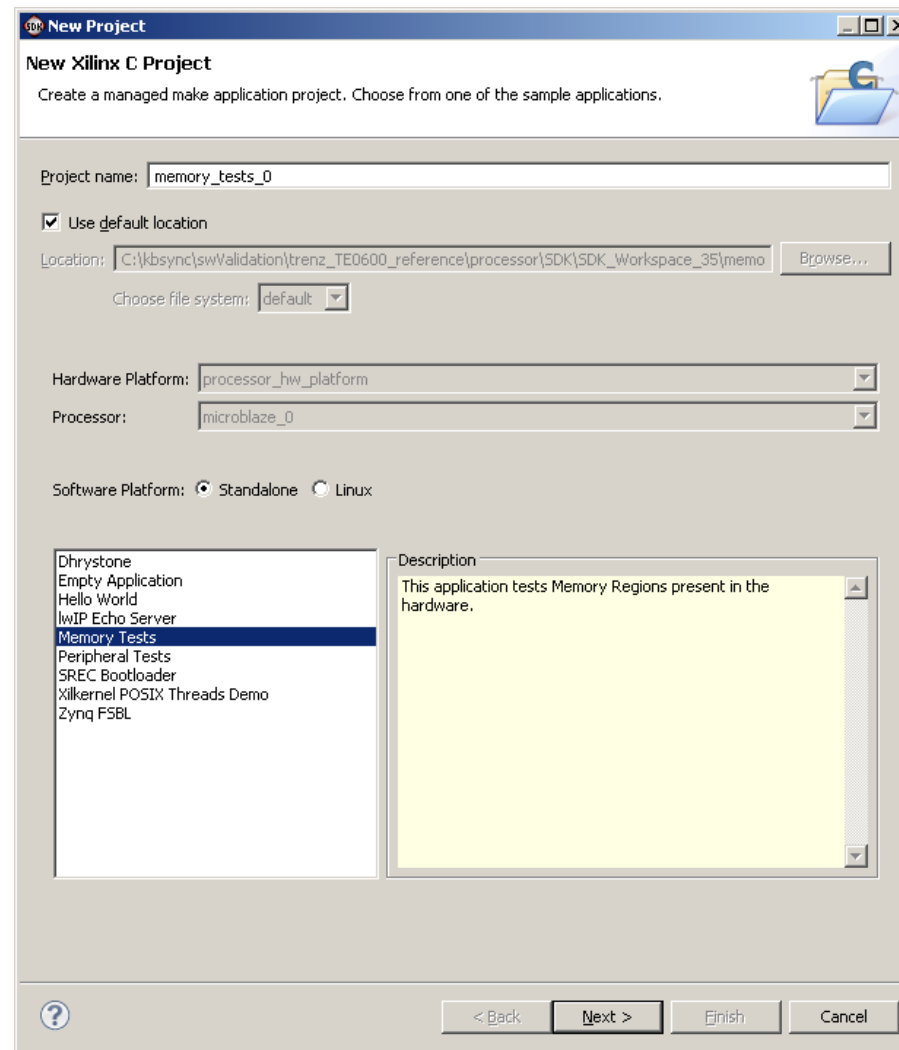
Obtain empty SDK configuration



from SDK menu choose to create New Xilinx C Project



choose Memory Tests template and click Next



New Project

New Xilinx C Project
Create a managed make application project. Choose from one of the sample applications.

Project name:

☒ Use default location

Location:

Choose file system:

Hardware Platform:

Processor:

Software Platform: ☒ Standalone ☐ Linux

	Description
Dhrystone	
Empty Application	
Hello World	
lwIP Echo Server	
Memory Tests	This application tests Memory Regions present in the hardware.
Peripheral Tests	
SREC Bootloader	
Xilkernel POSIX Threads Demo	
Zynq FSBL	

keep default BSP project name
memory_tests_bsp_0 and click Finish

New Project

New Xilinx C Project
Create a managed make application project. Choose from one of the sample applications.

☒ Create a new Board Support Package project

The template provided by application 'Memory Tests' will be used to configure the project.

Project name: memory_tests_bsp_0

☒ Use default location

Location: C:\kbsync\swValidation\trenz_TE0600_reference\processor\SDK\SDK_Workspace_35\men Browse...

Choose file system: default

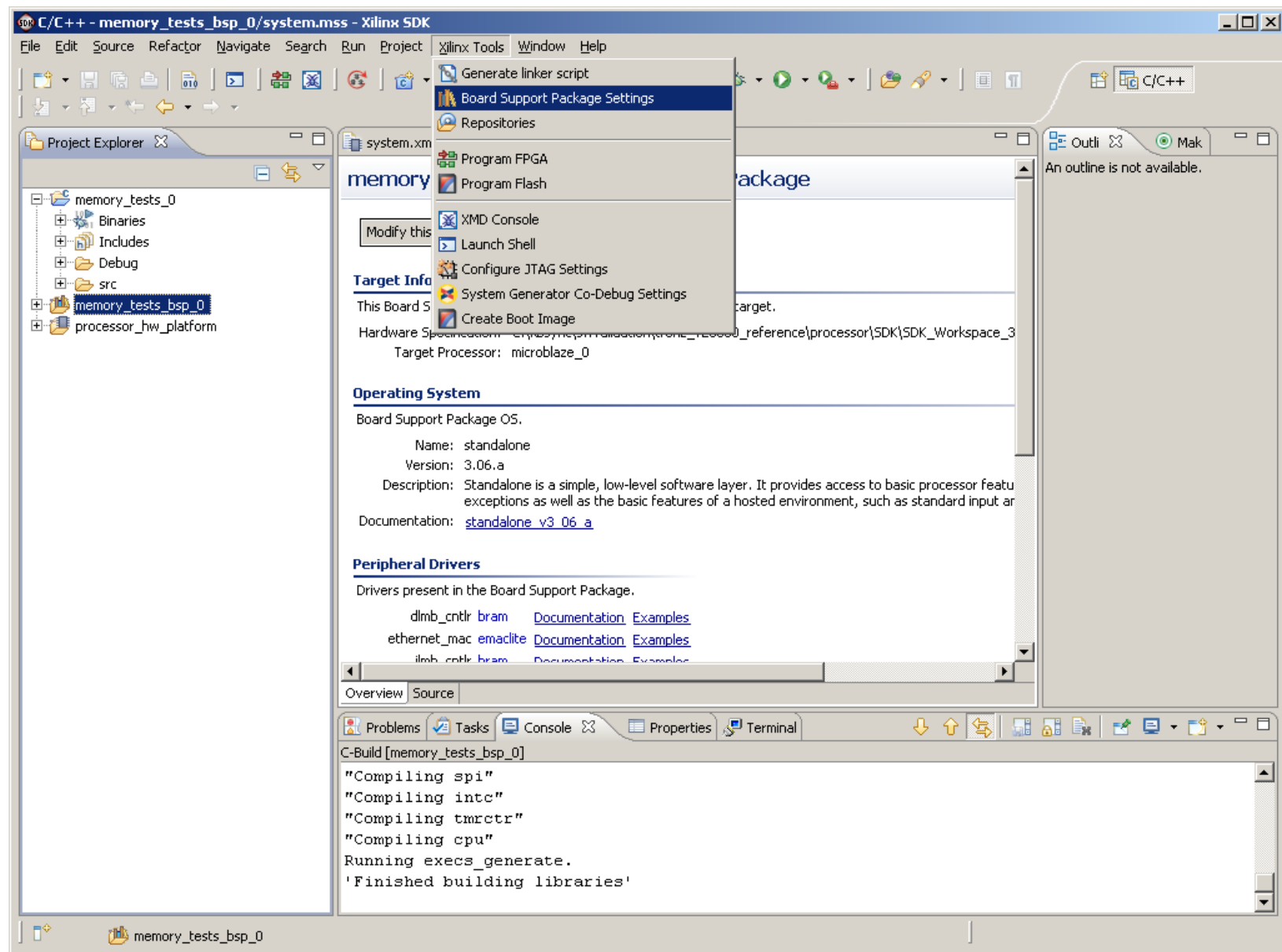
☐ Target an existing Board Support Package

Available Board Support Packages:

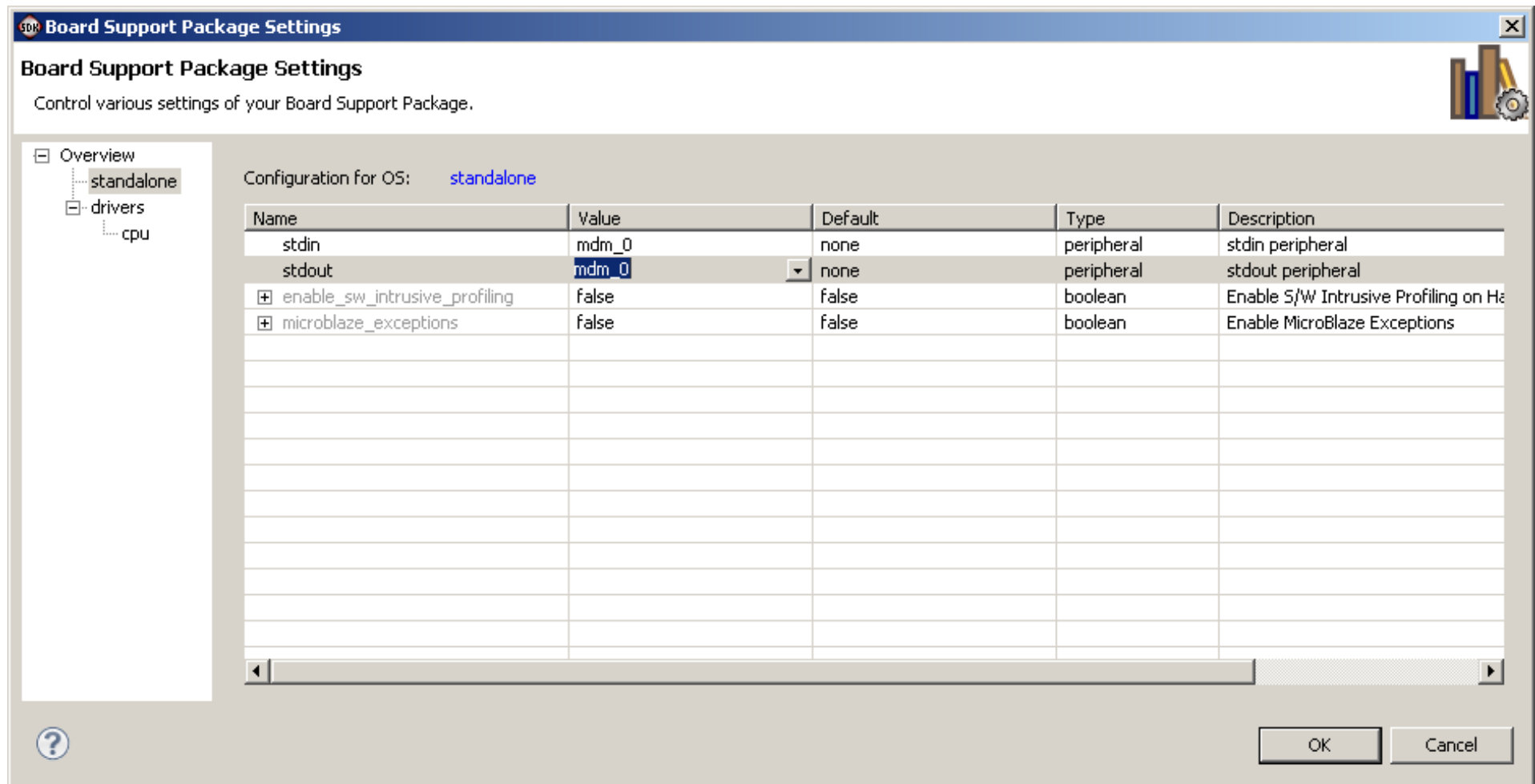
No Board Support Packages found

? < Back Next > Finish Cancel

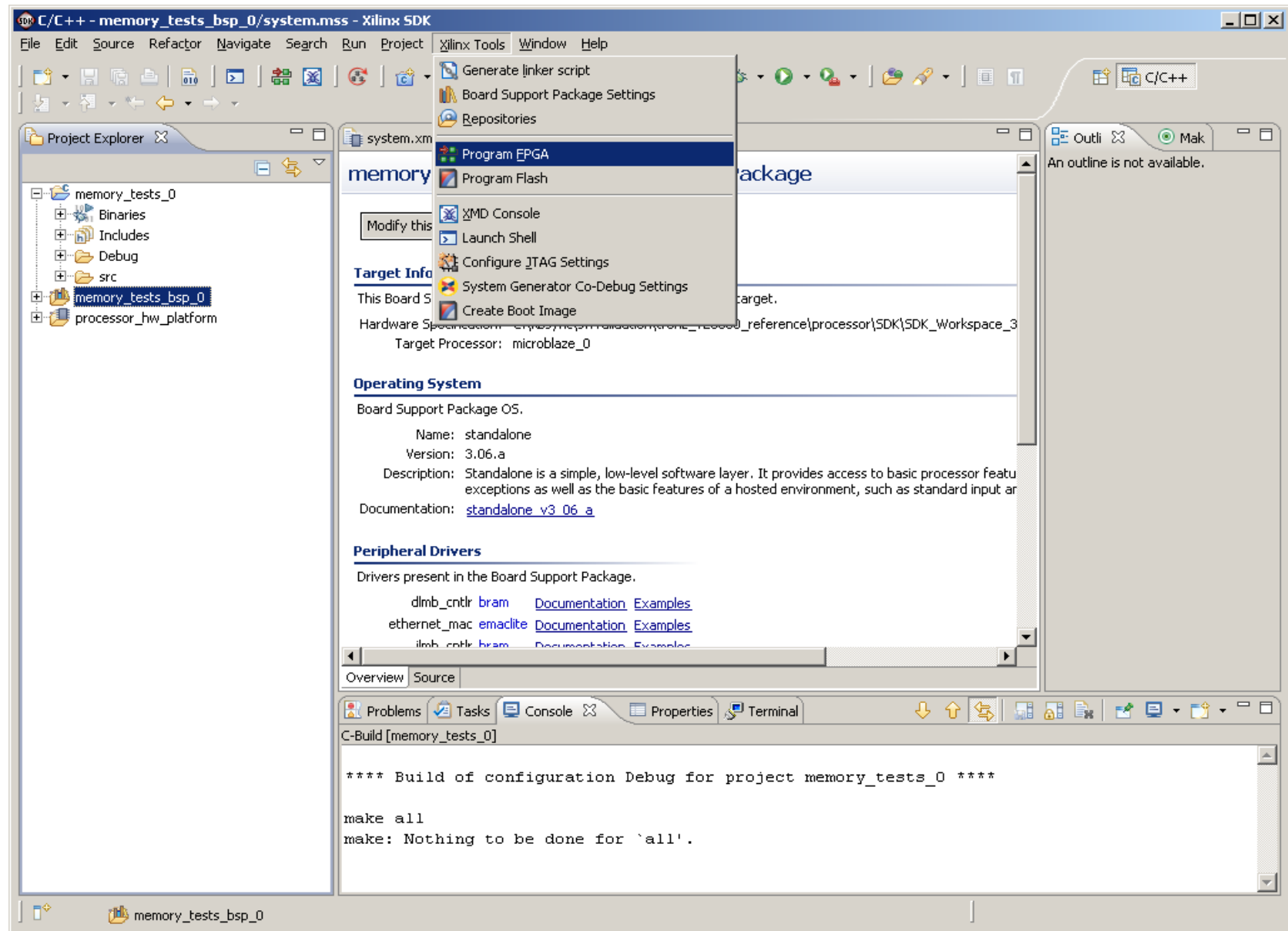
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



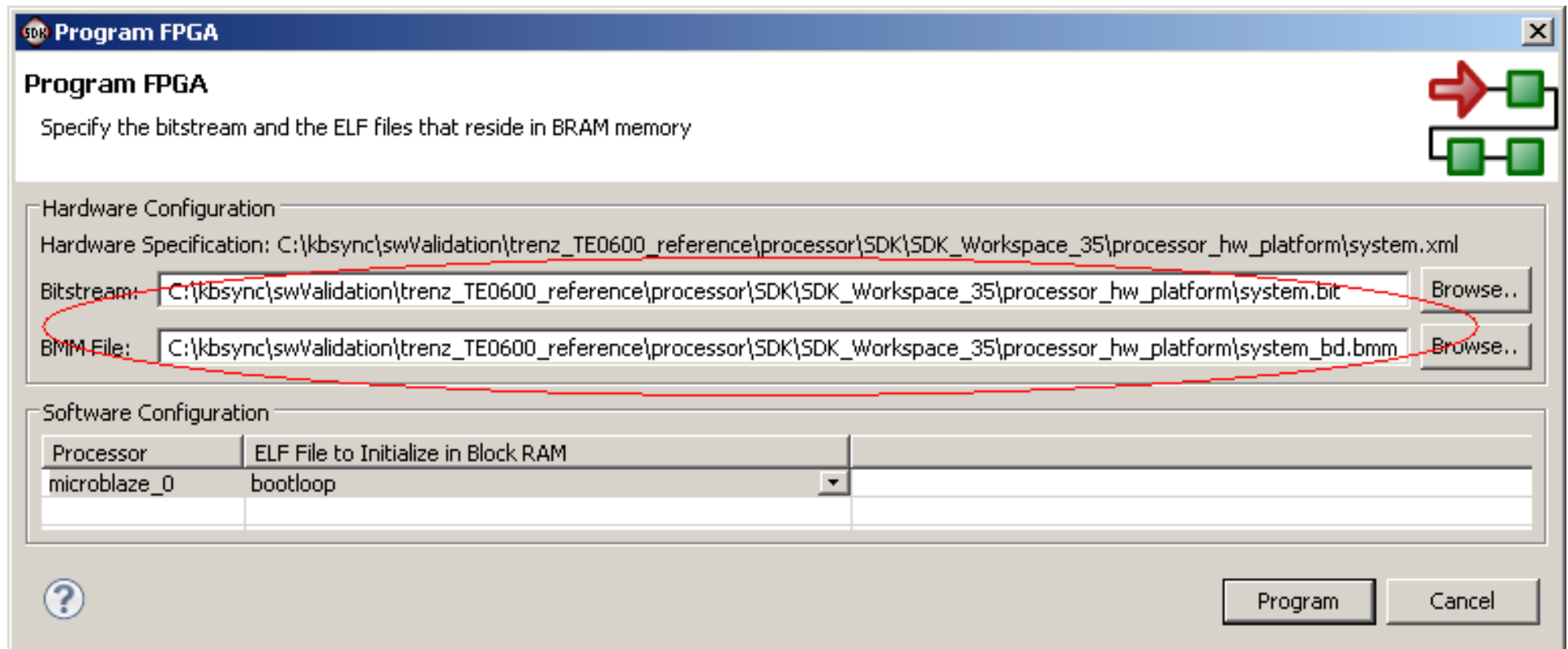
from standalone section apply mdm_0 to stdin
and
stdout then click OK



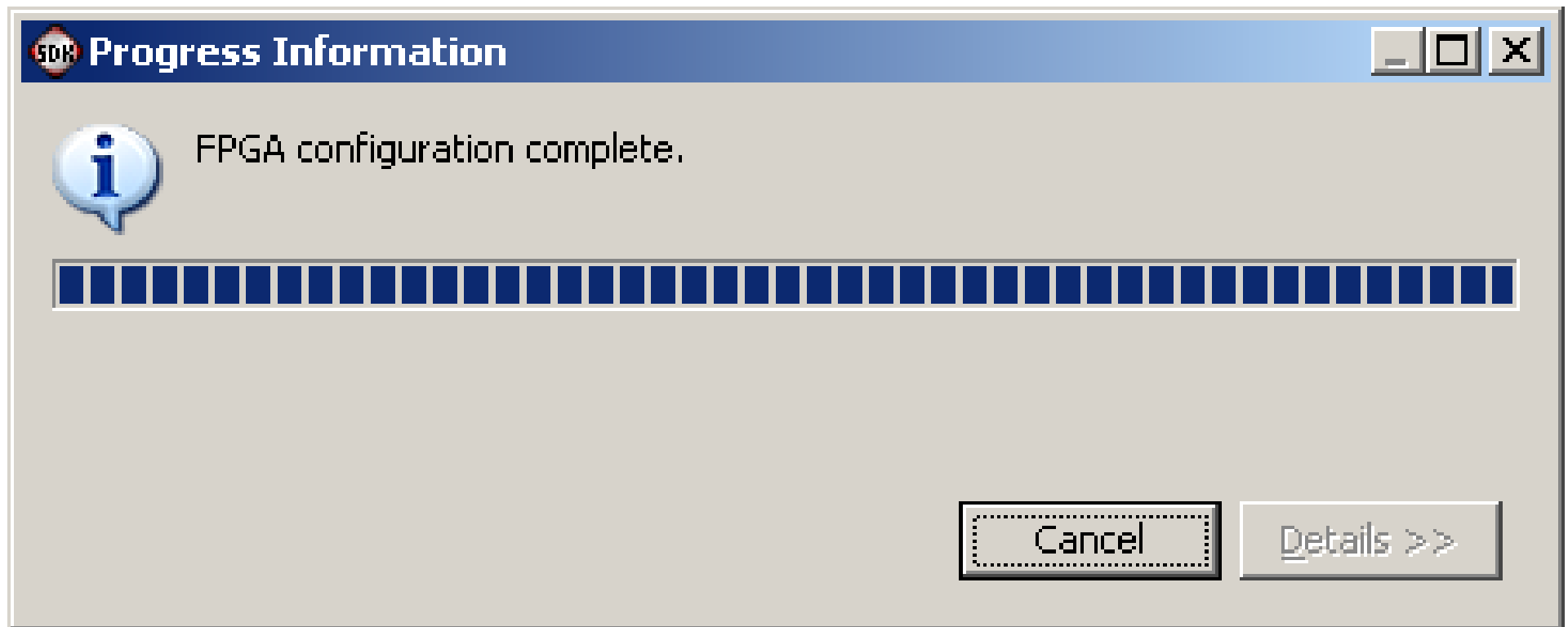
connect the prototype board TE0600 and choose Program FPGA from menu



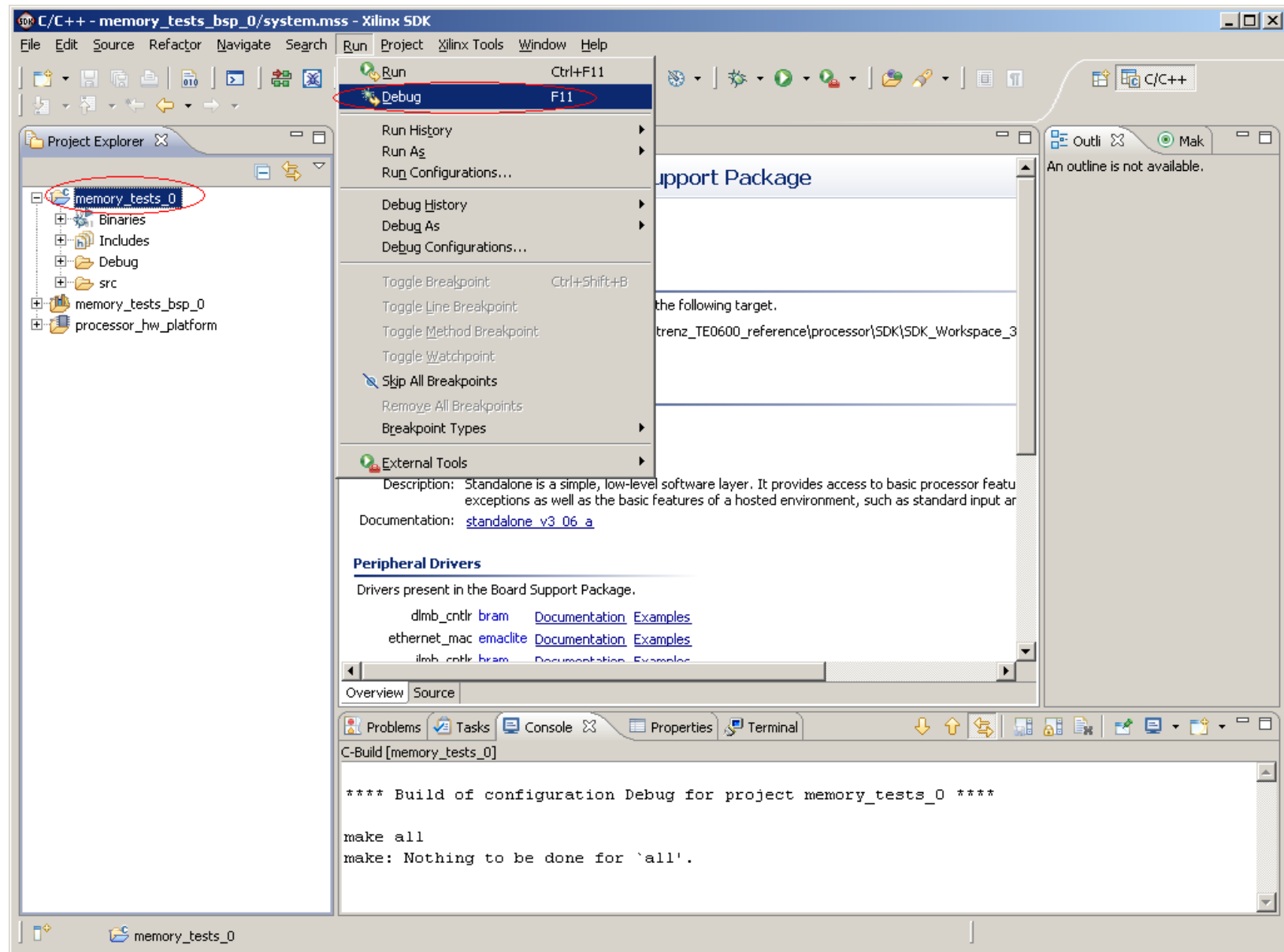
provide correct Bistream and BMM files then click
Program



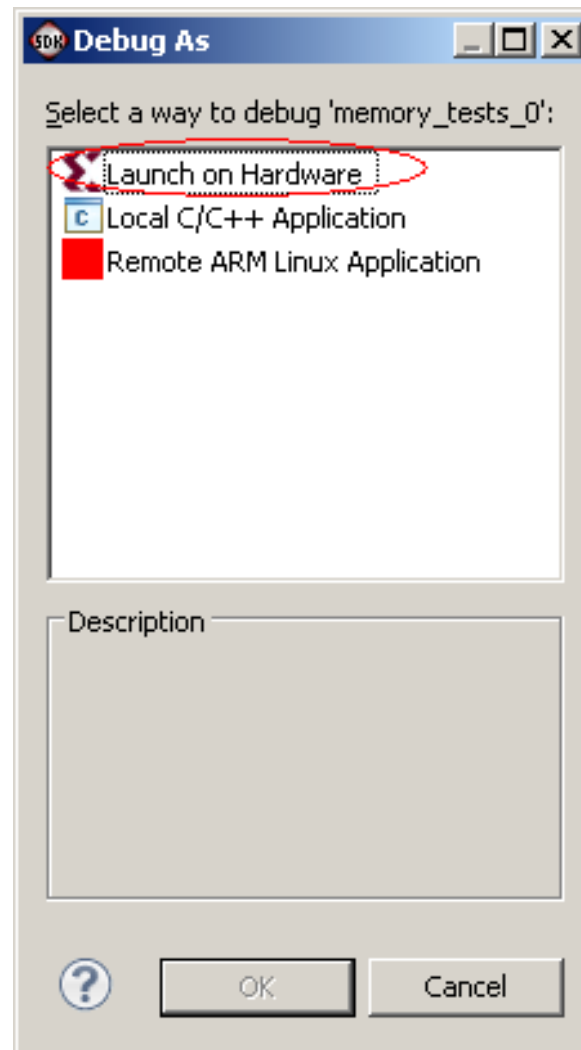
wait for FPGA programming completion



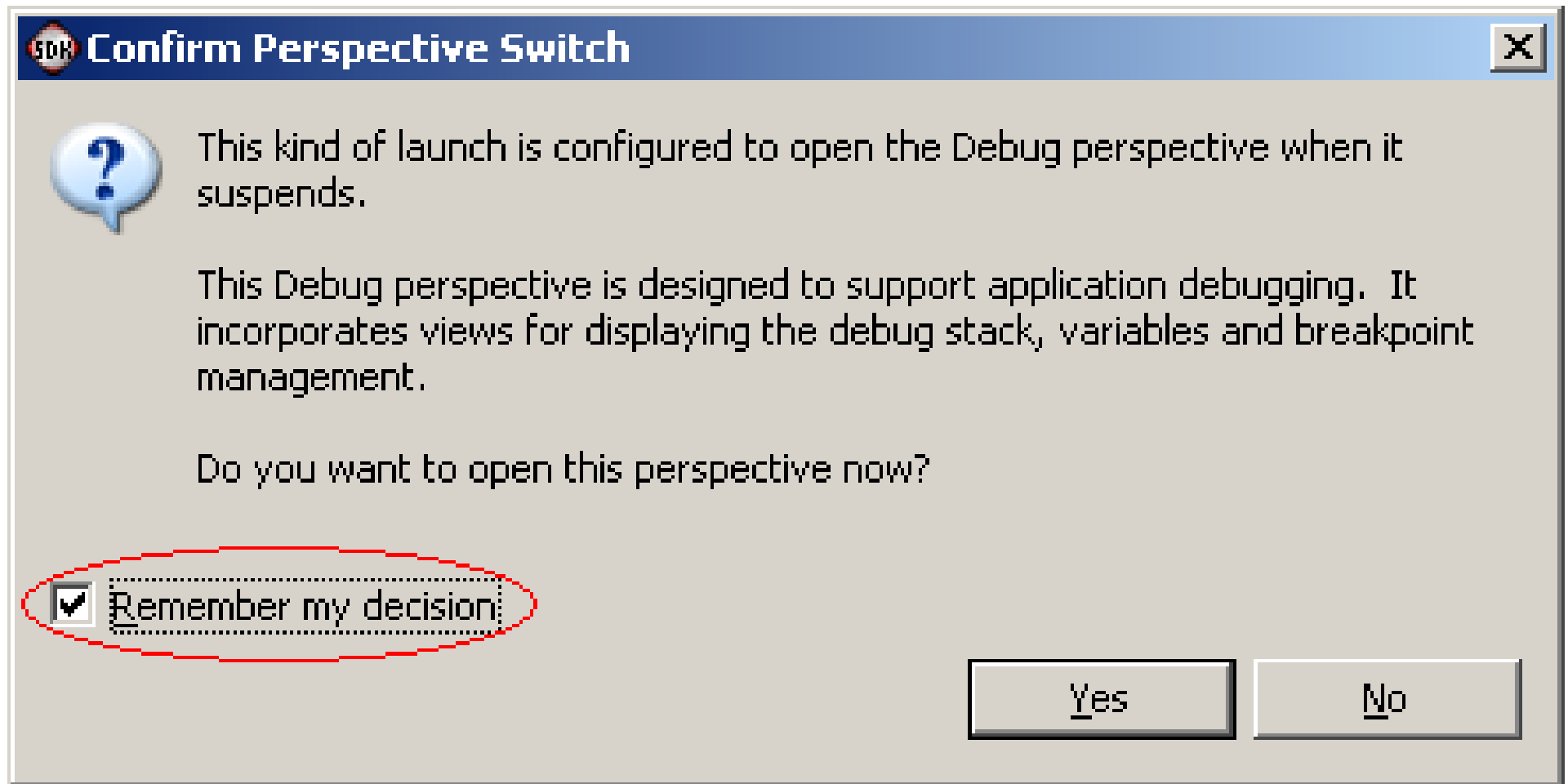
step on memory_tests_0 application and choose Debug menu



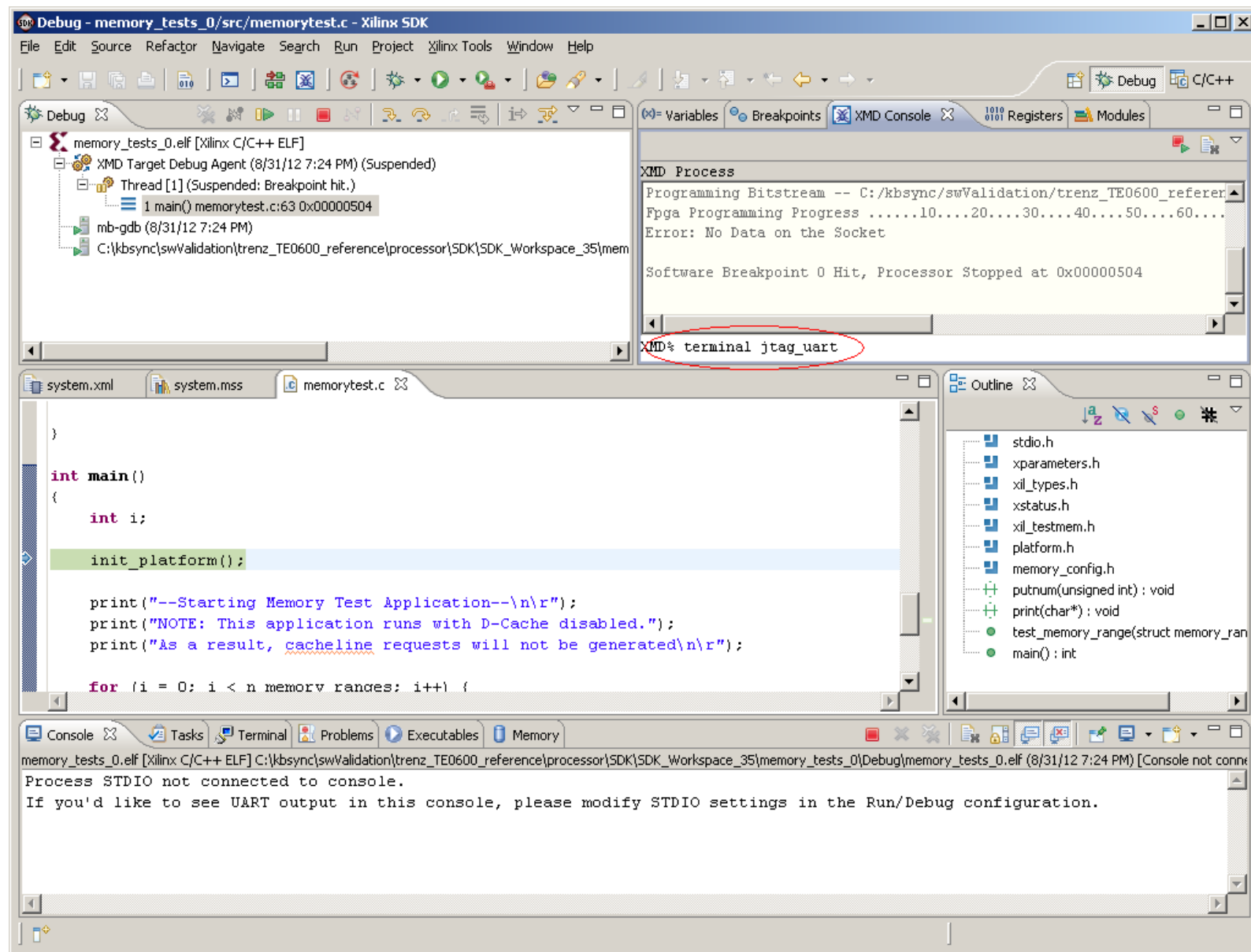
Confirm launch on a hardware



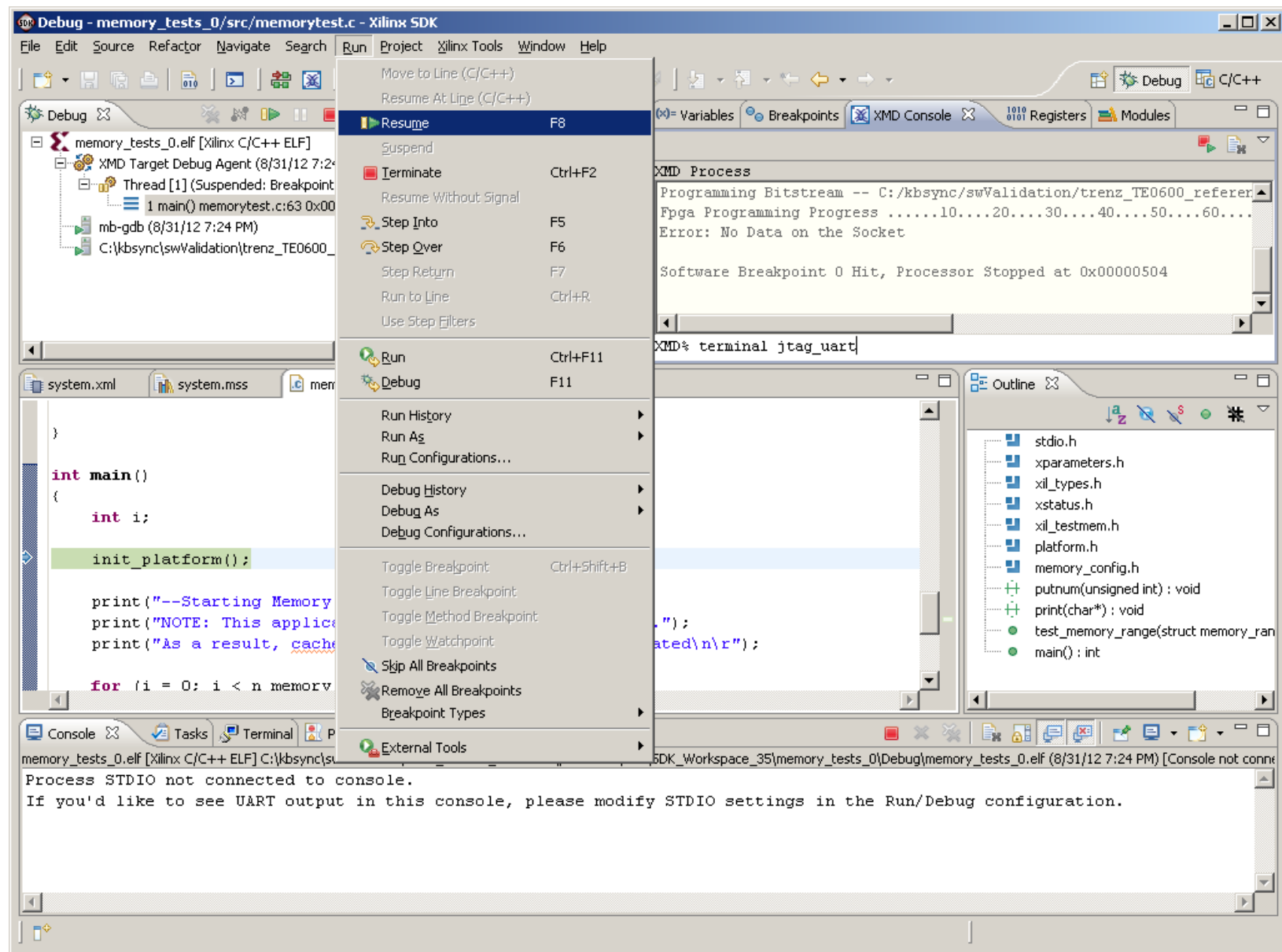
choose remember decision and confirm switching
to
Debug design by clicking Yes button



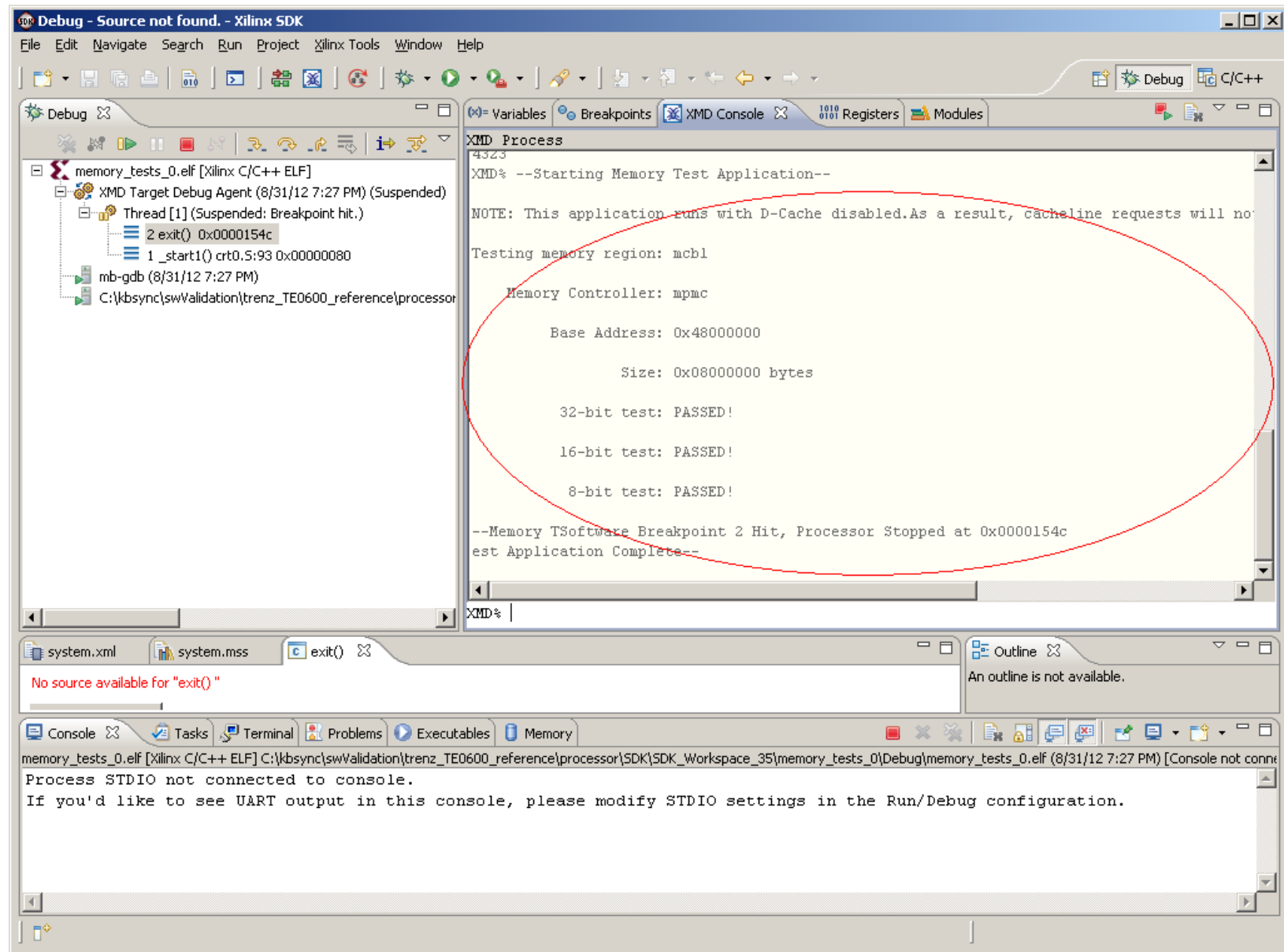
switch to XMD Console tab and type command
"terminal jtag_uart"



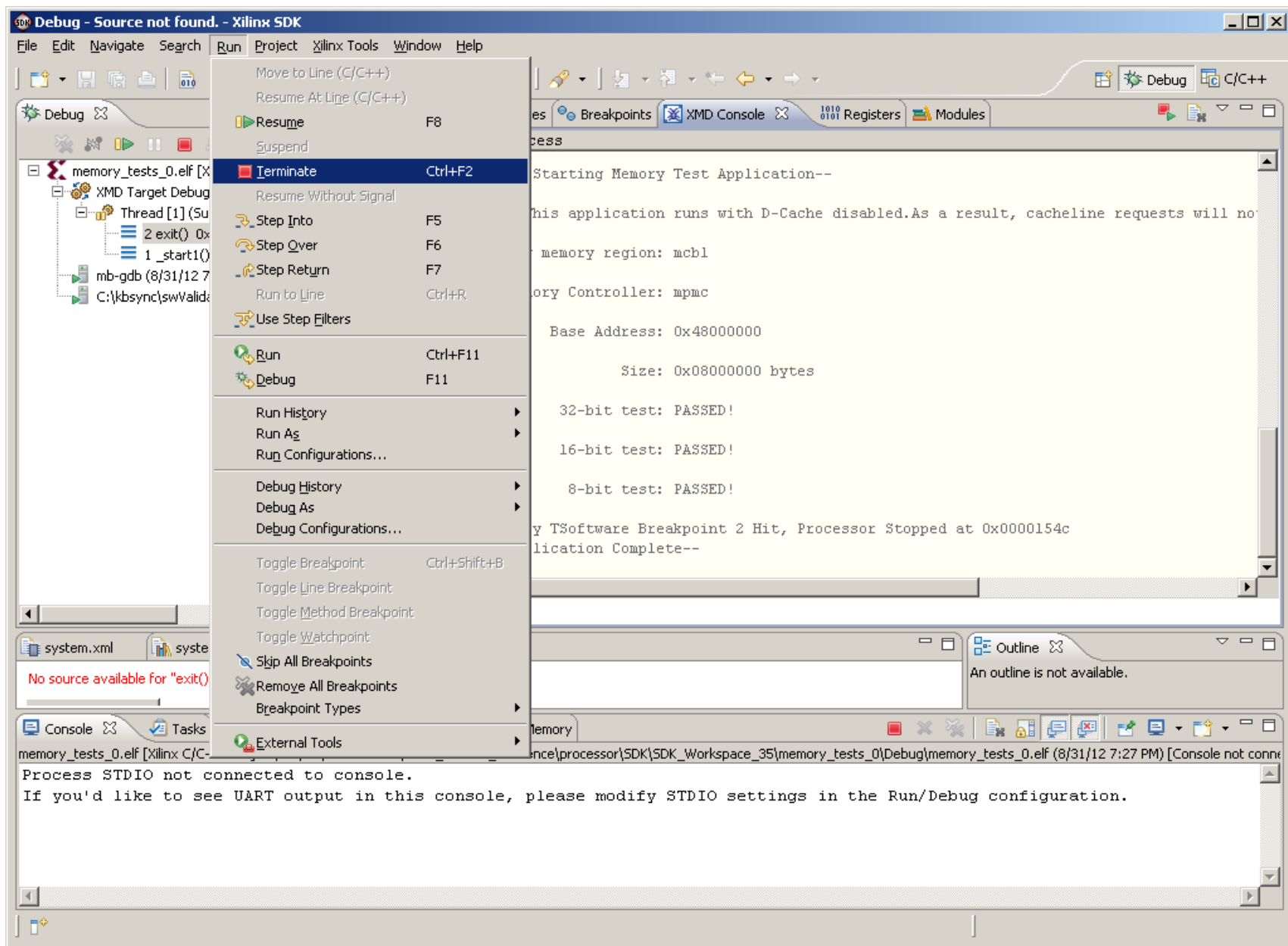
resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application



TE0600 board configuration complete

external memory configuration
confirmed with test application