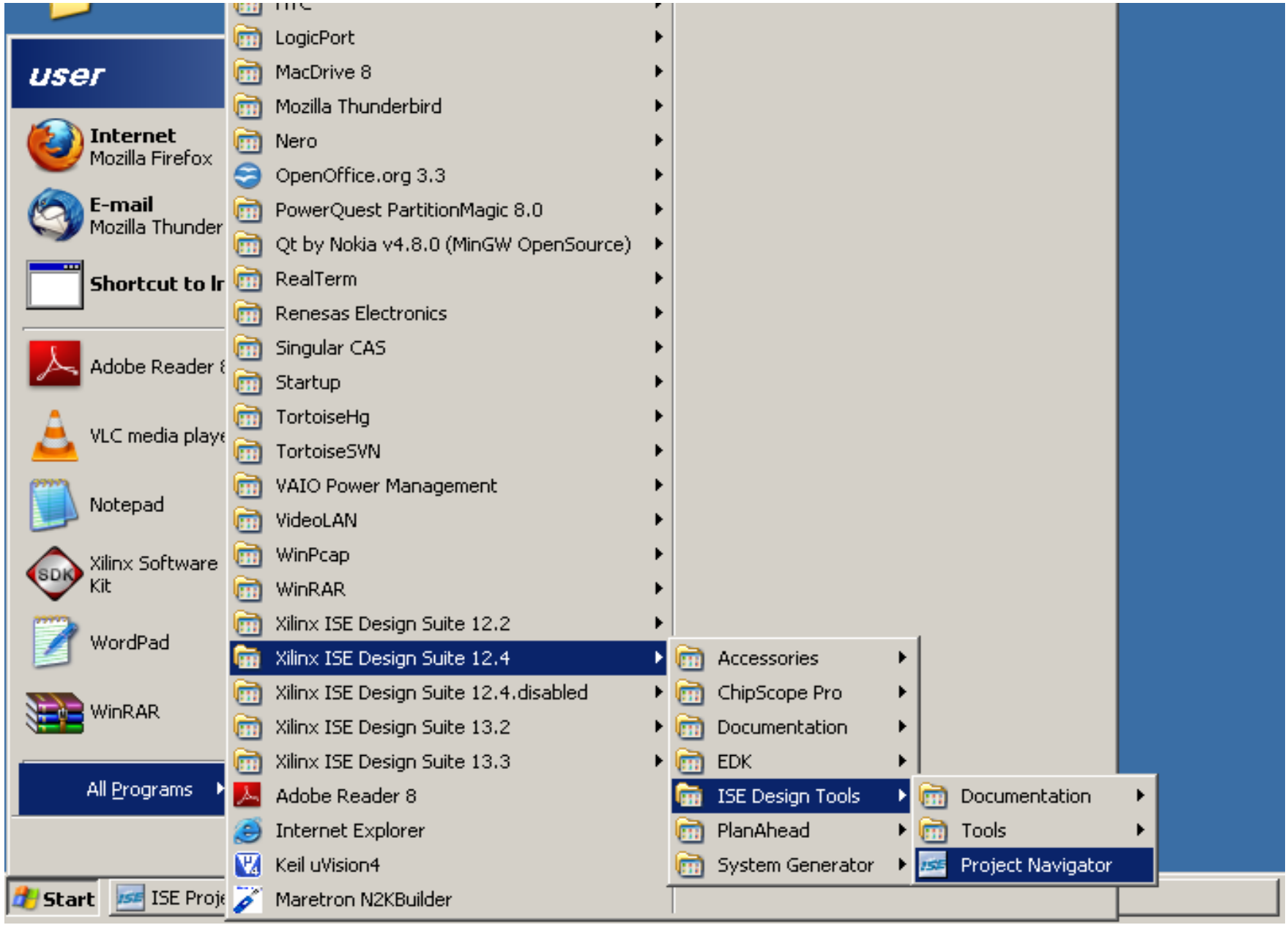
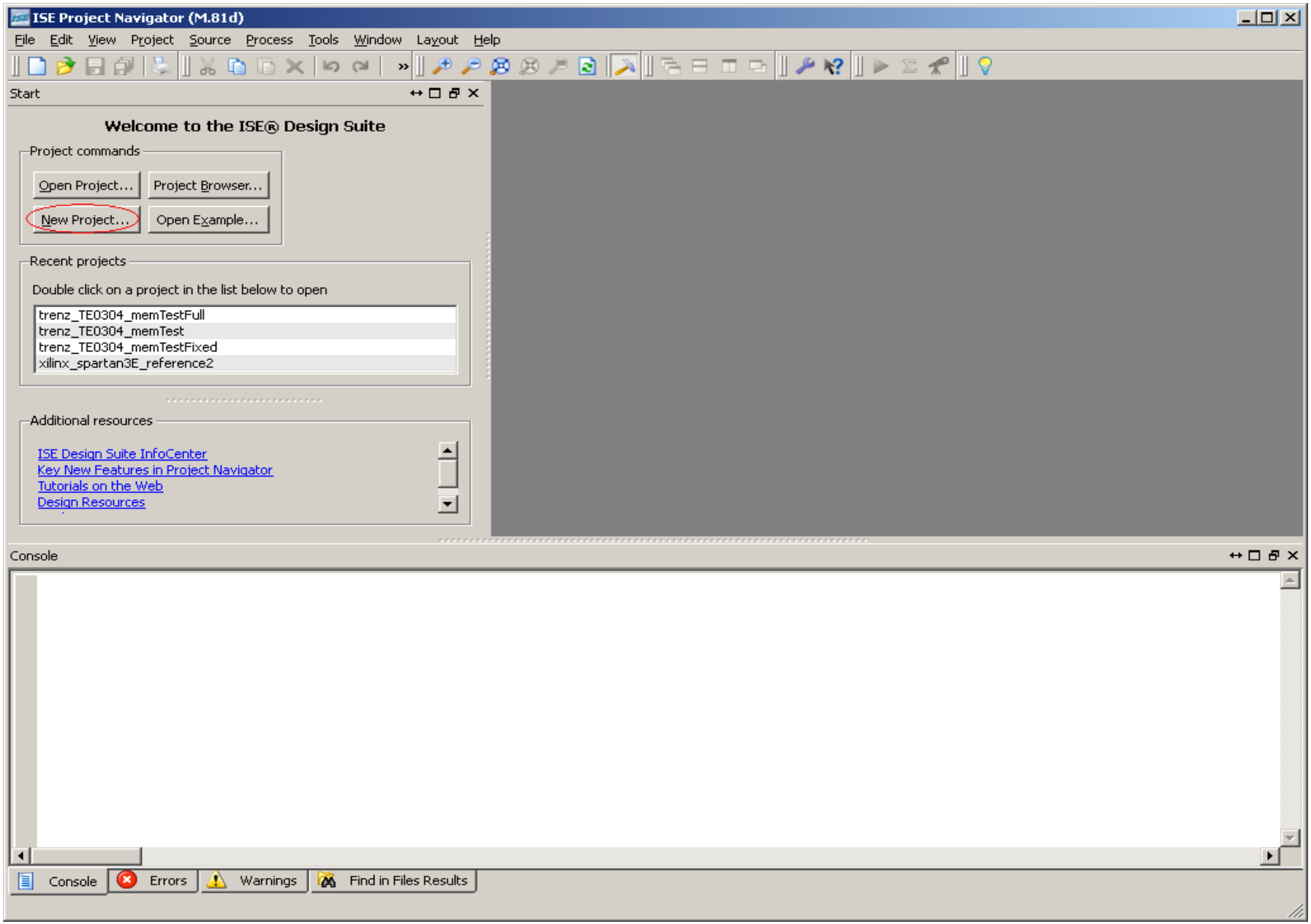
TE0630 platform

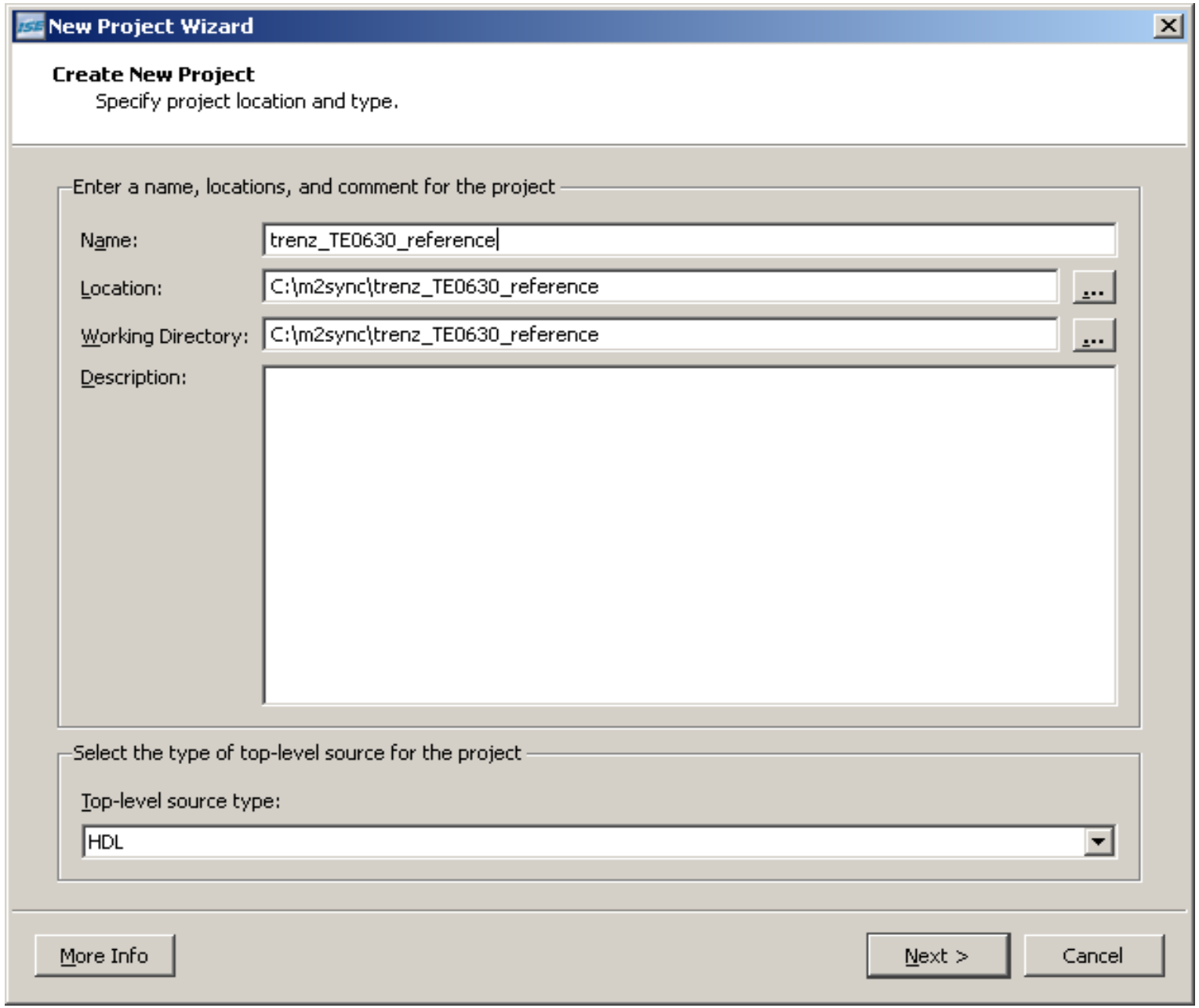
reference project creation sequence



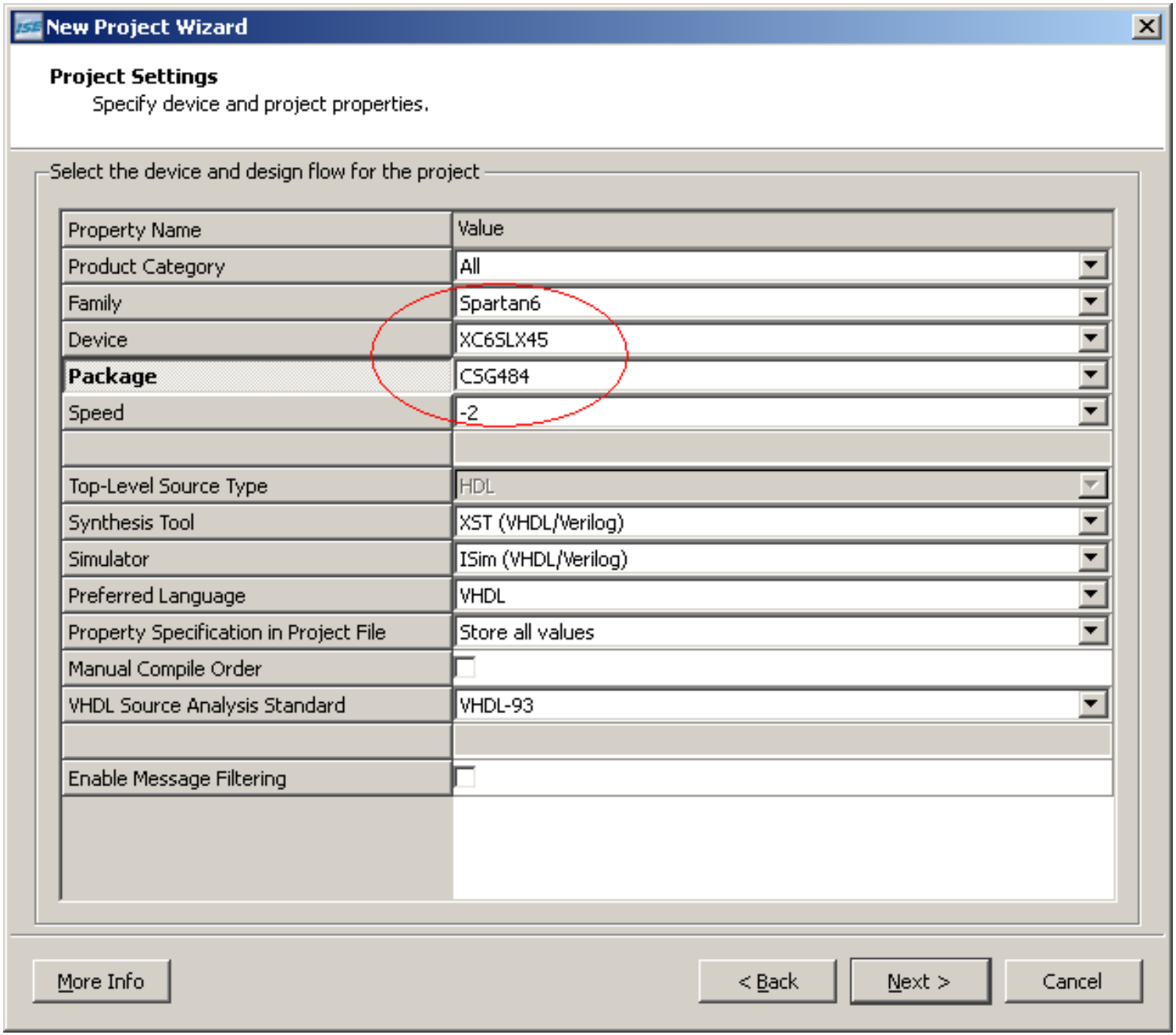
start Xilinx ISE Project Navigator



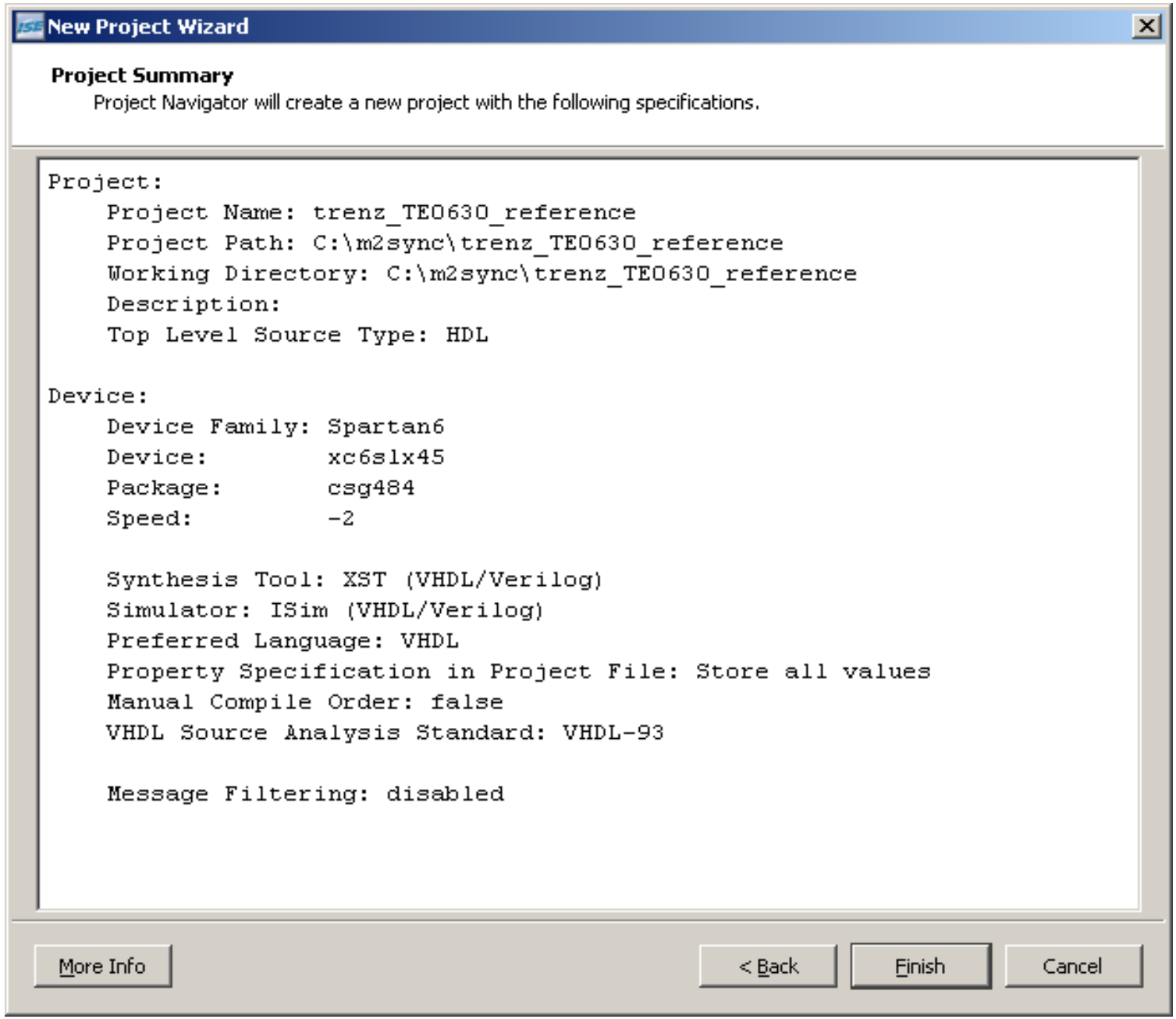
click button to create a new project



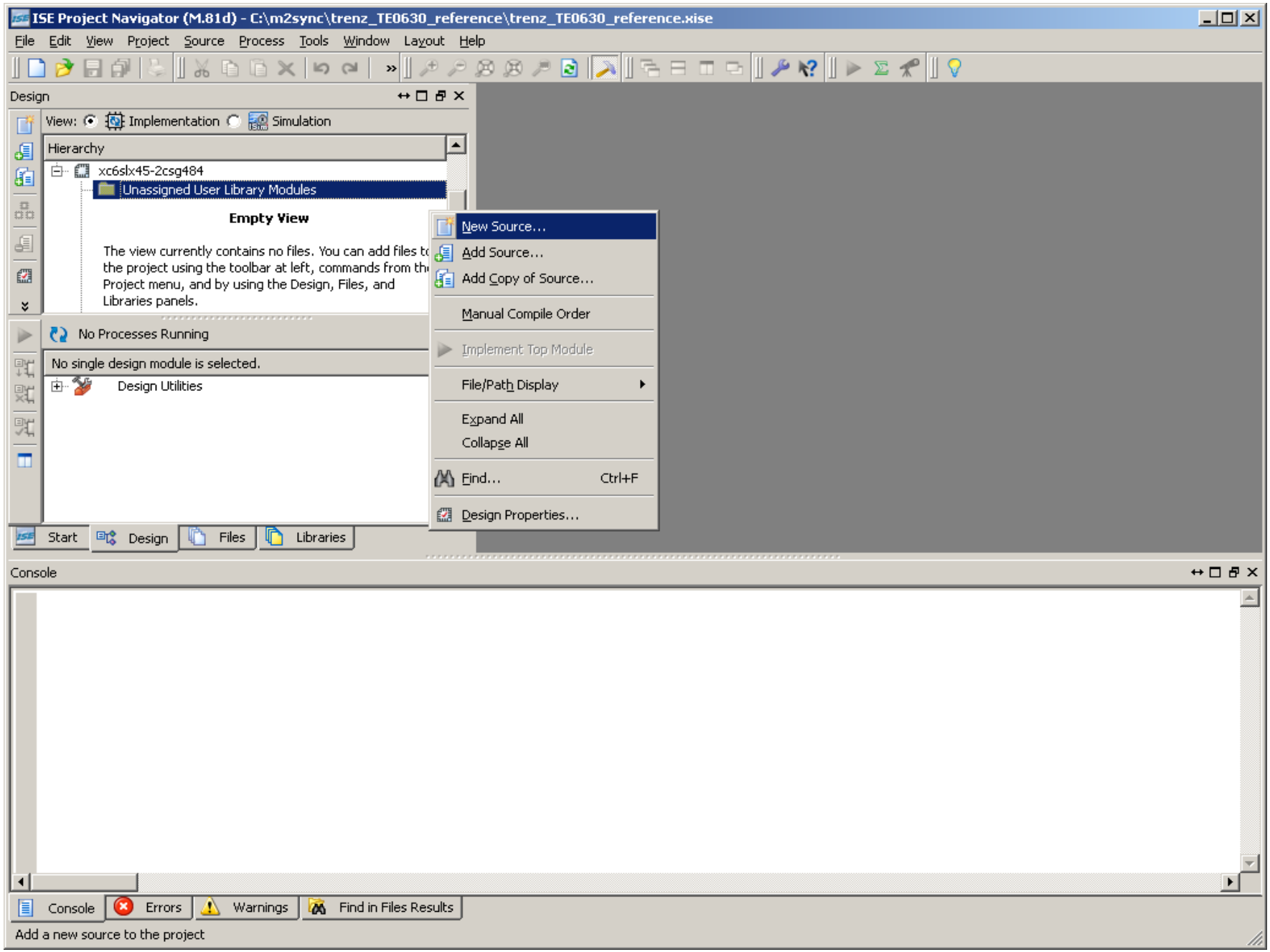
choose project name, then click Next



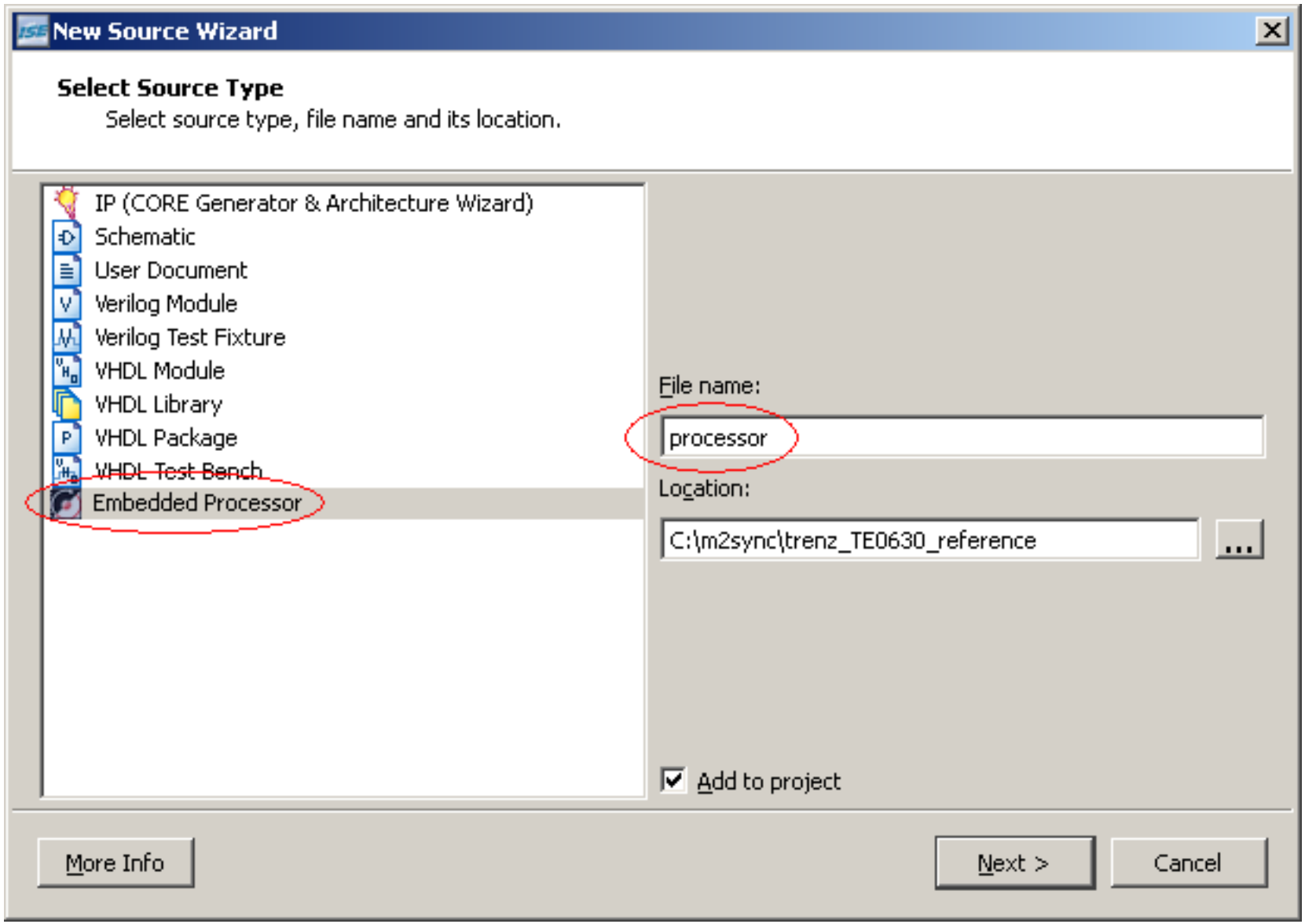
provide correct Family, Device, Package and Speed, then click Next



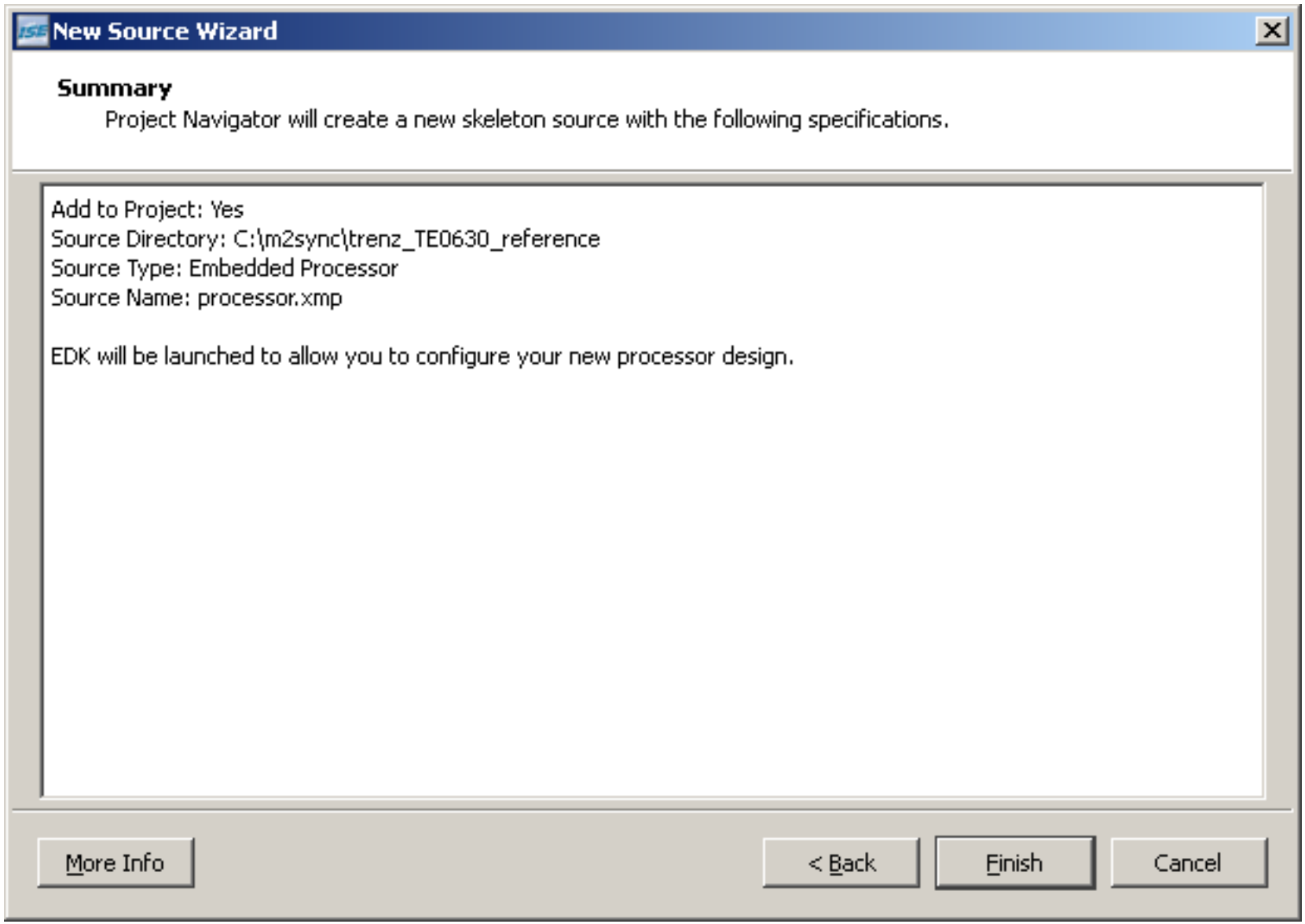
verify configuration and click Finish



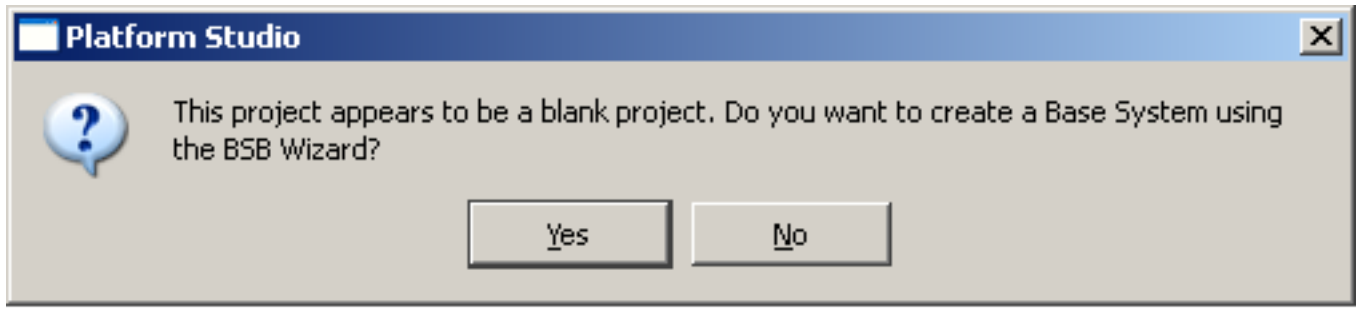
right button menu to add New Source



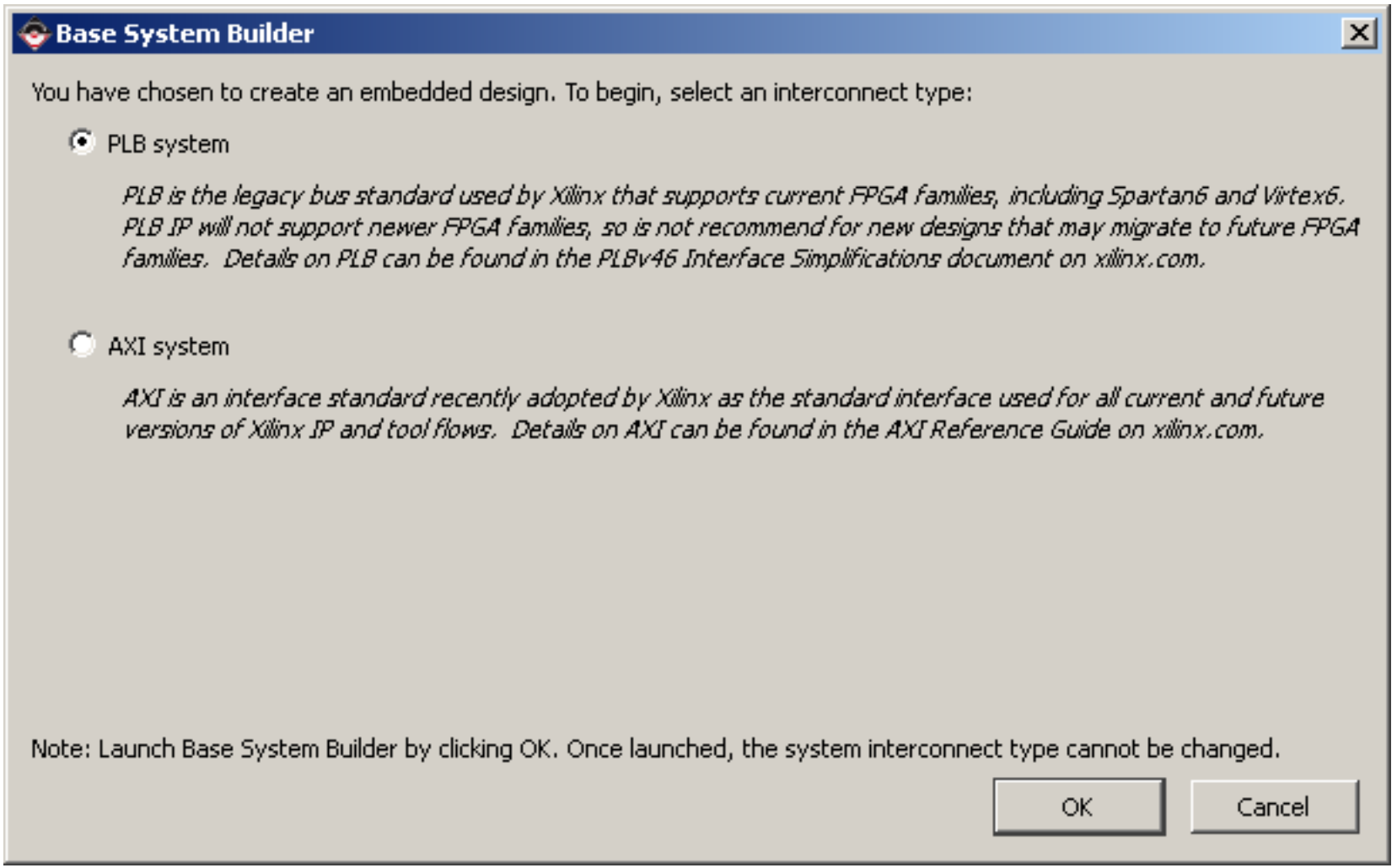
choose Embedded Processor, provide File name then click Next



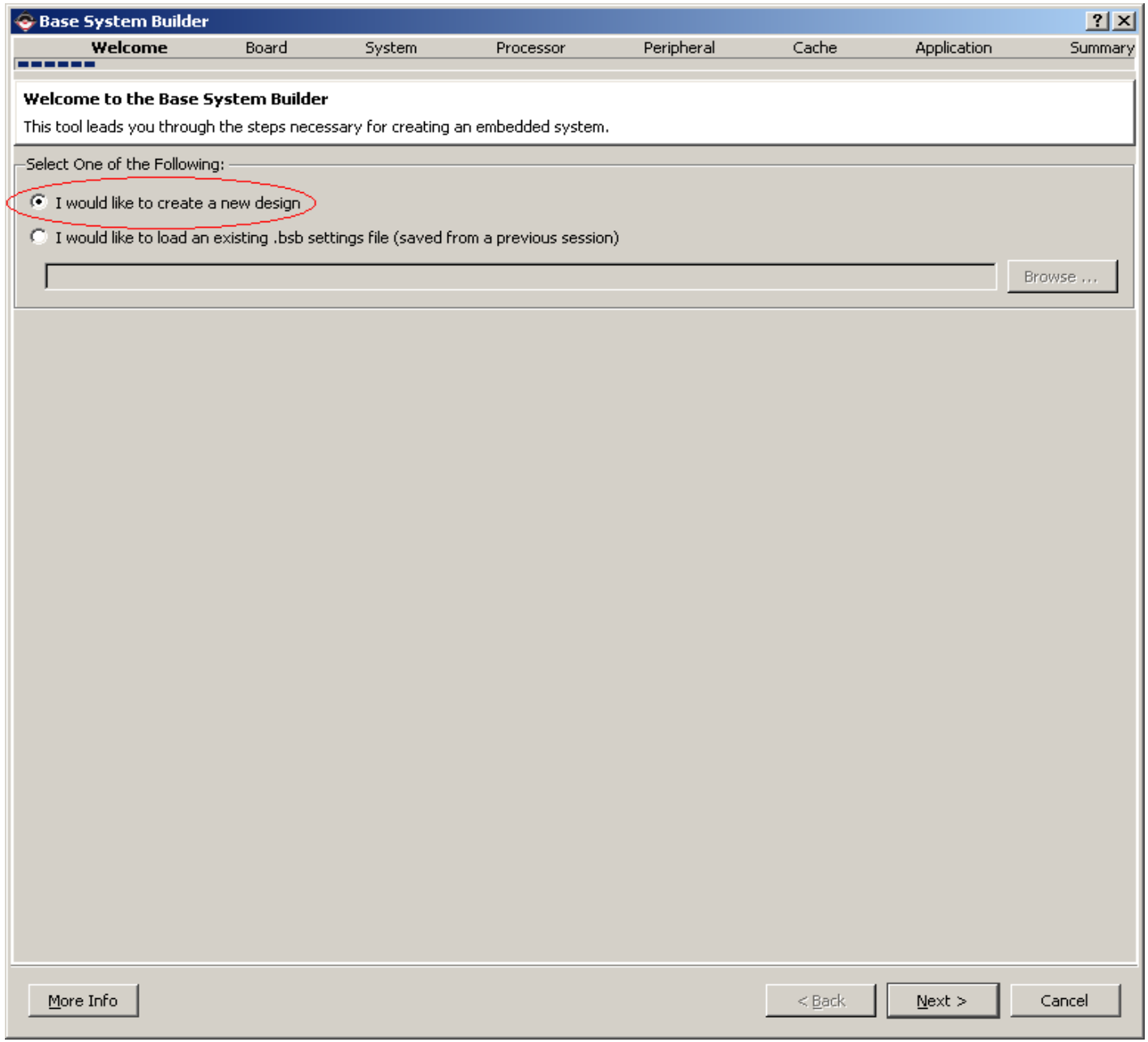
verify configuration then click Finish



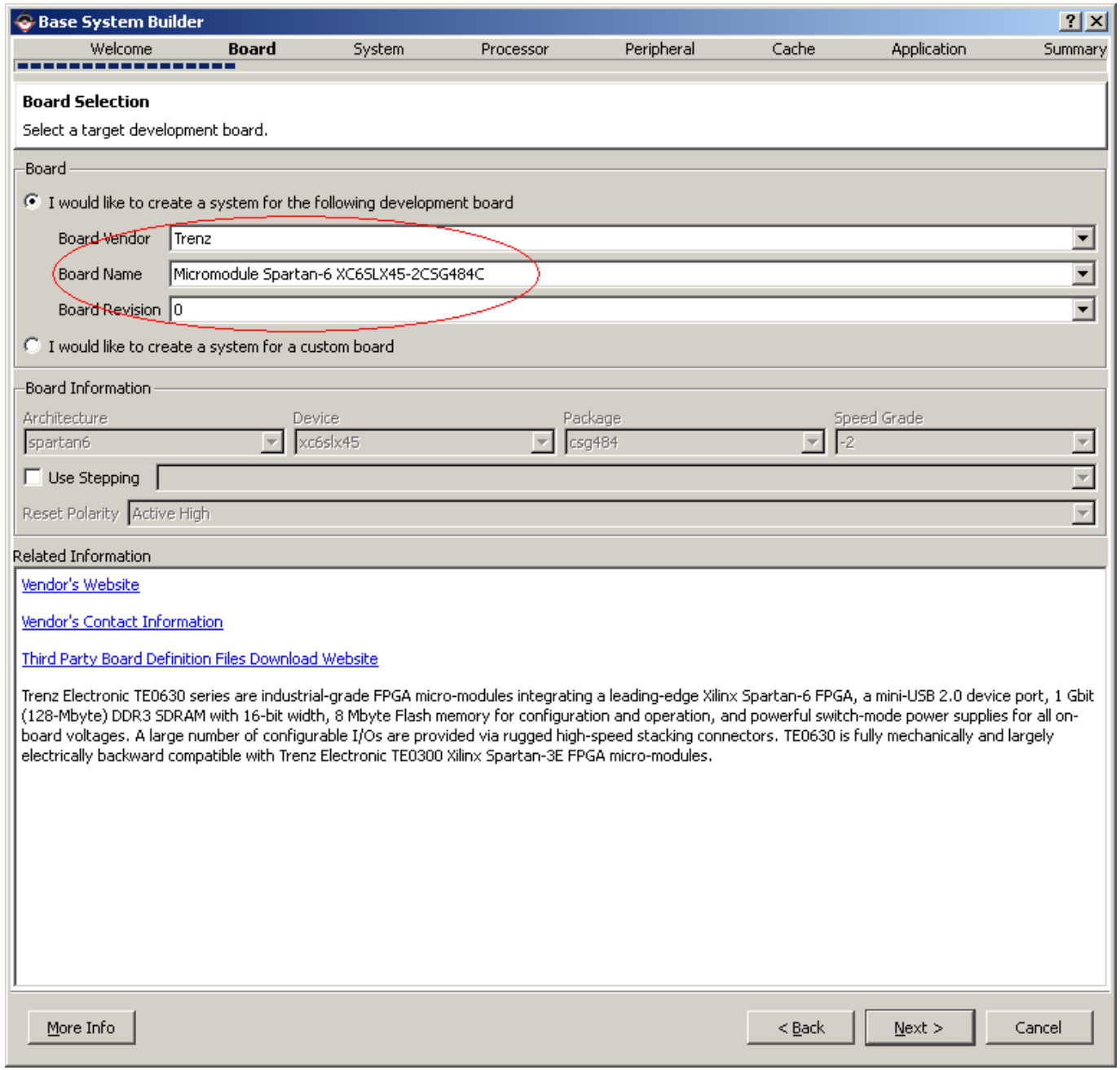
confirm Yes to launch BSB Wizard



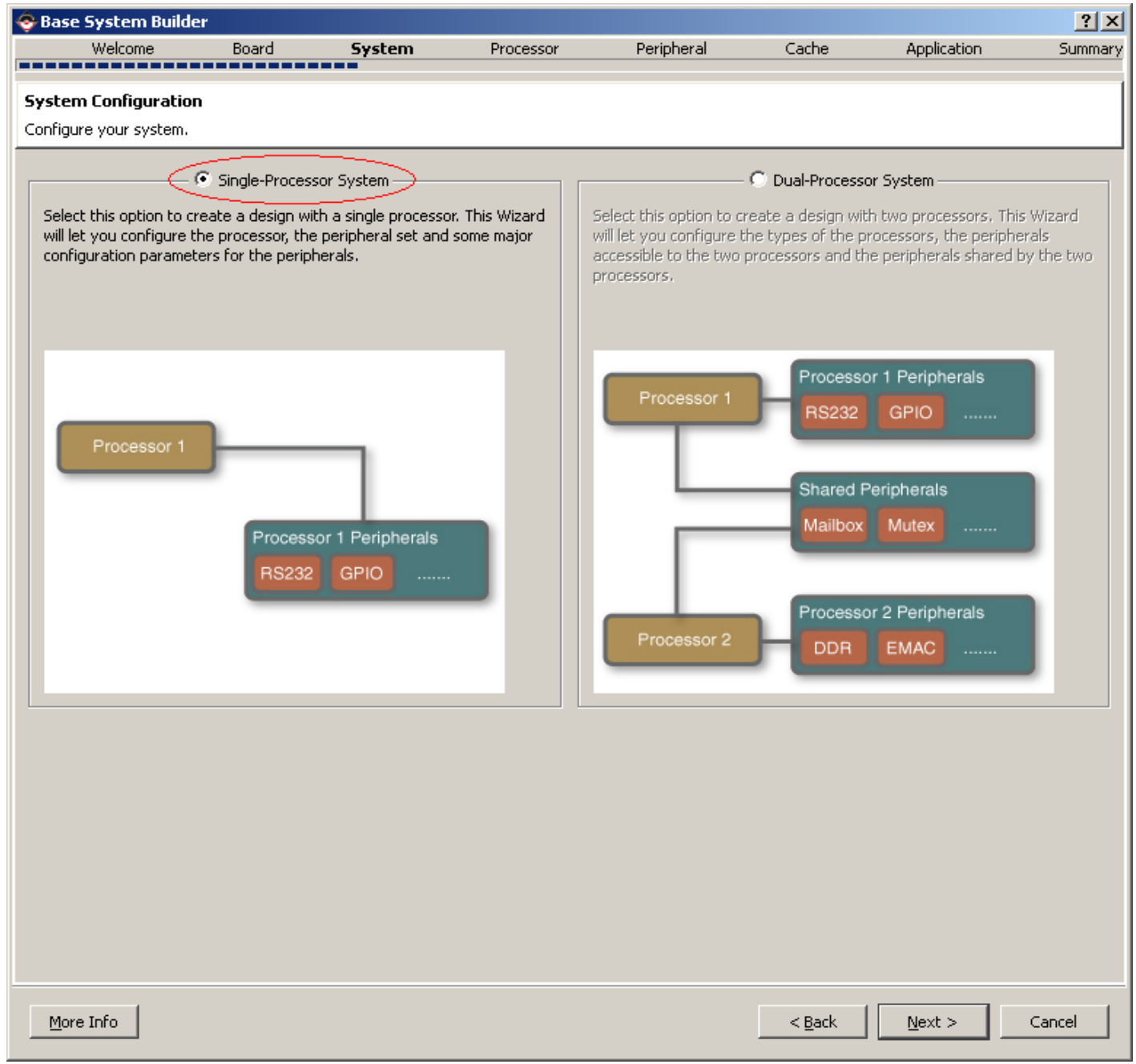
choose PLB system



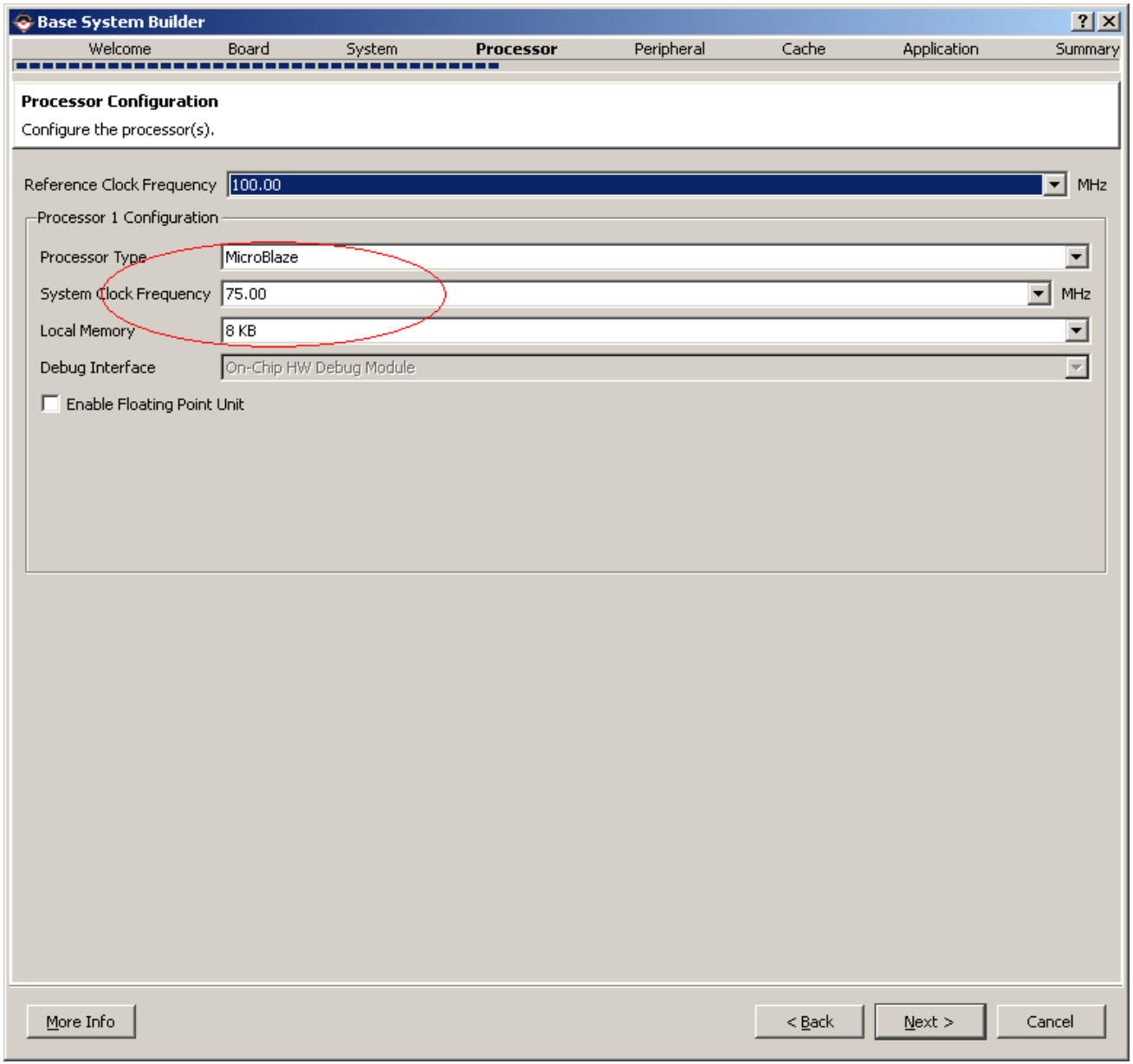
choose create new design then click Next



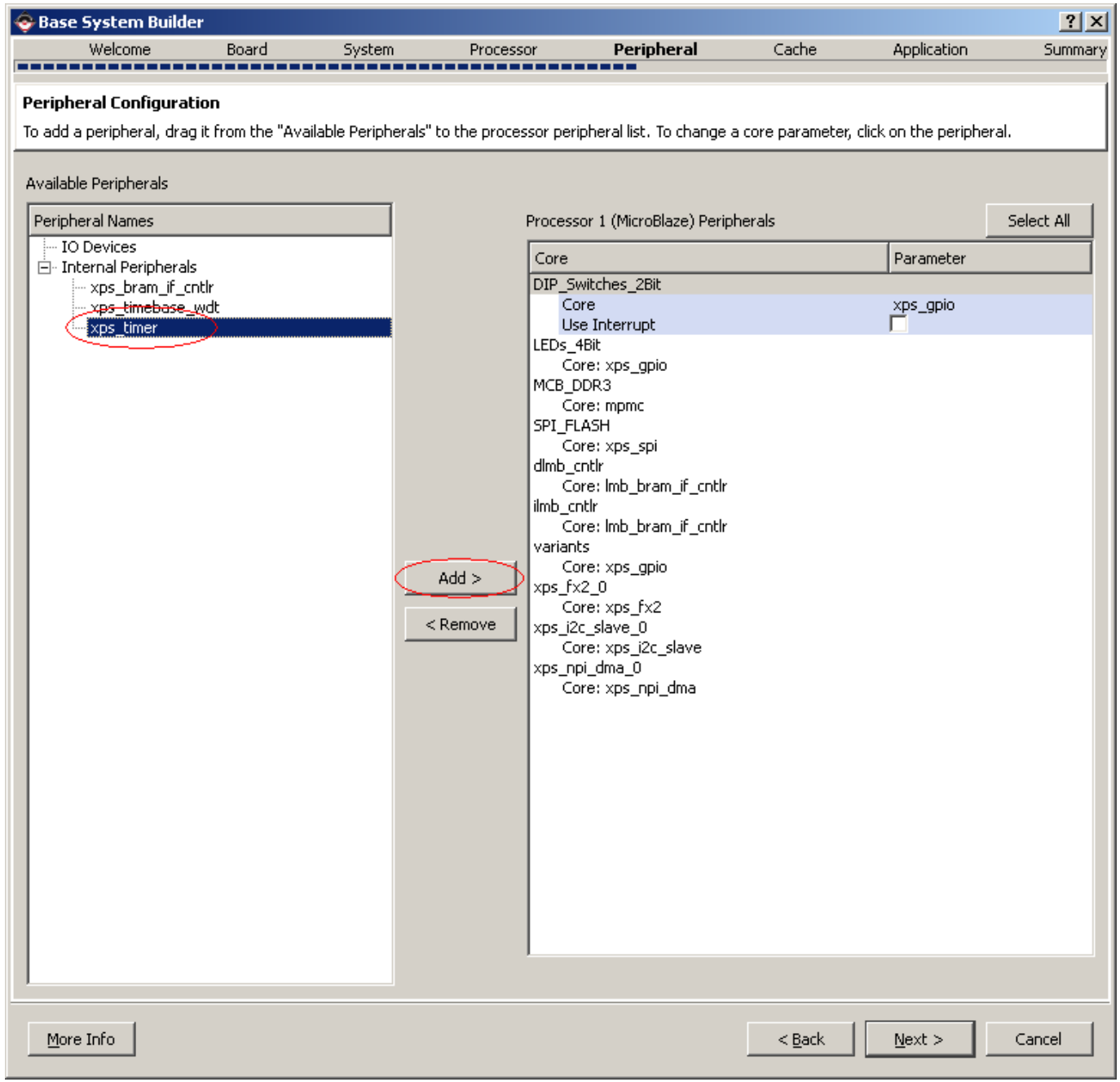
choose correct Vendor, Name and Revision then click Next



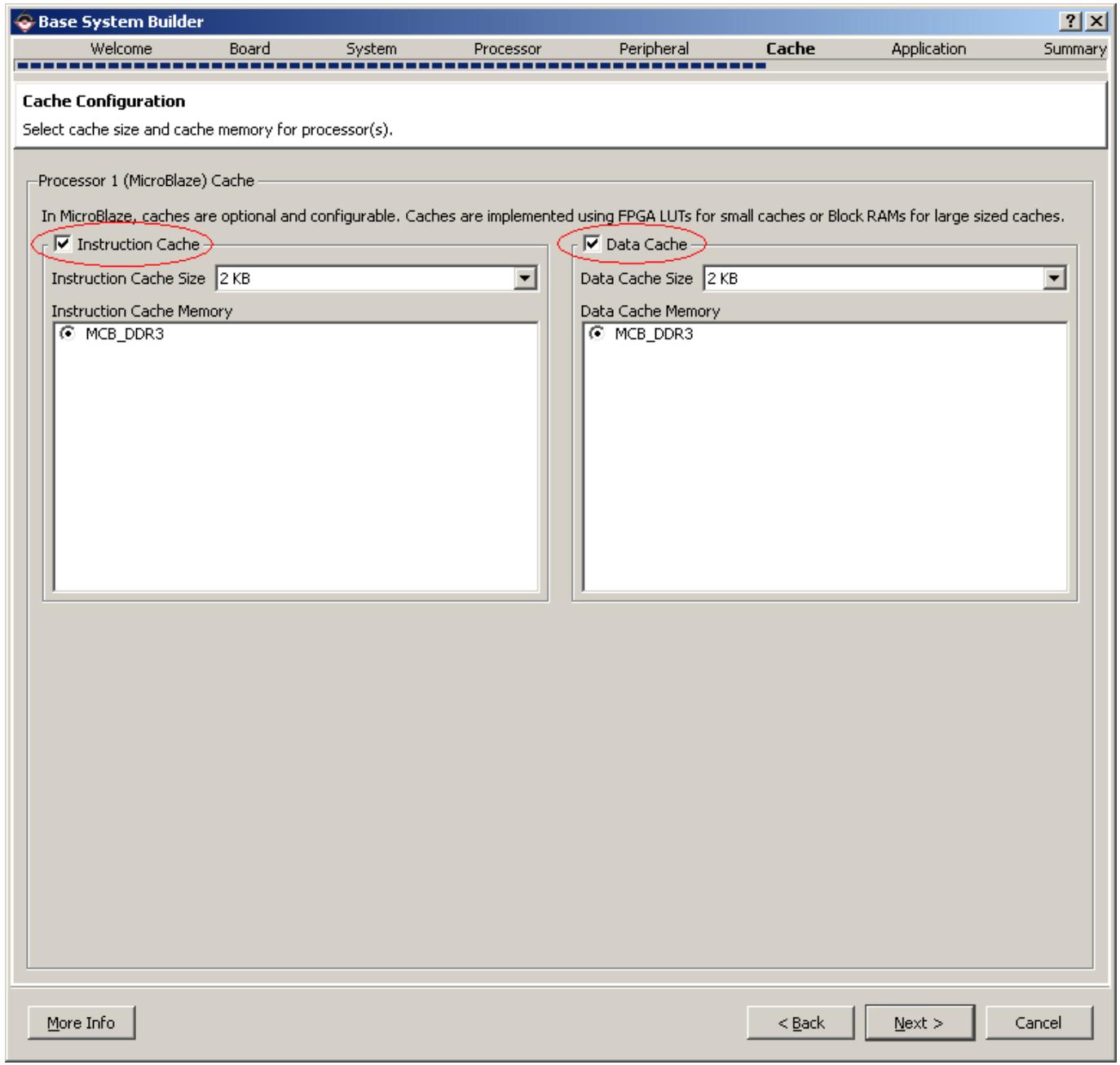
choose Single-Processor System then click Next



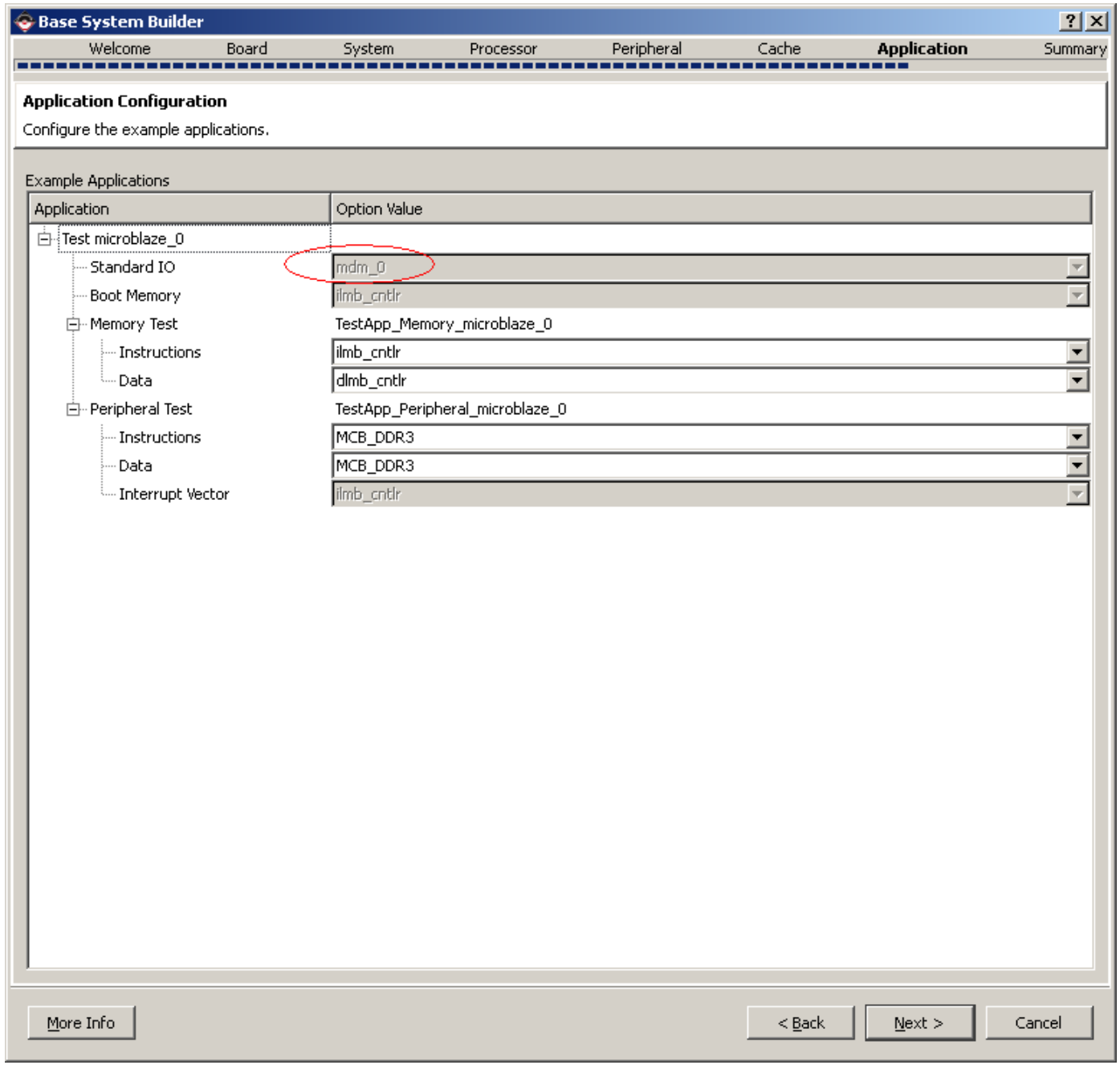
choose default Processor Type, System Clock Frequency (it will be fixed later) and Local Memory size then click Next



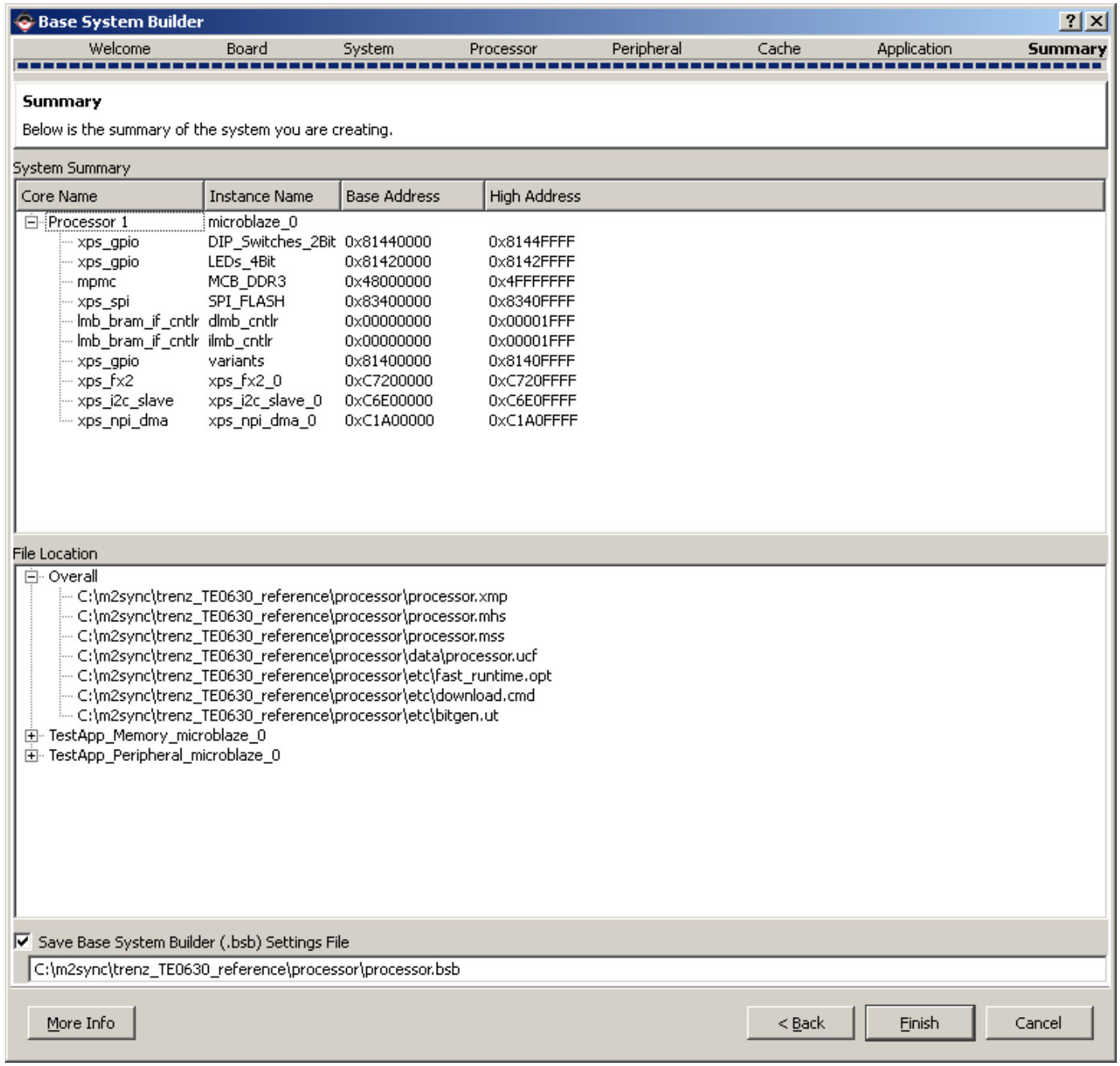
add xps_timer (XilKernel required), then click Next



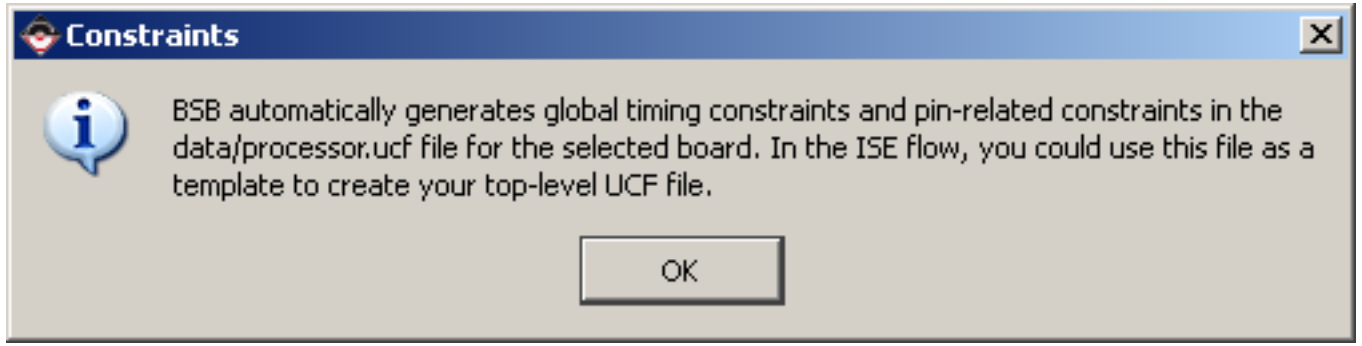
enable Instruction and Data Caches then click Next



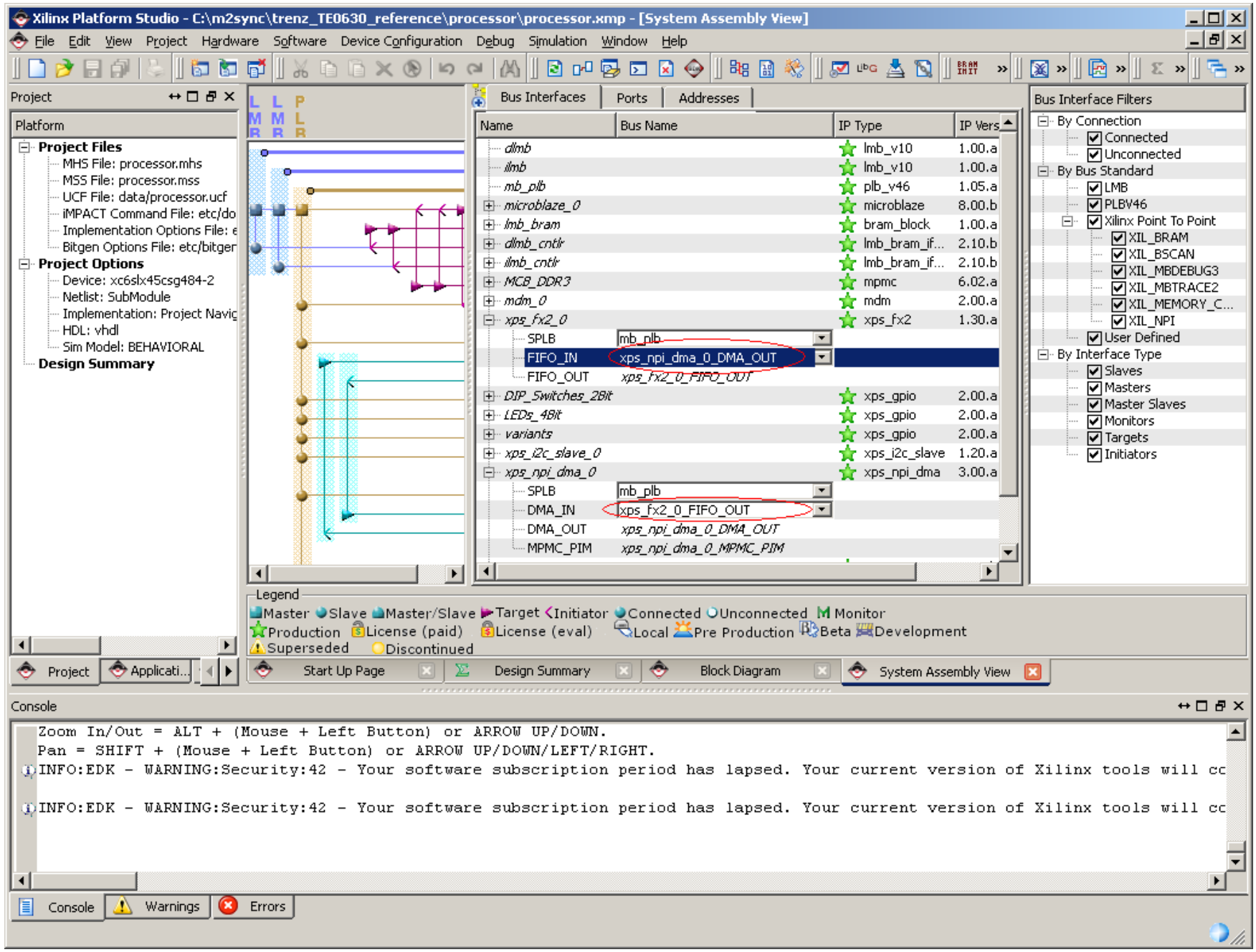
verify if mdm_0 choosen as Standard IO then click Next



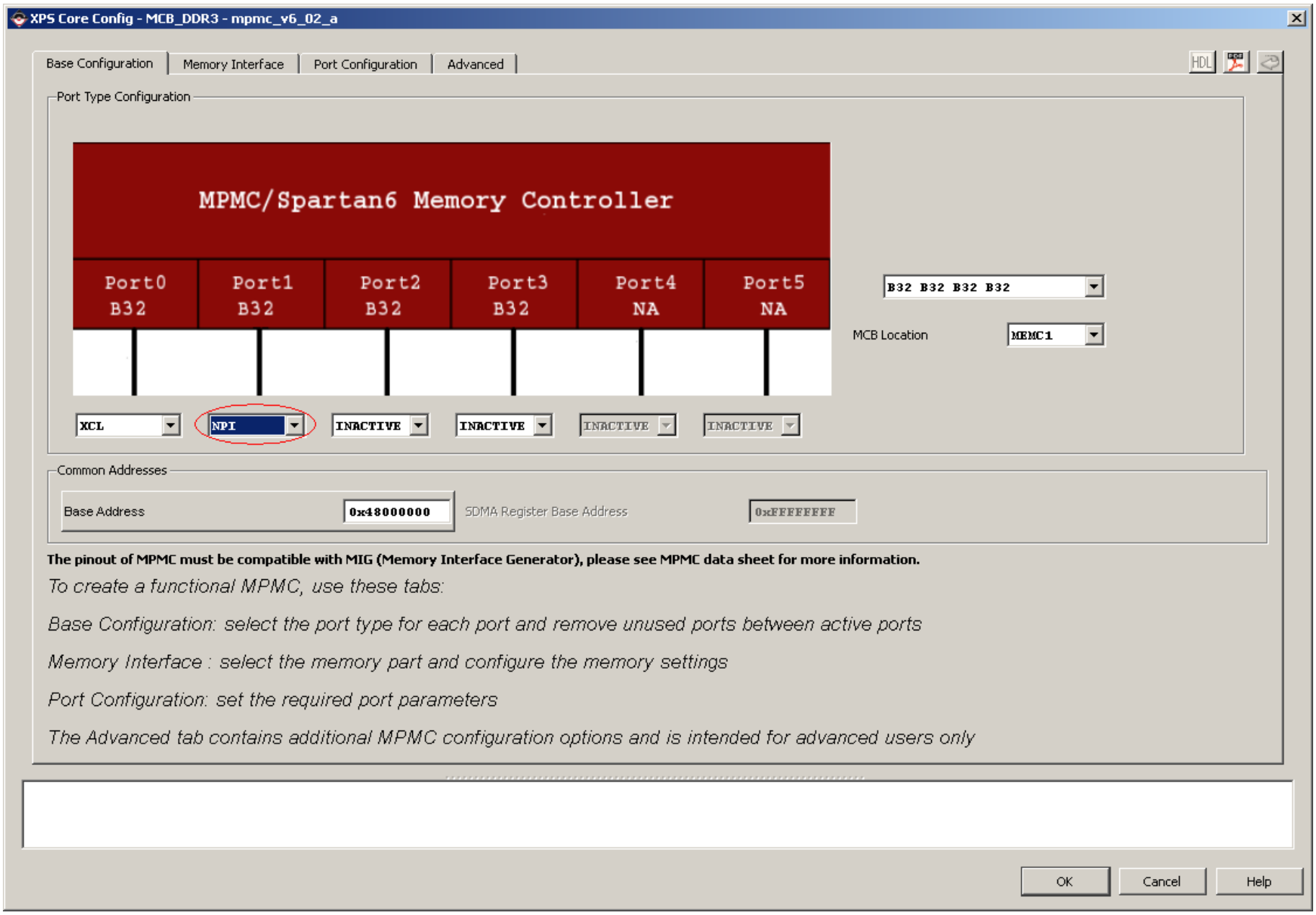
verify created configuration then click Finish



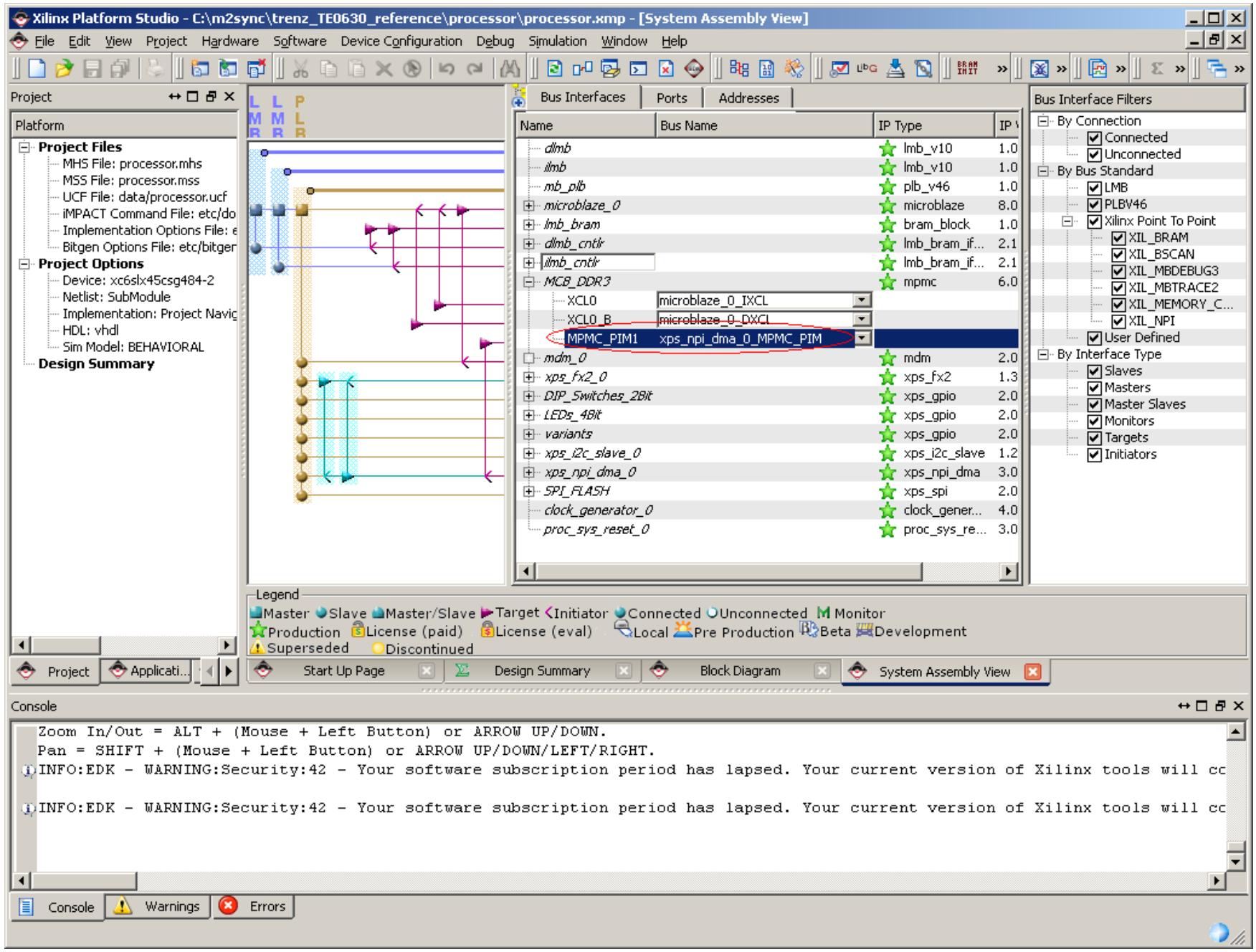
confirm UCF file creation



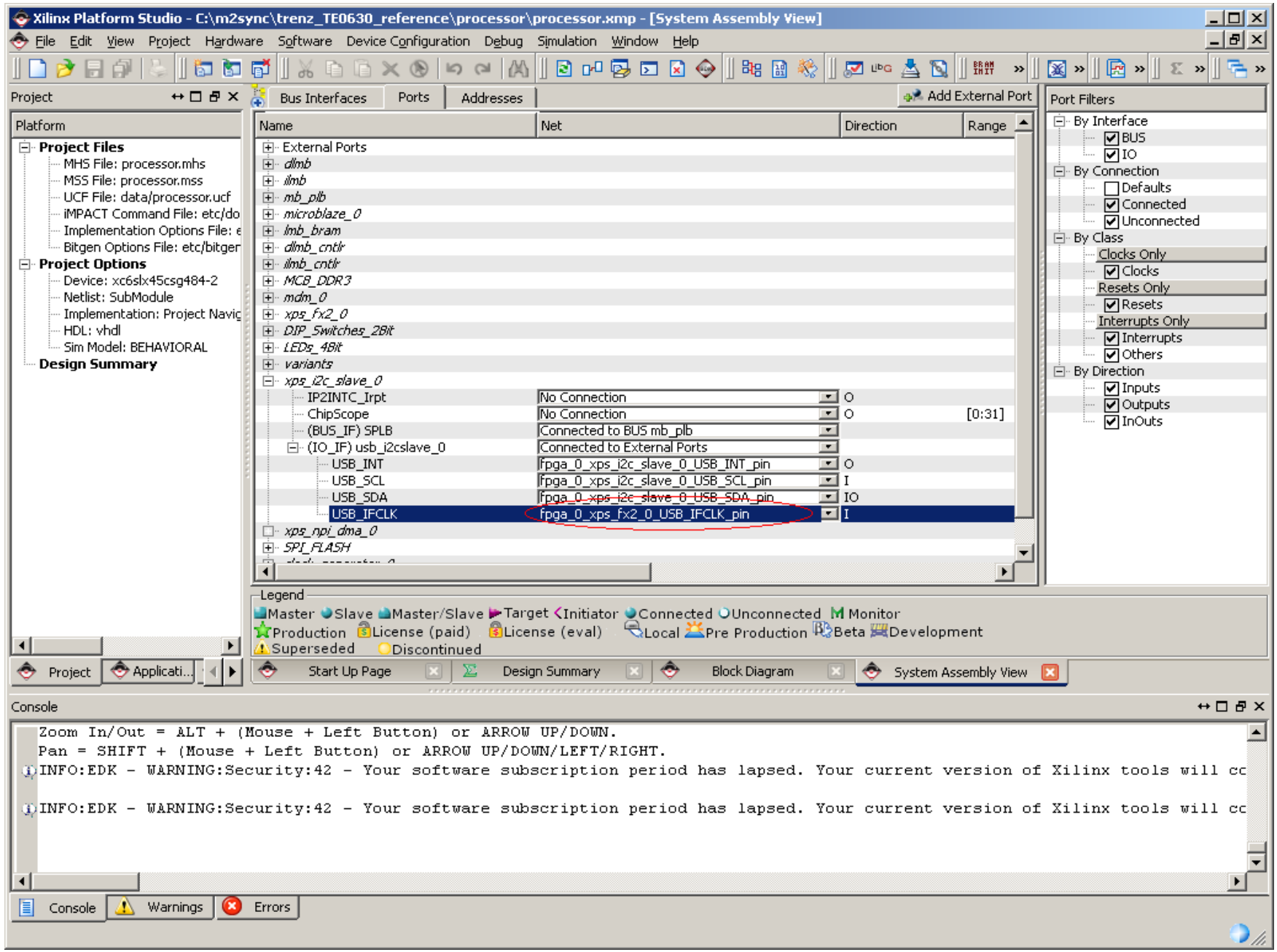
connect npi_dma and fx2 pcores to each other



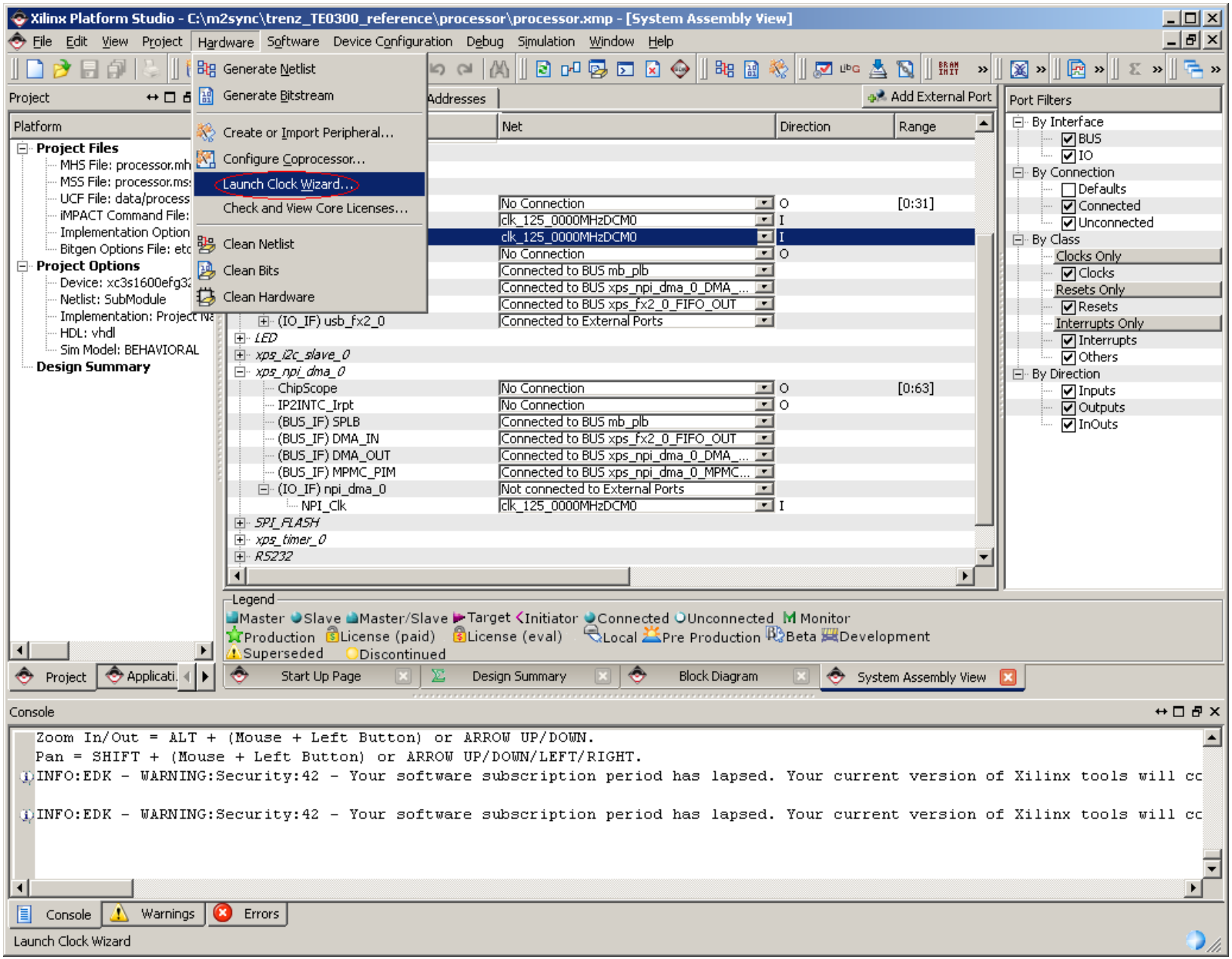
double click on MCB_DDR3 pcore and configure NPI port



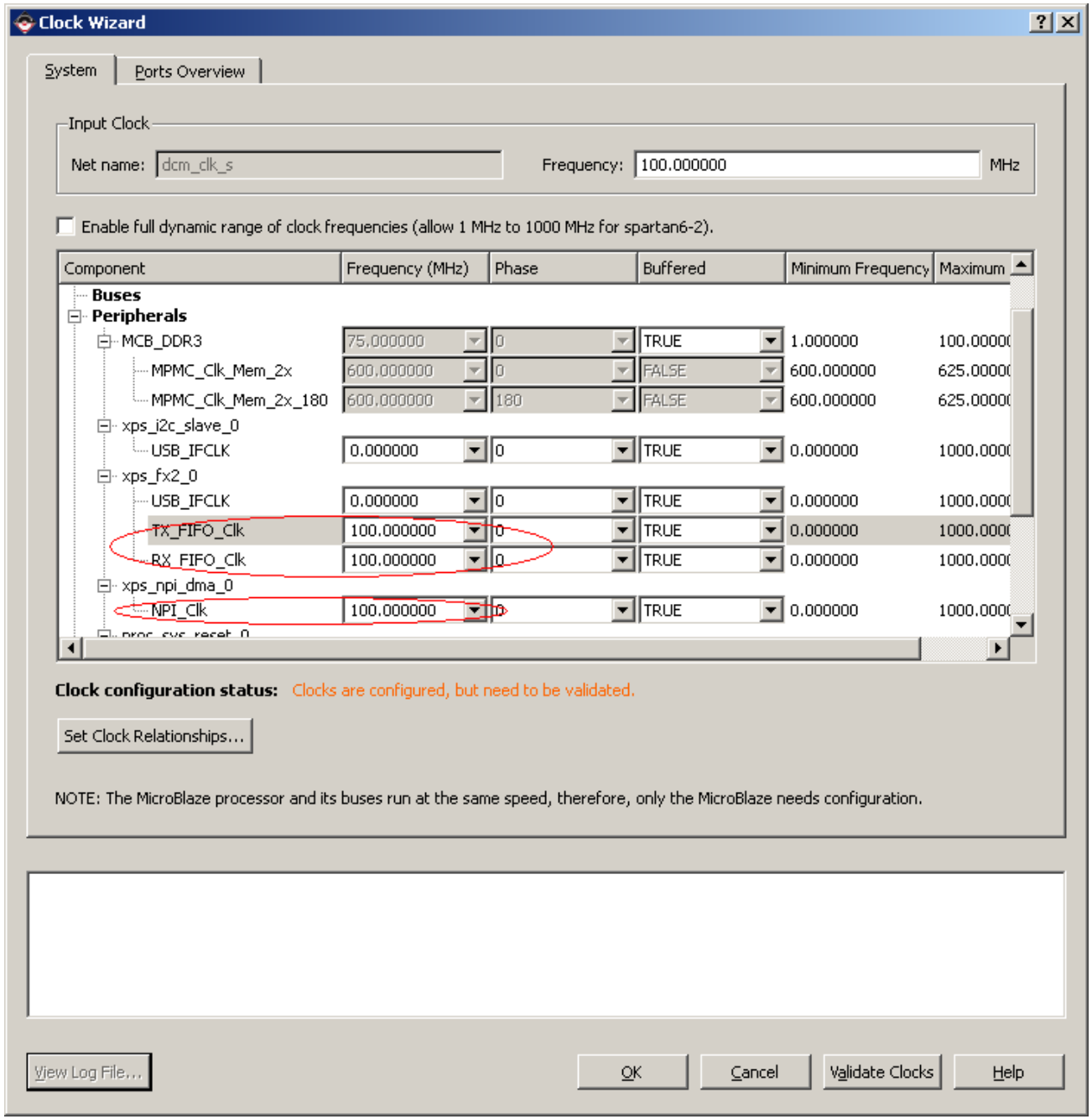
connect mpmc and npi_dma pcores



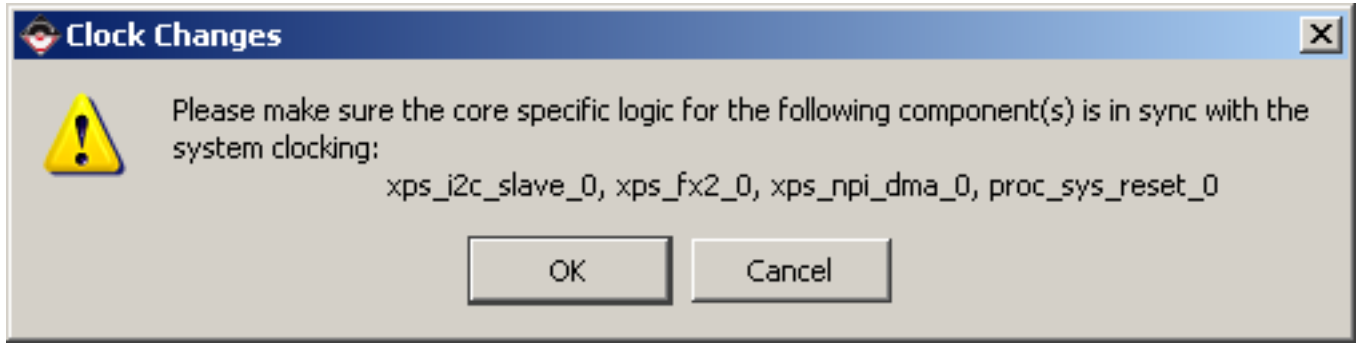
switch to Ports tab and connect xps_i2c clock signal



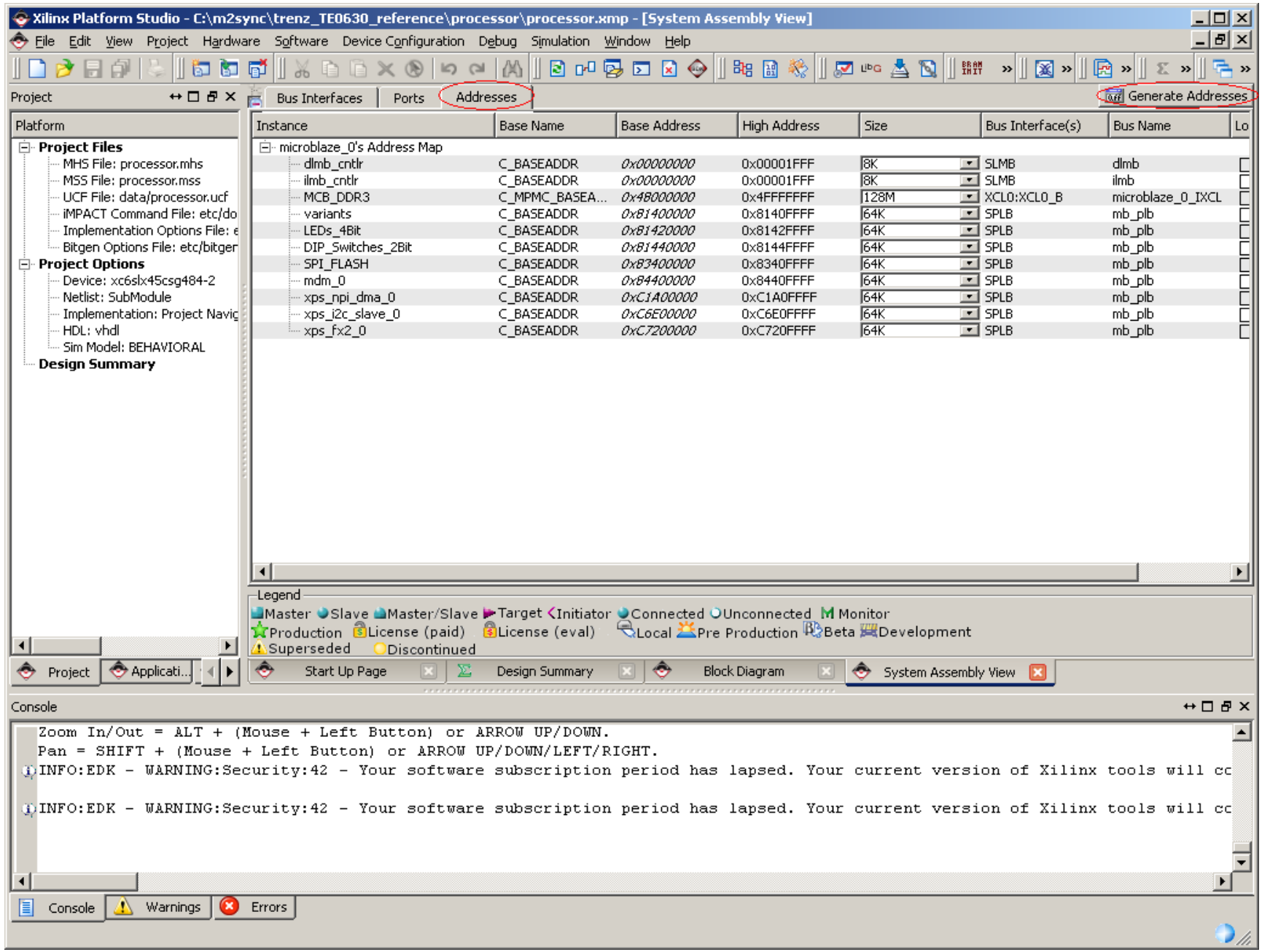
launch Clock Wizard



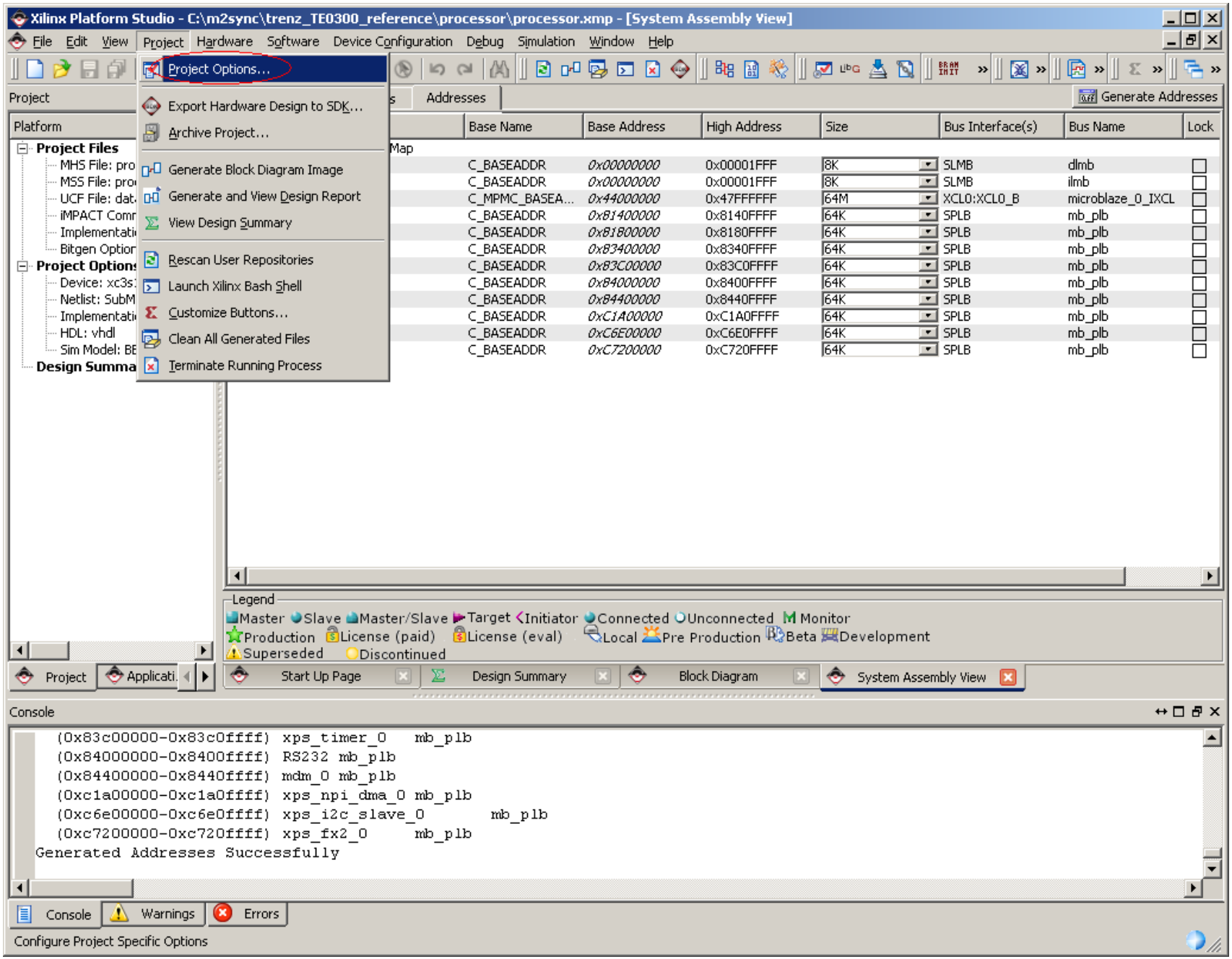
specify clocks for xps_fx2 and xps_npi_dma pcores, validate them, then click OK



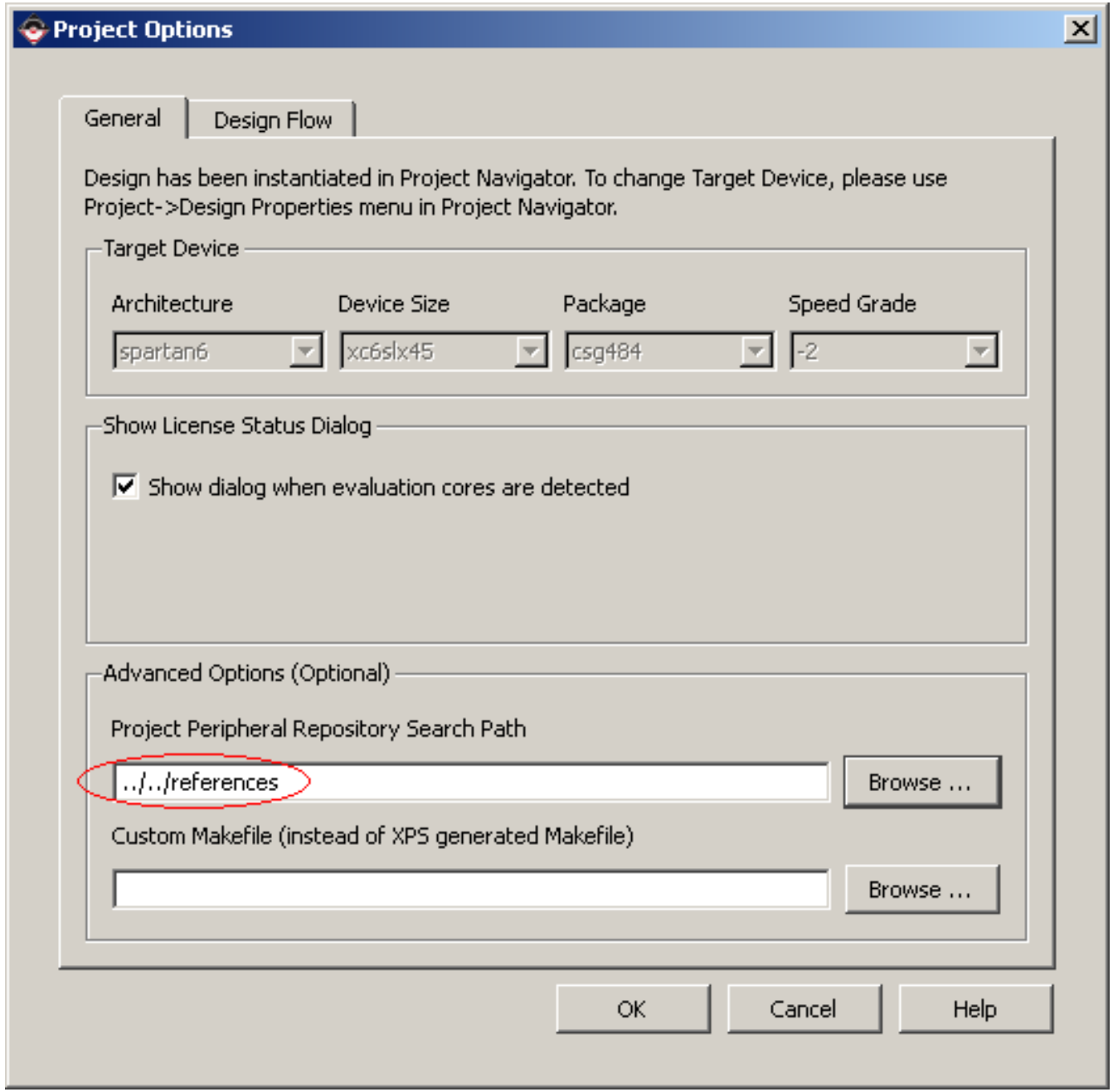
confirm Clock Changes



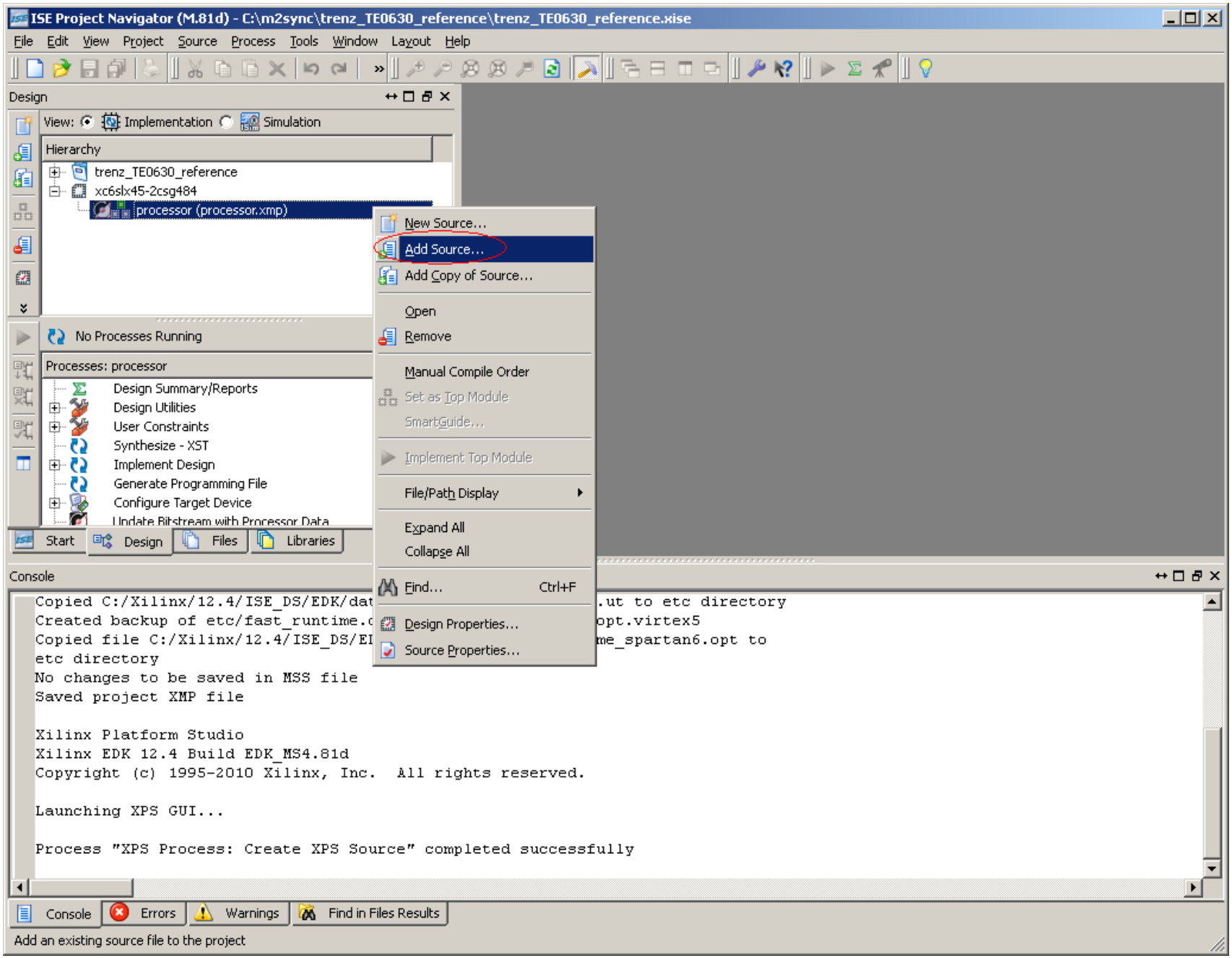
switch to Addresses tab and re-generate addresses



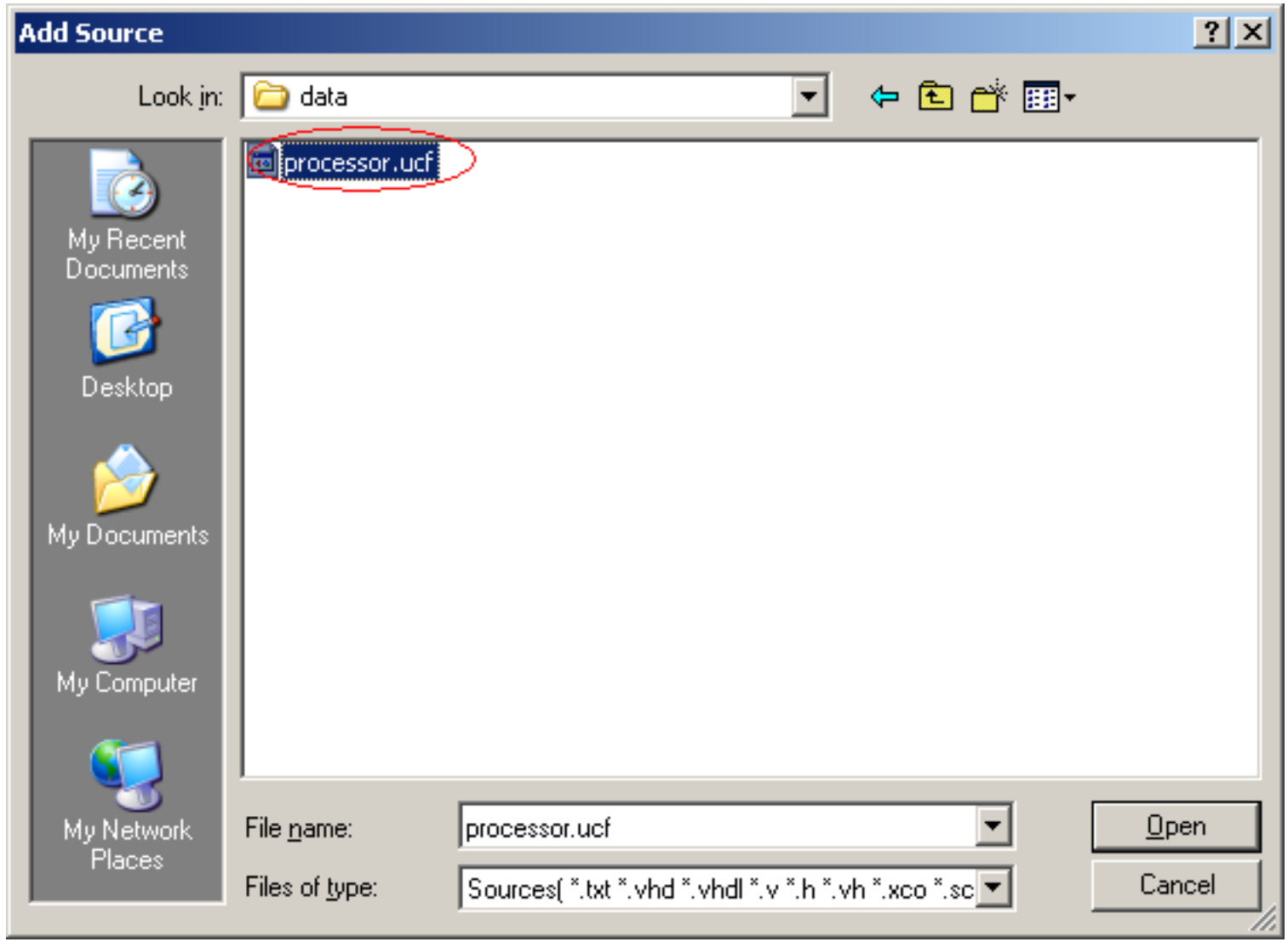
launch Project Options



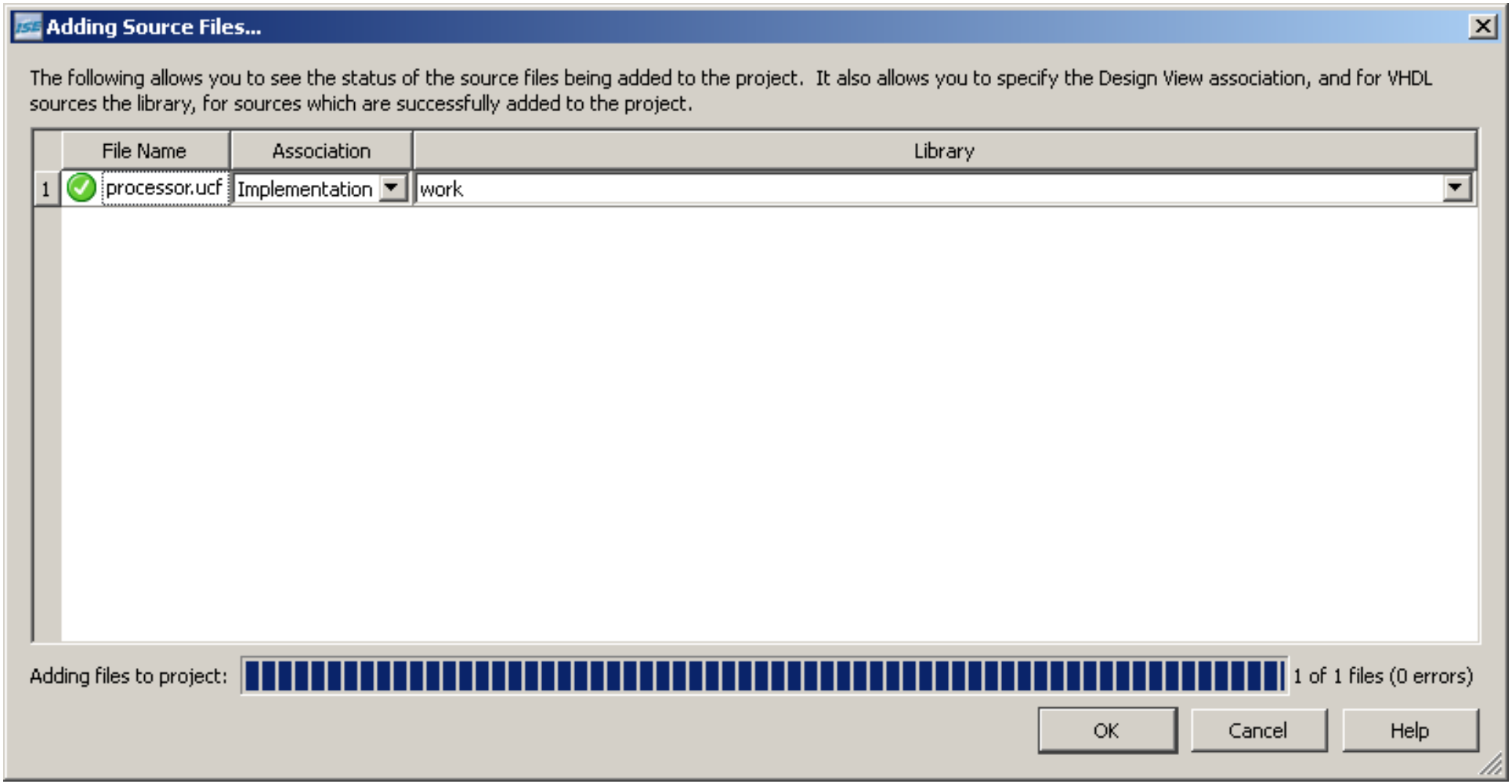
provide path to the private pcores (npi_dma, fx2, i2c_slave) then click OK



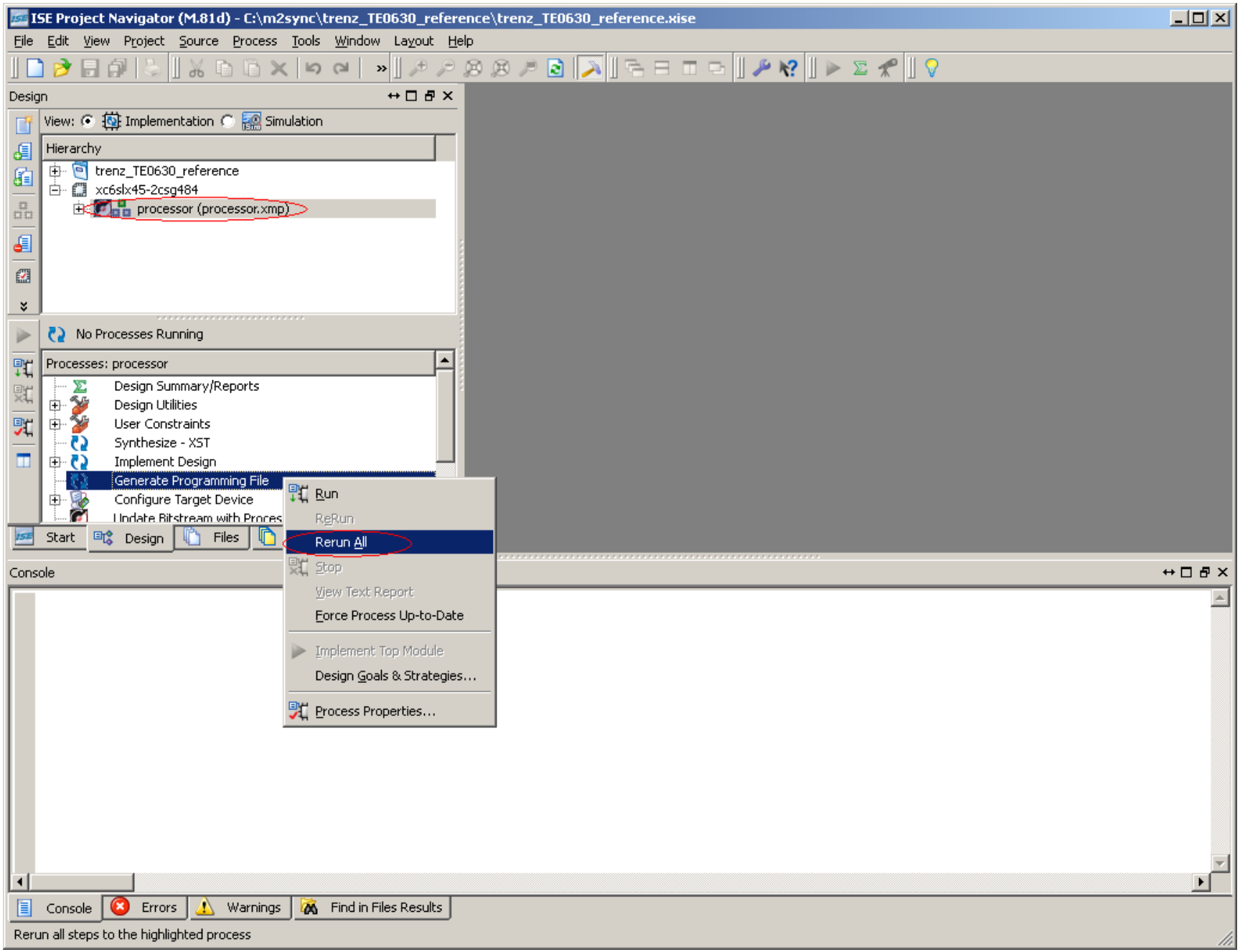
return to ISE Project Navigator and add Source



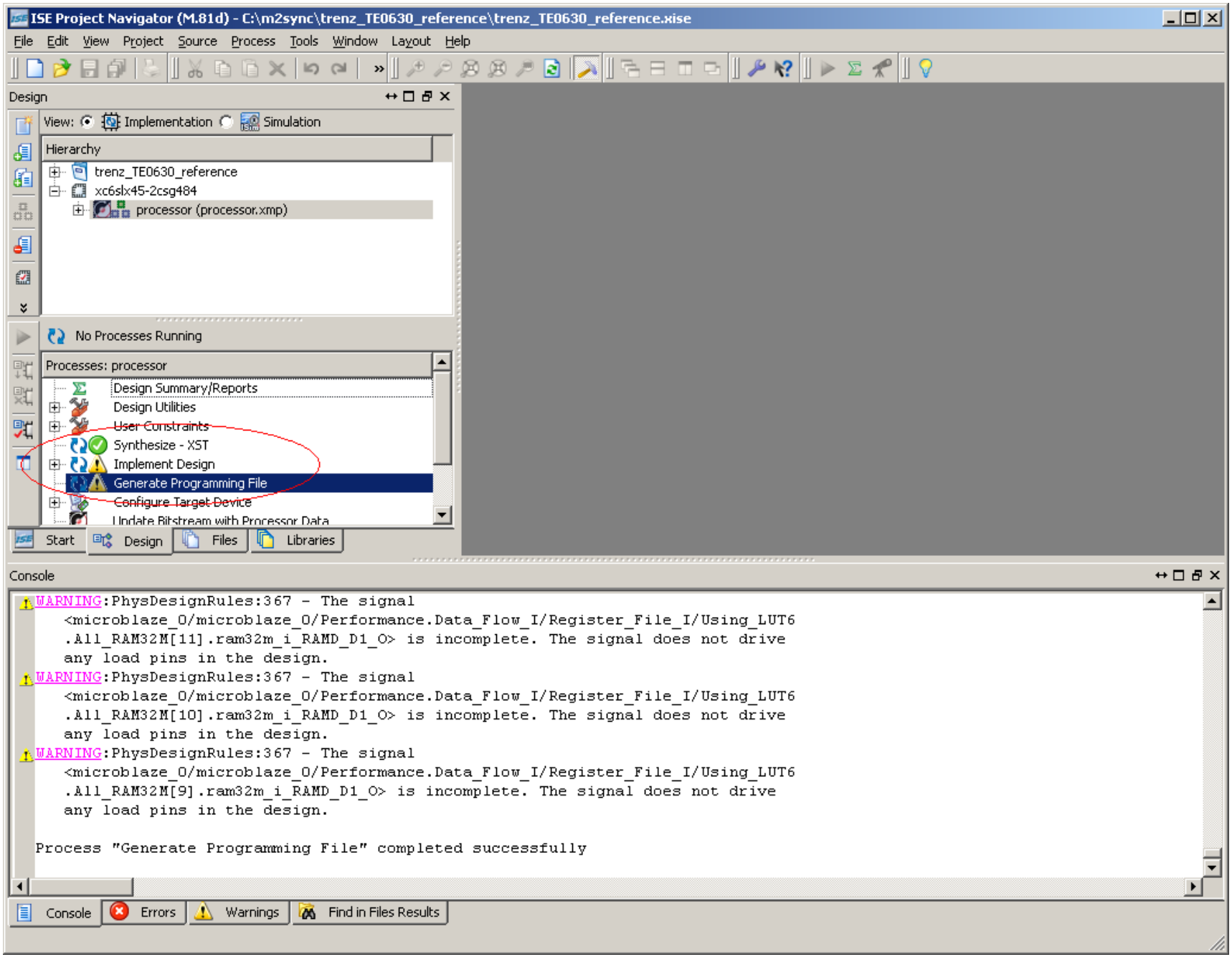
choose processor.ucf from processor/data/ subfolder then click Open



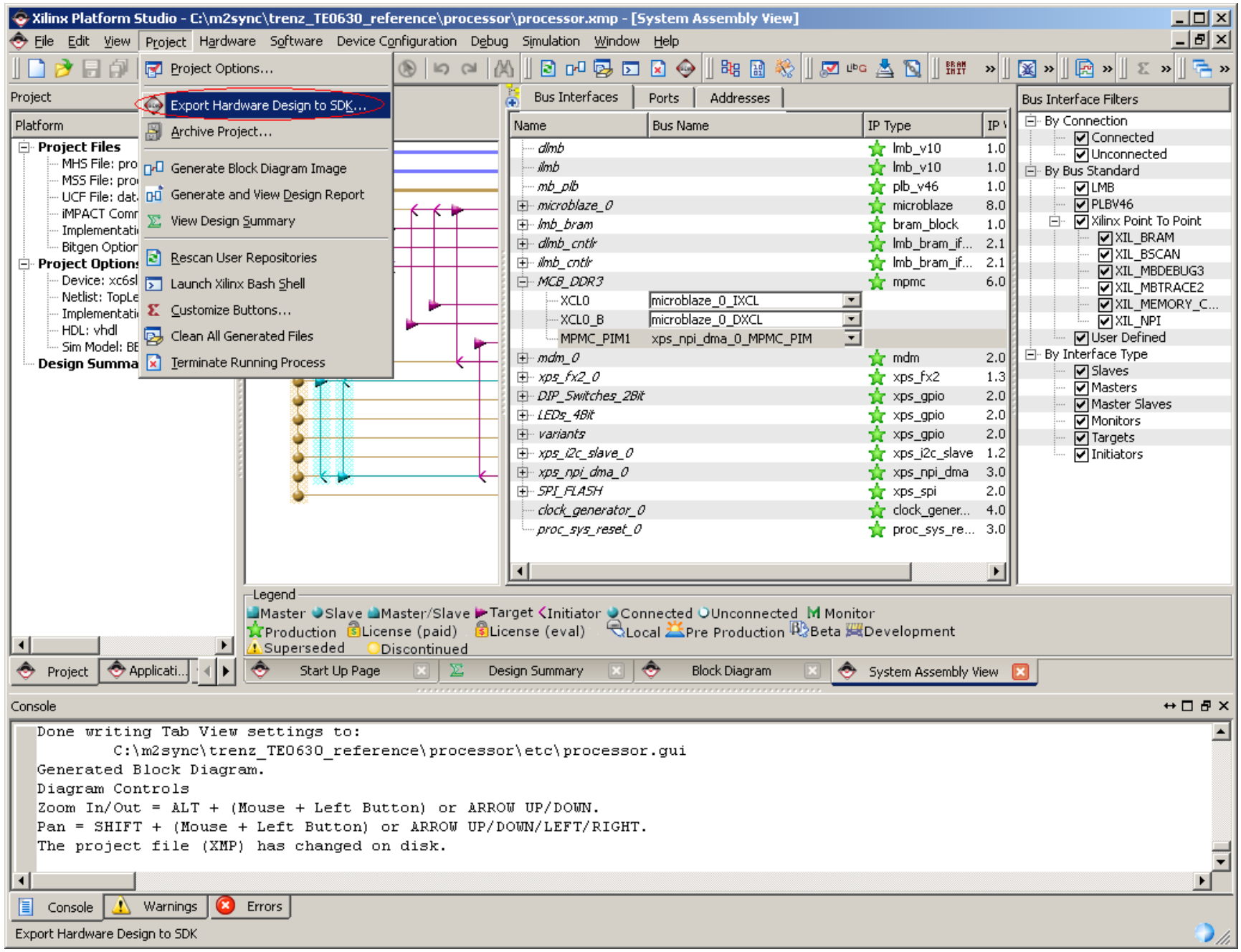
confirm adding Source File by clicking OK



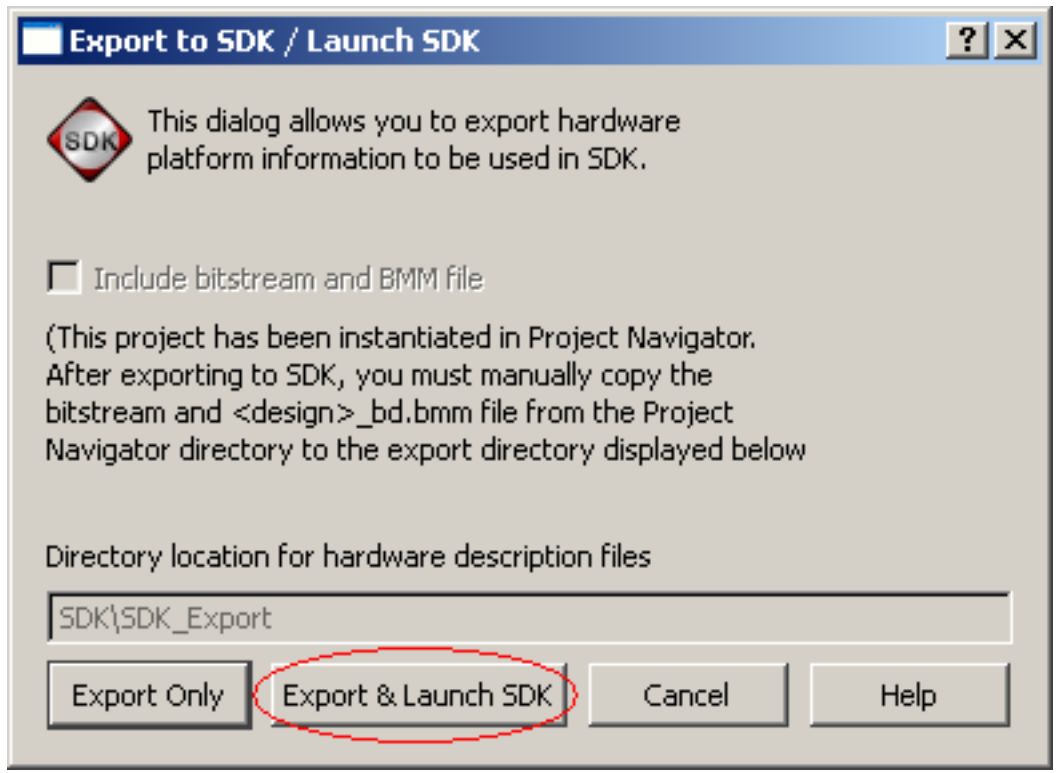
step on processor.xmp, choose Generate Programming File and click Rerun All



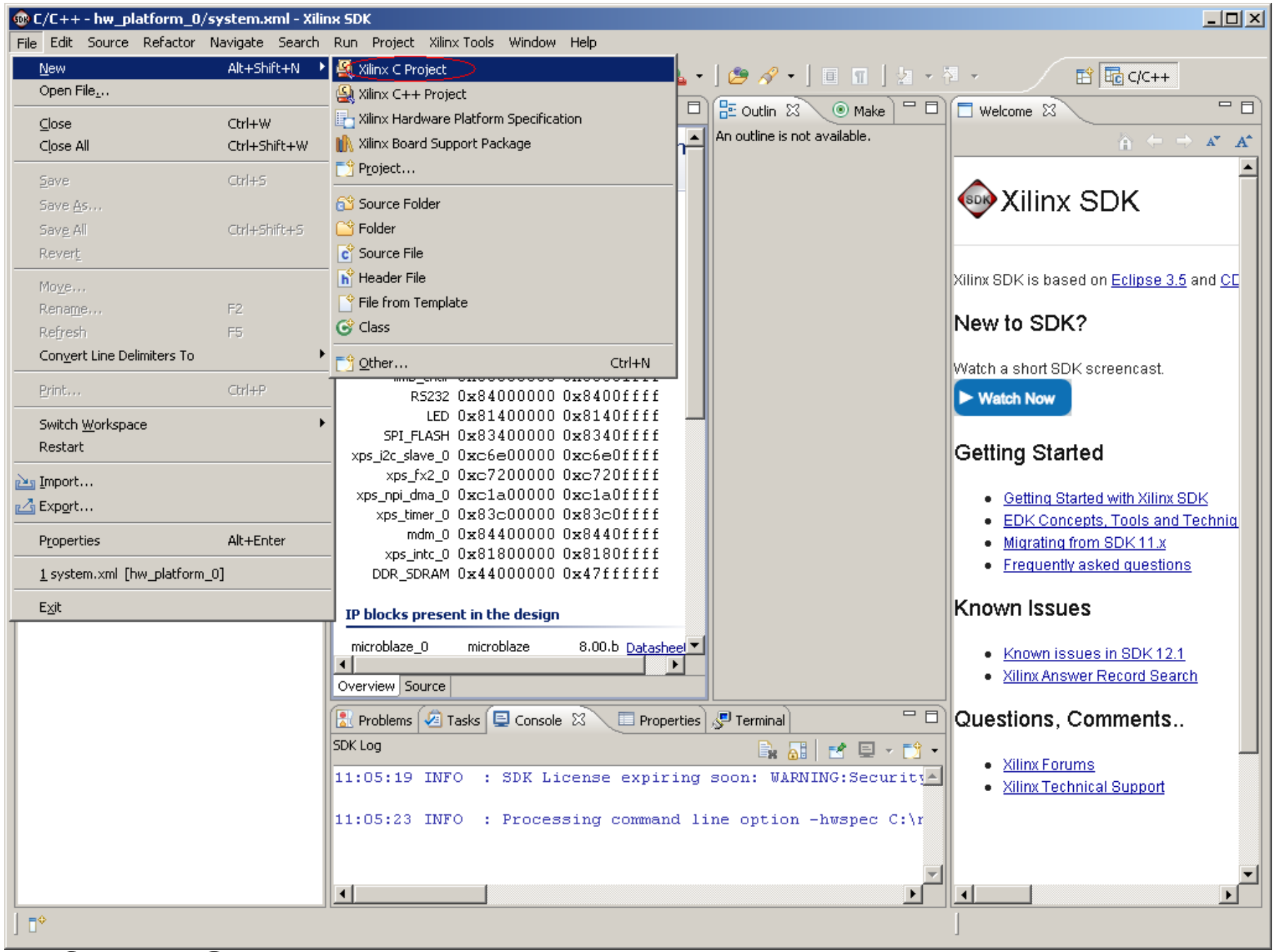
confirm generation success and return to Xilinx Platform Studio



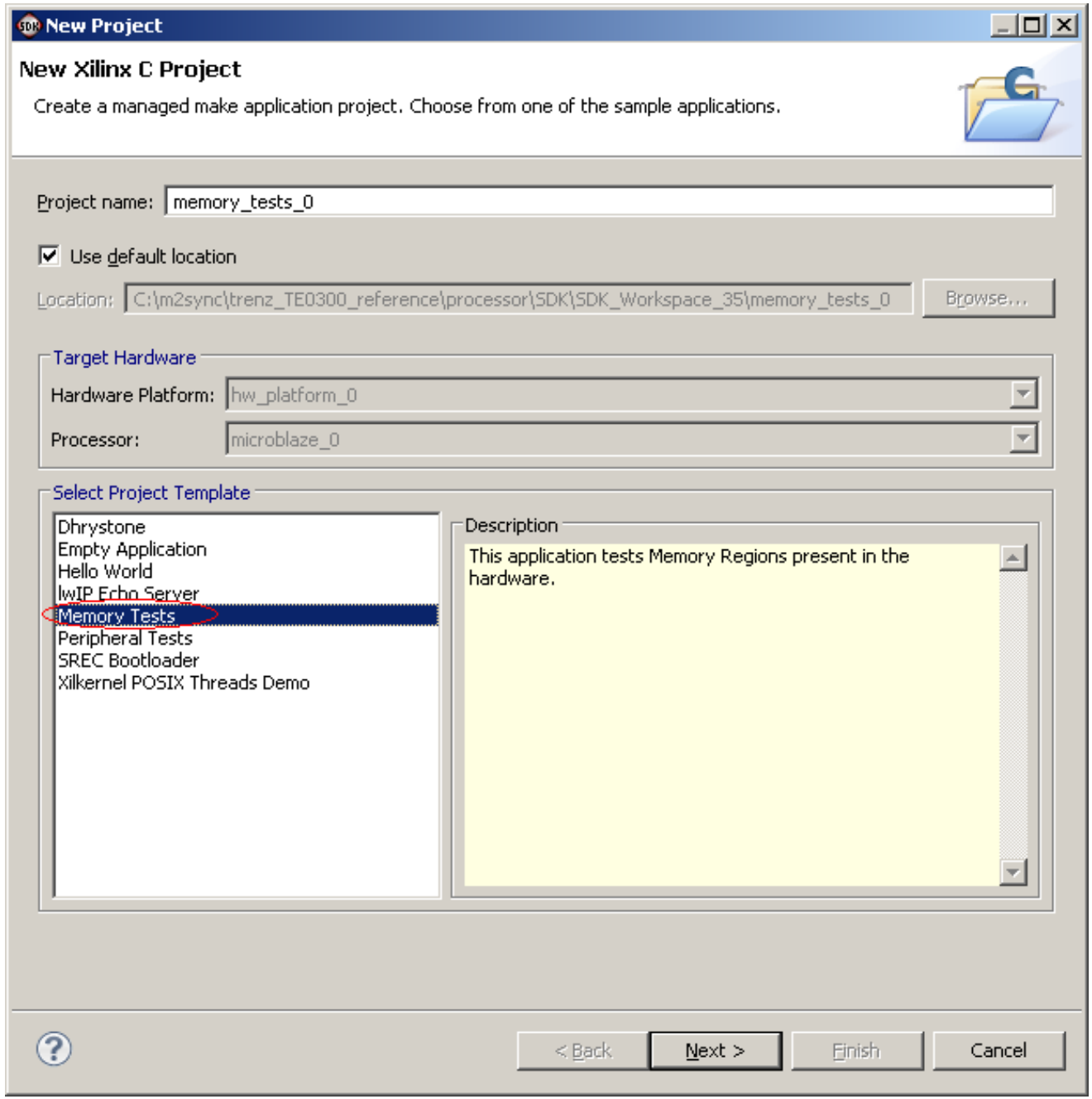
choose from menu Export Hardware Design to SDK



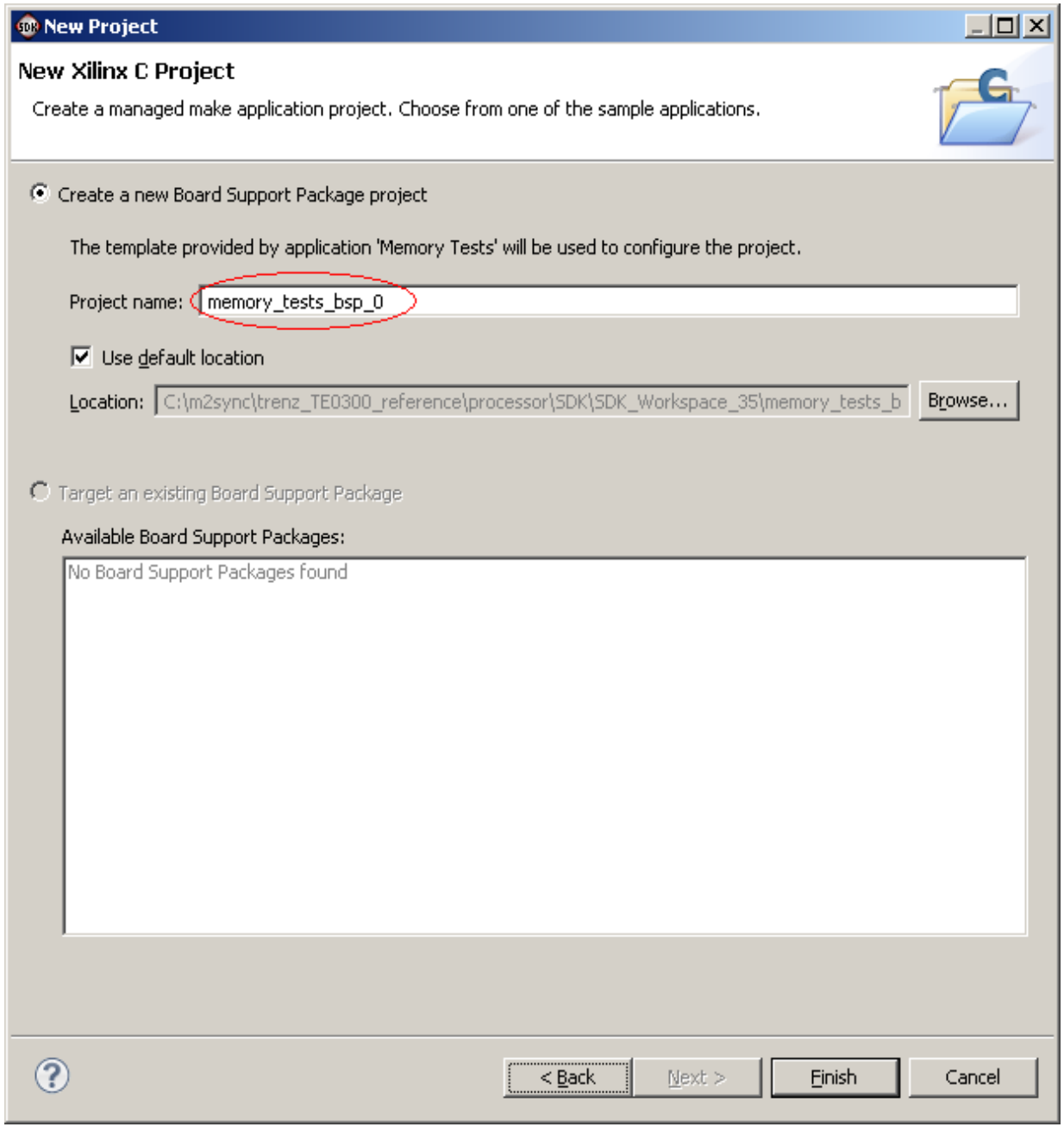
because Xilinx SDK isn't running yet, choose Export & Launch SDK button



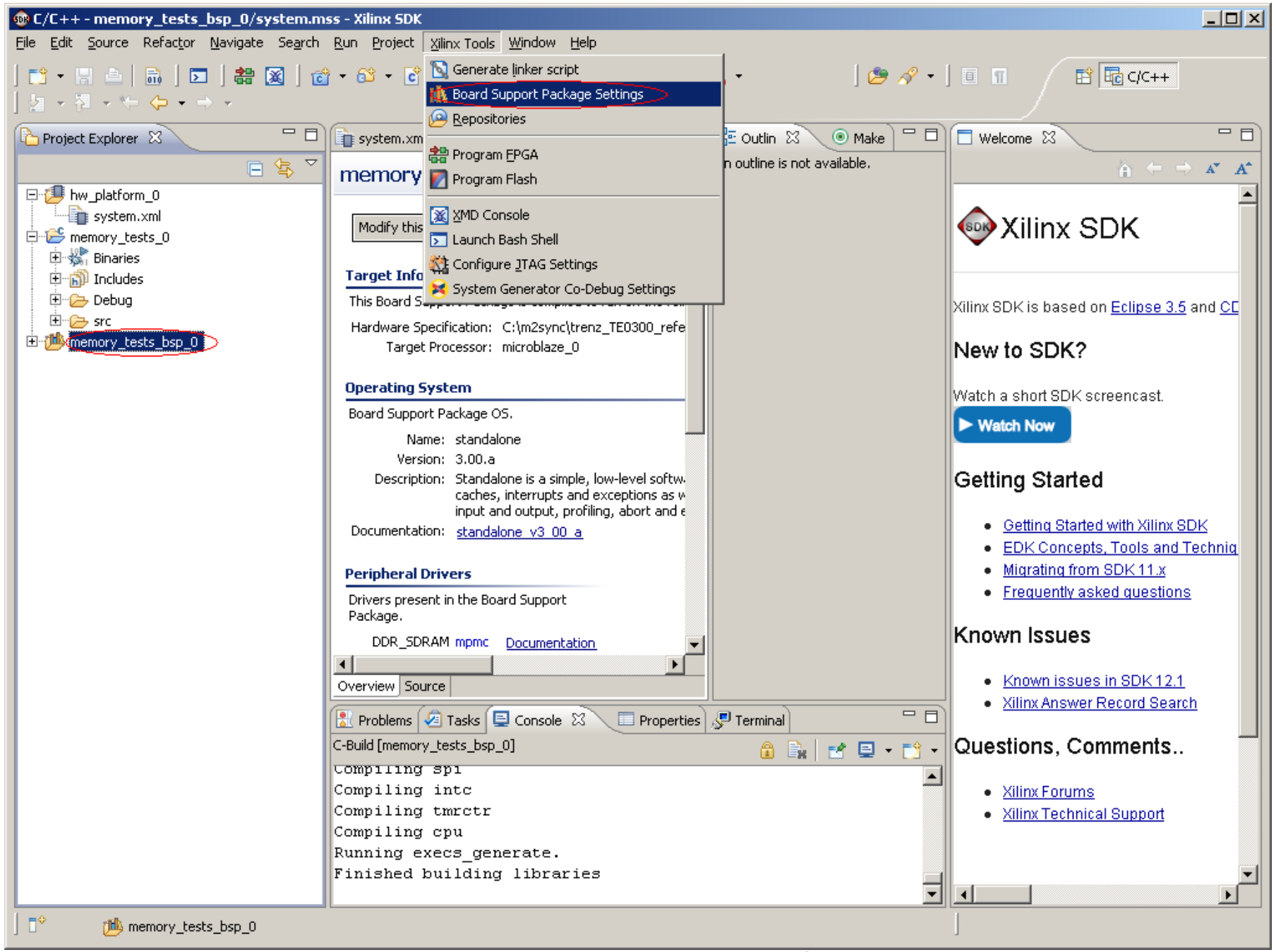
from SDK menu choose to create New Xilinx C Project



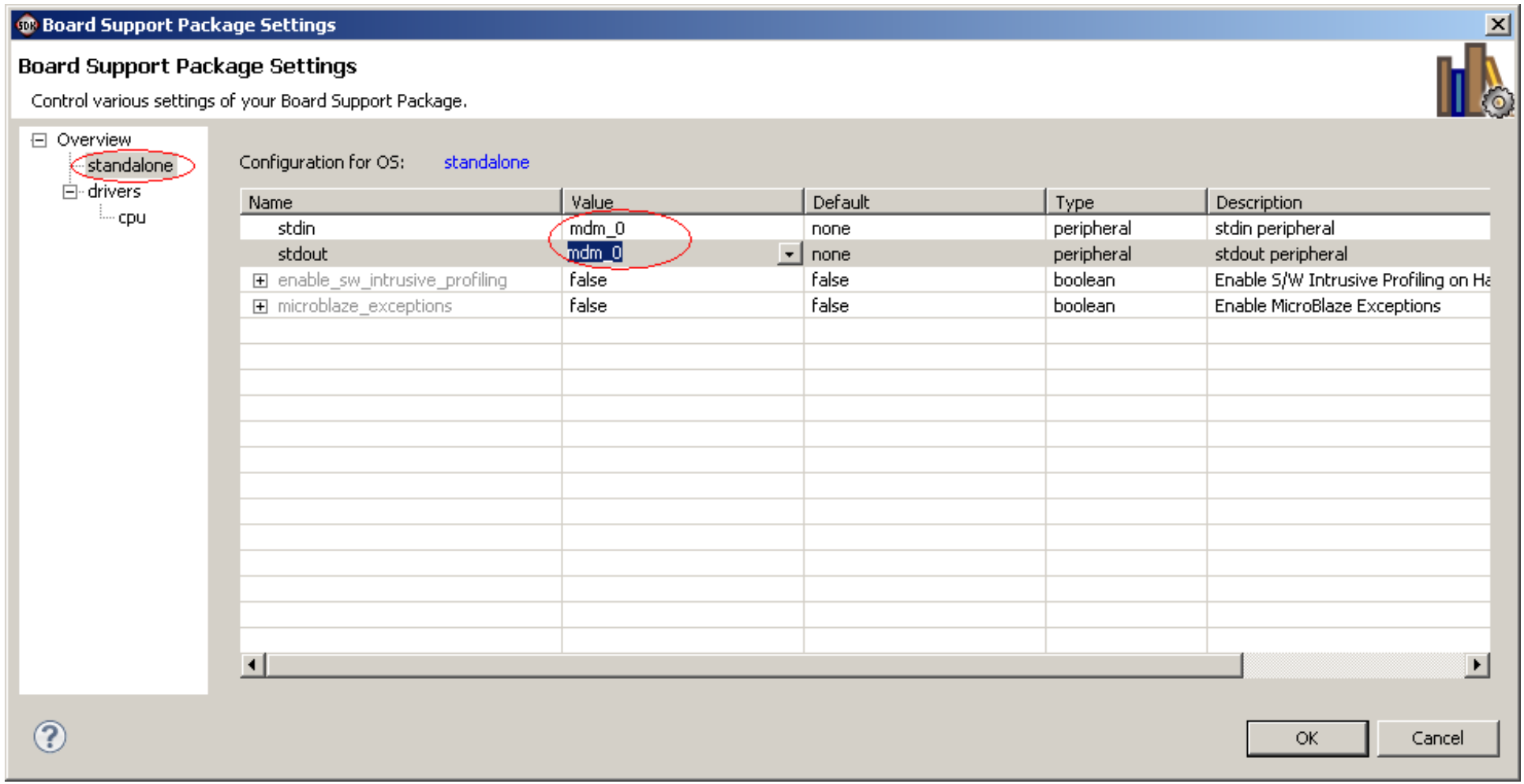
choose Memory Tests template and click Next



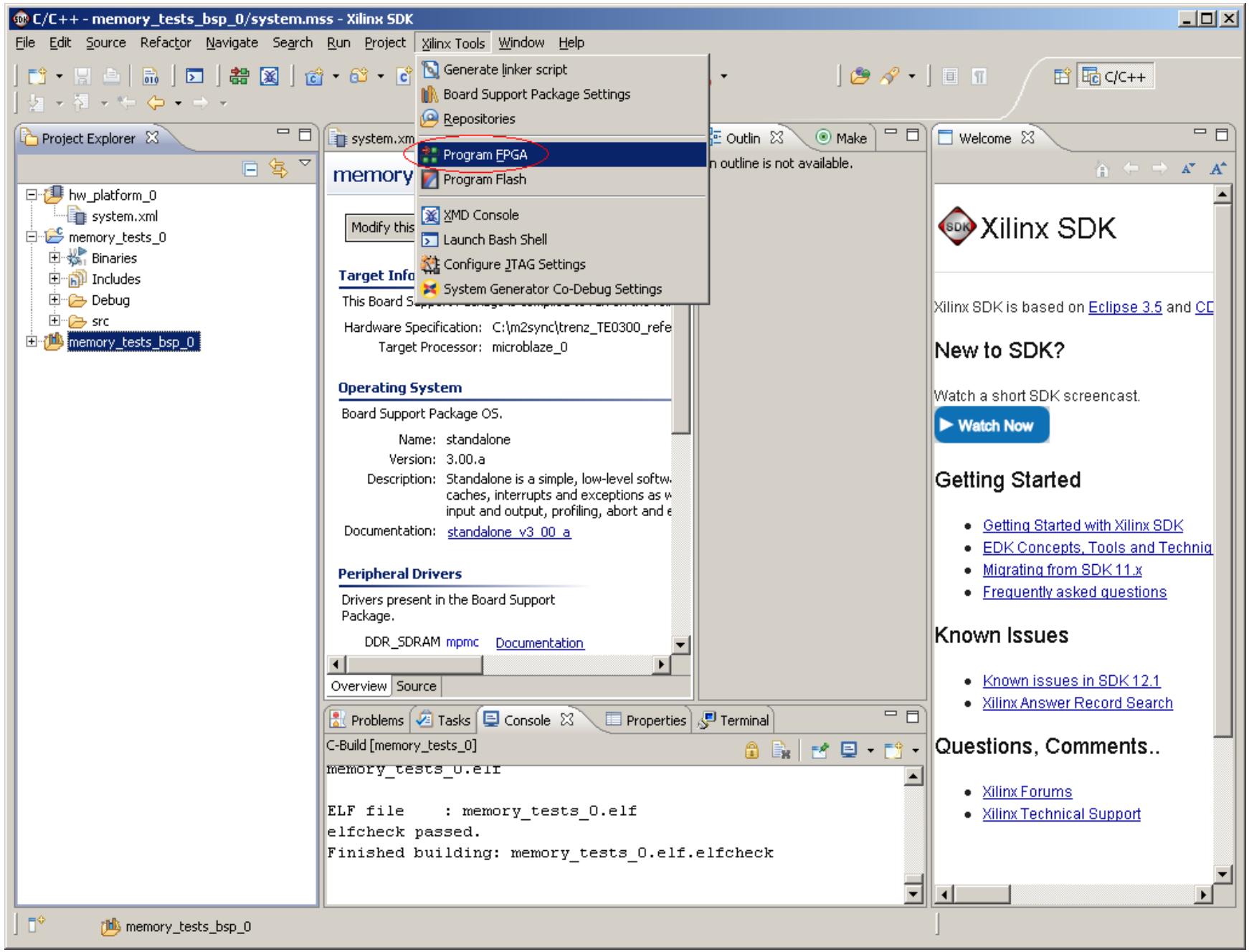
keep default BSP project name memory_tests_bsp_0 and click Finish



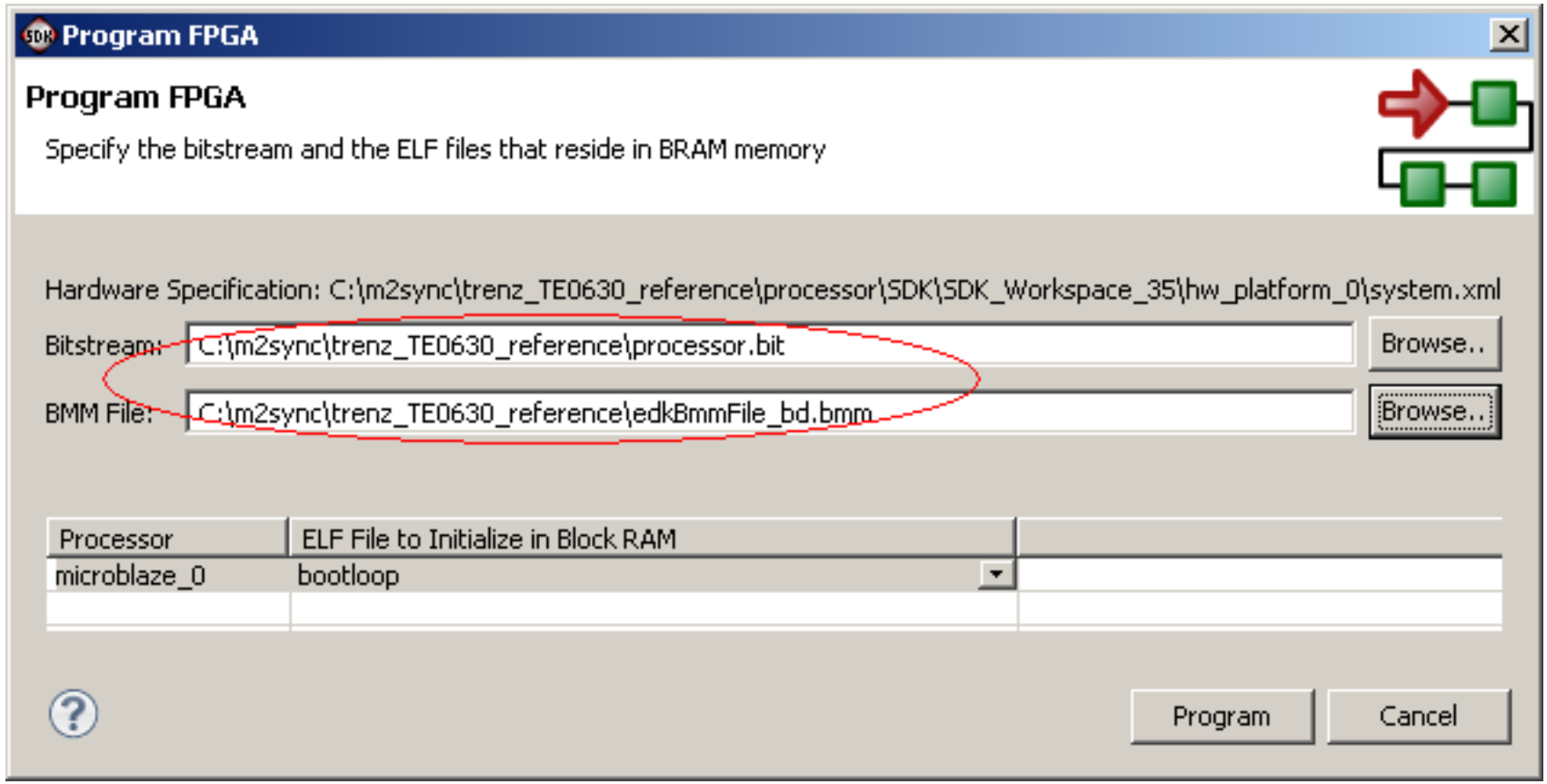
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



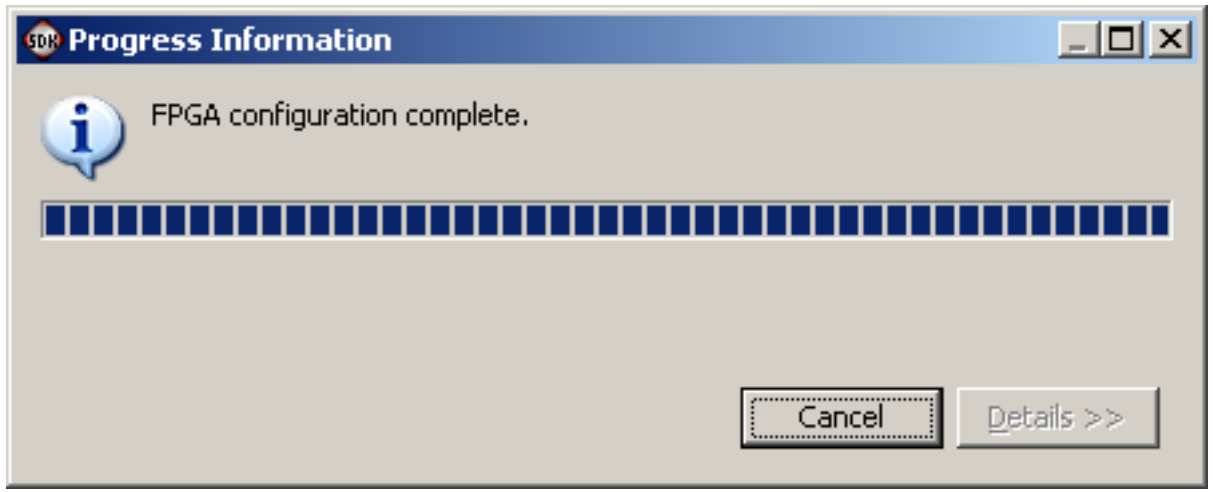
from standalone section apply mdm_0 to stdin and stdout then click OK



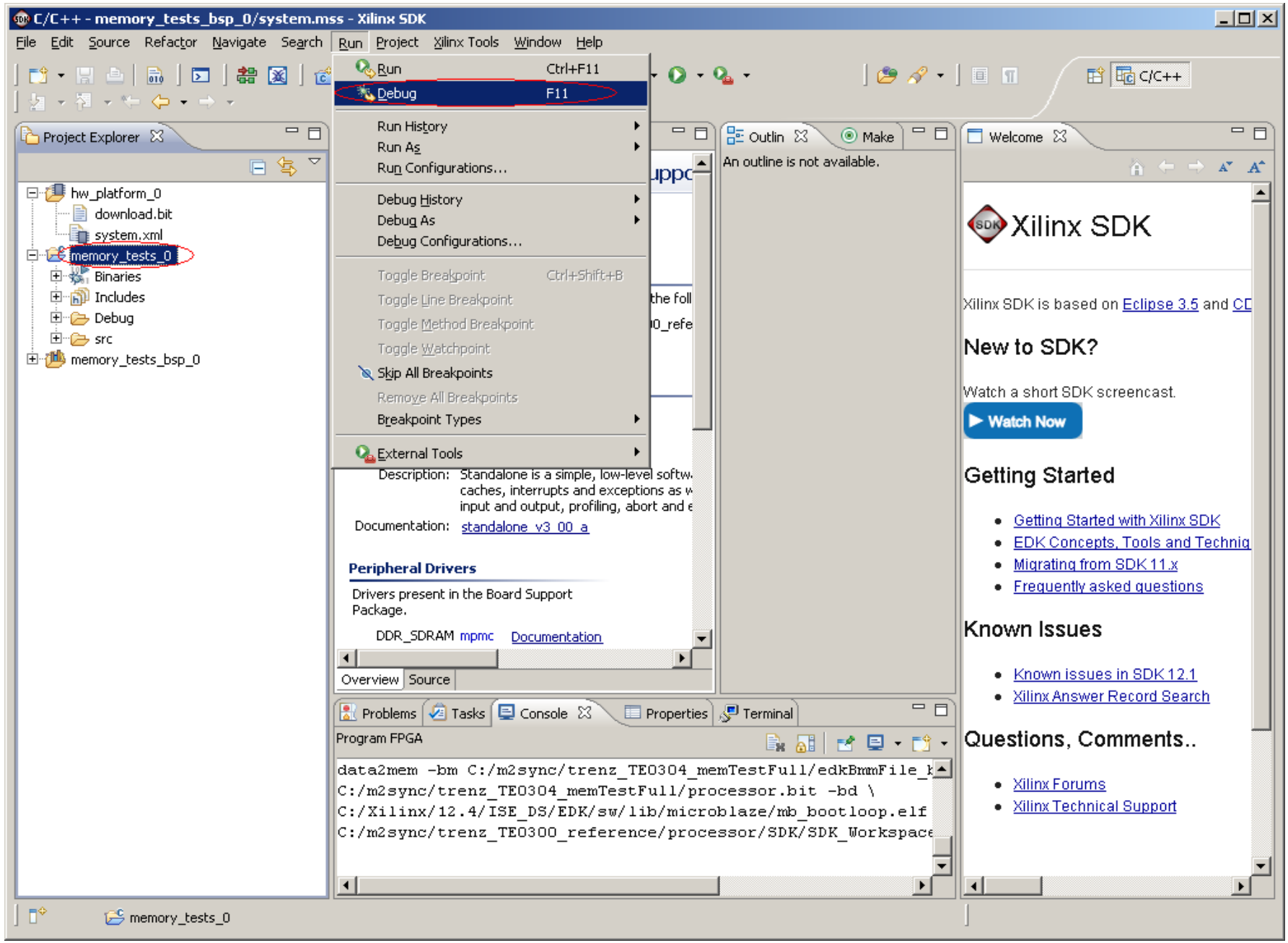
connect the prototype board TE0300 and choose Program FPGA from menu



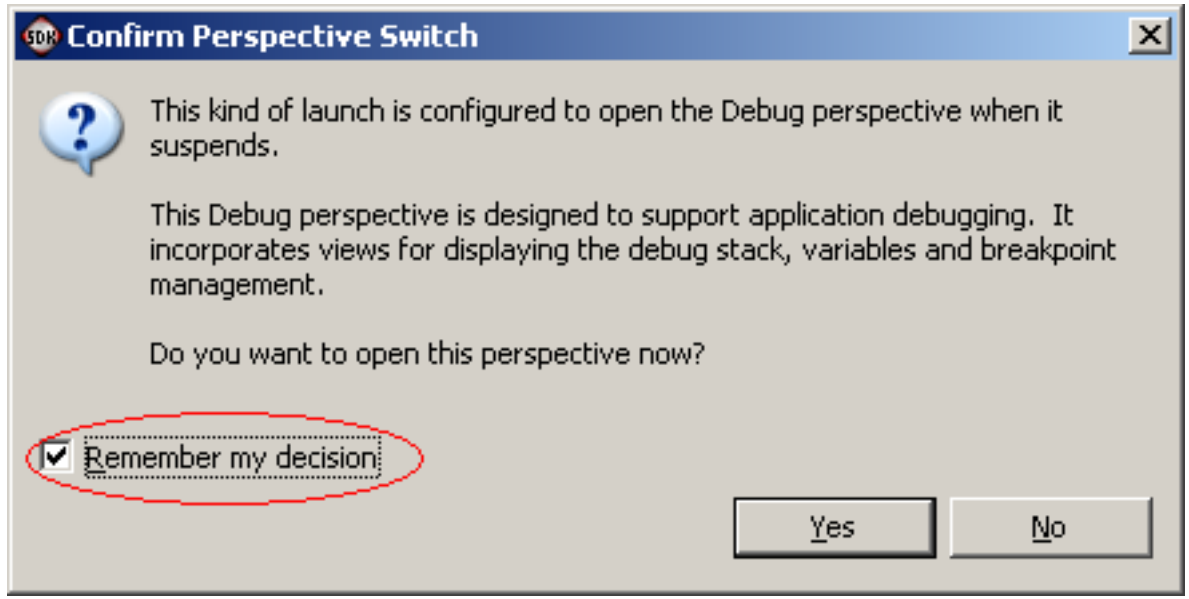
provide correct Bistream and BMM files then click Program



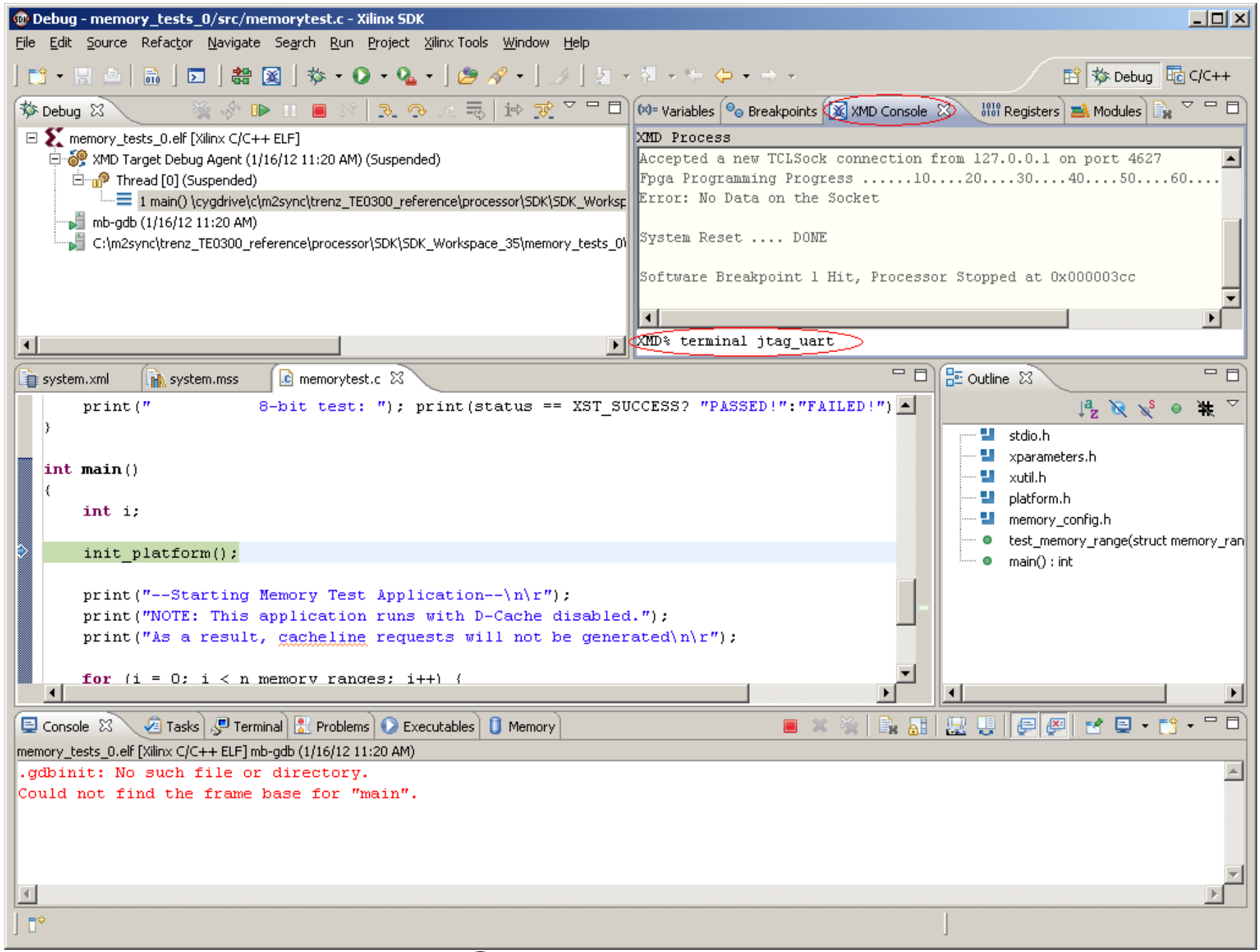
wait for FPGA programming completion



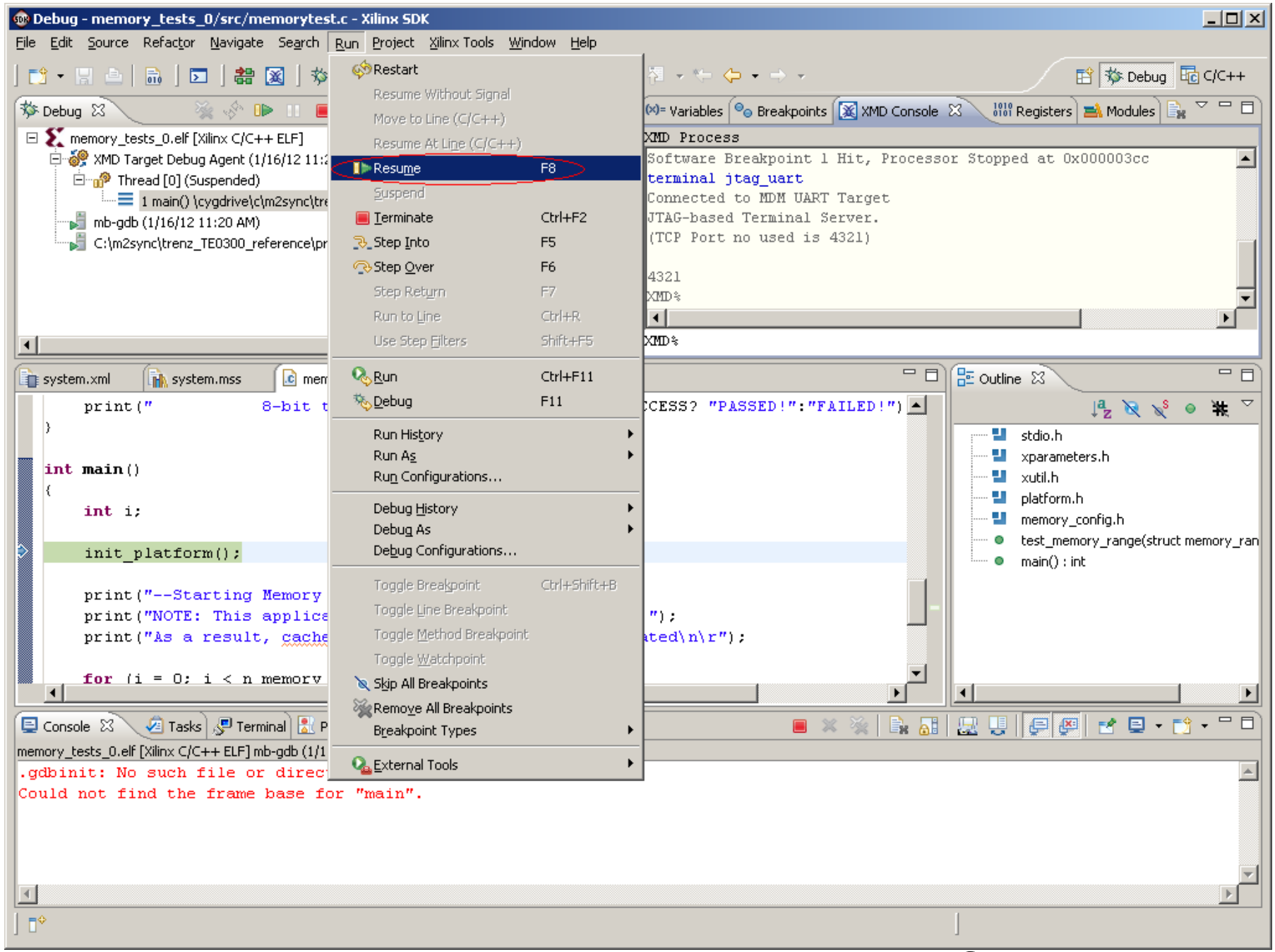
step on memory_tests_0 application and choose Debug menu



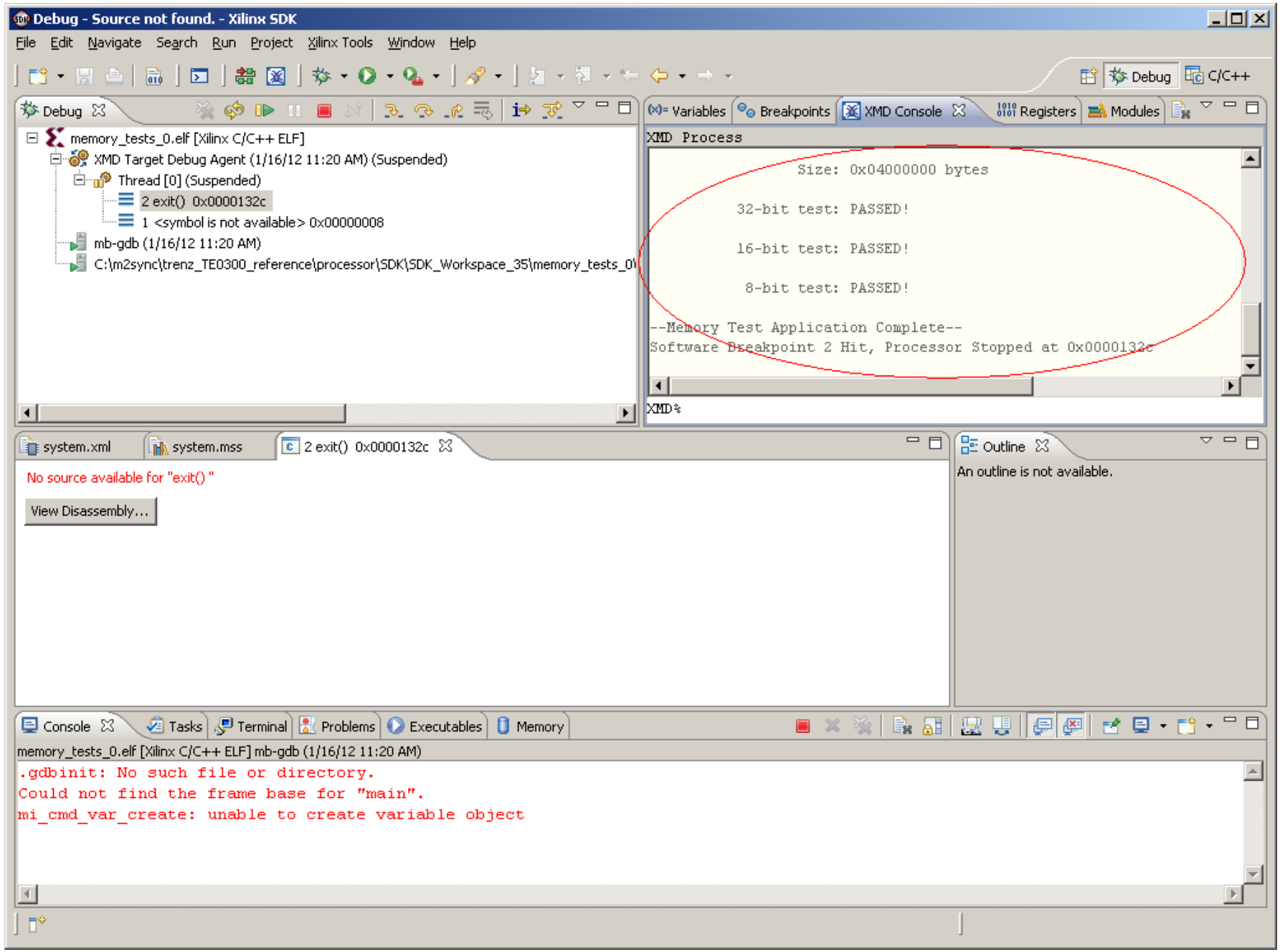
choose remember decision and confirm switching to Debug design by clicking Yes button



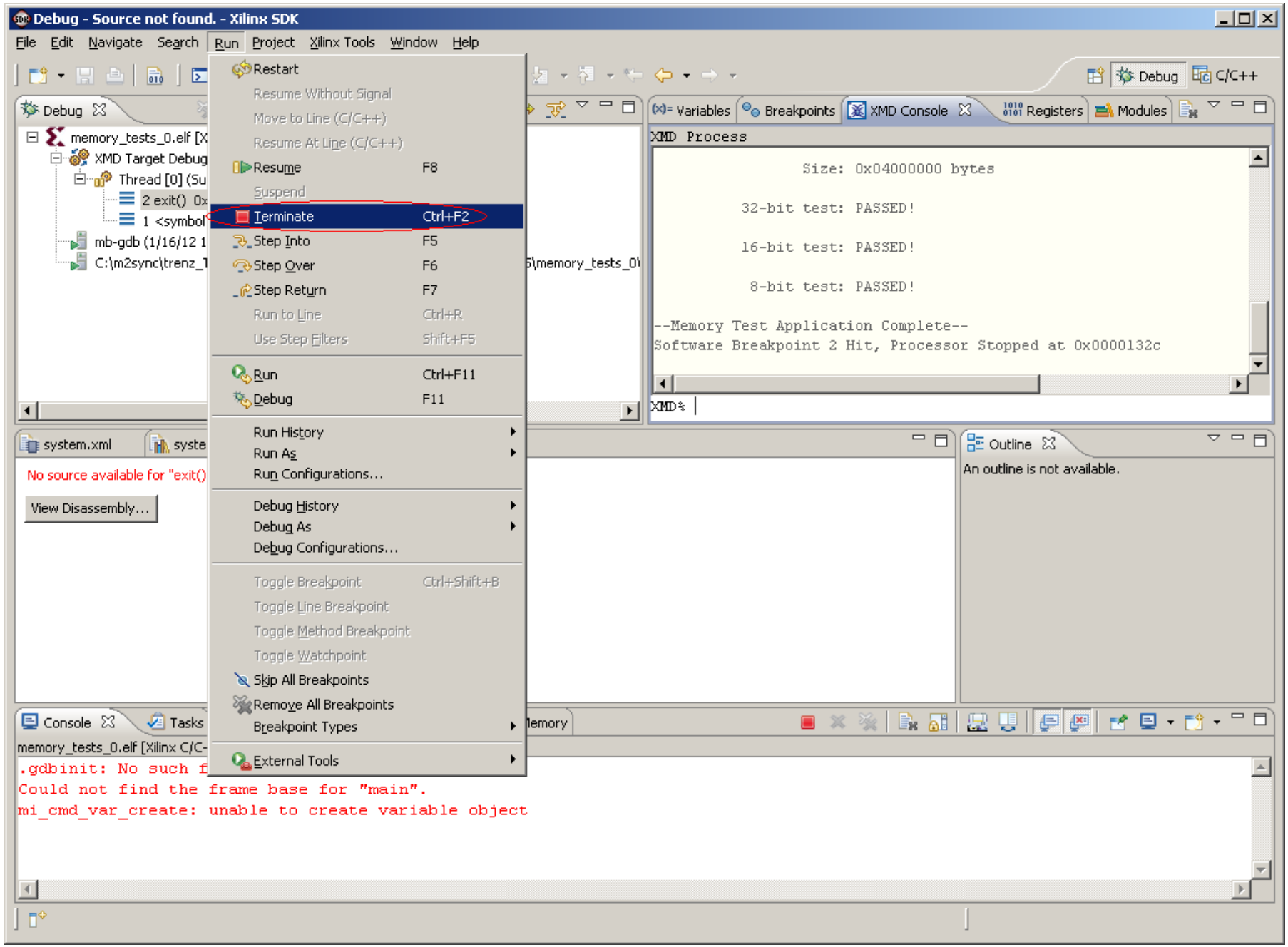
switch to XMD Console tab and type command "terminal jtag_uart"



resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application

TE0630 board configuration complete

external memory configuration confirmed with test application