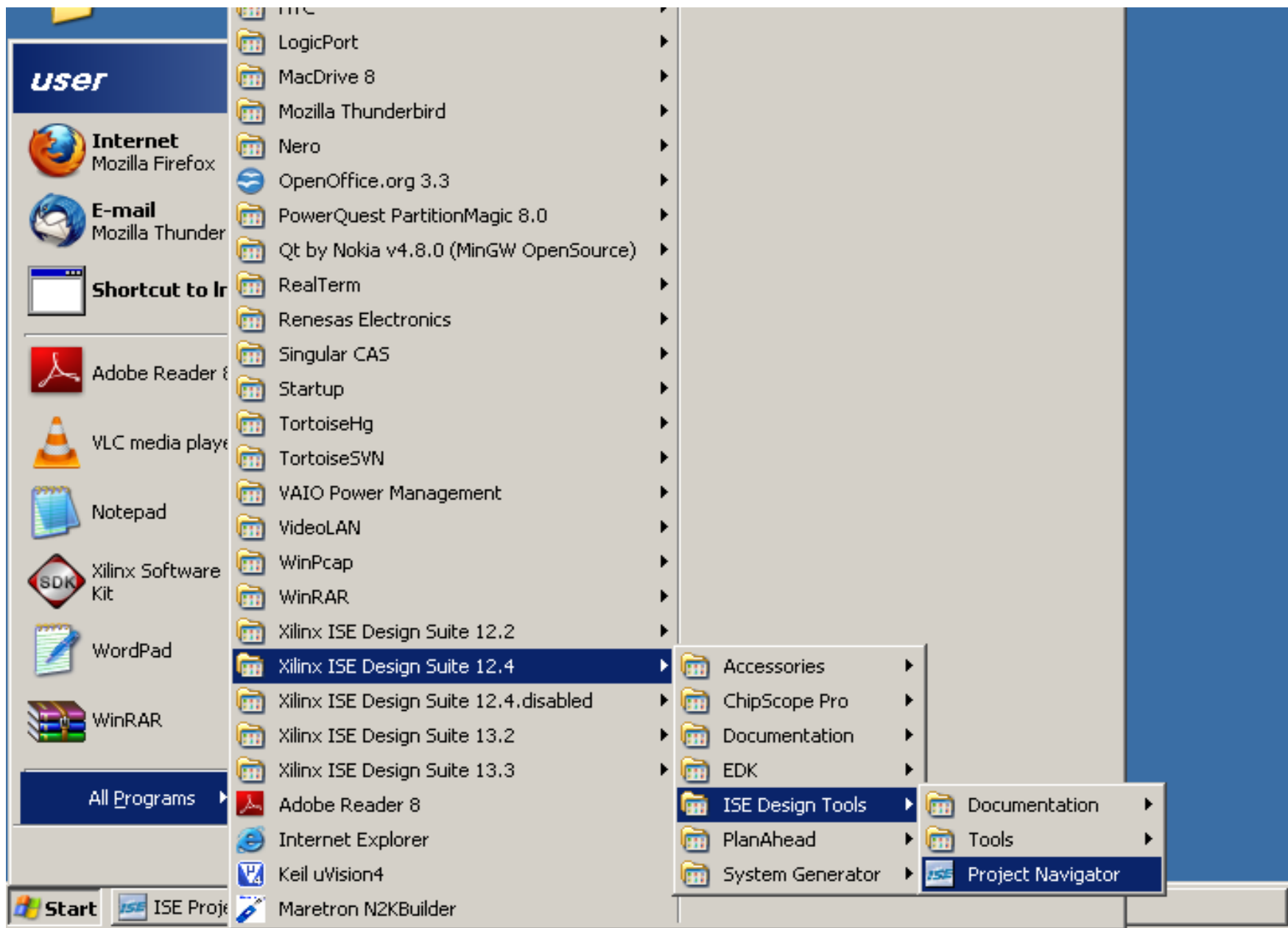
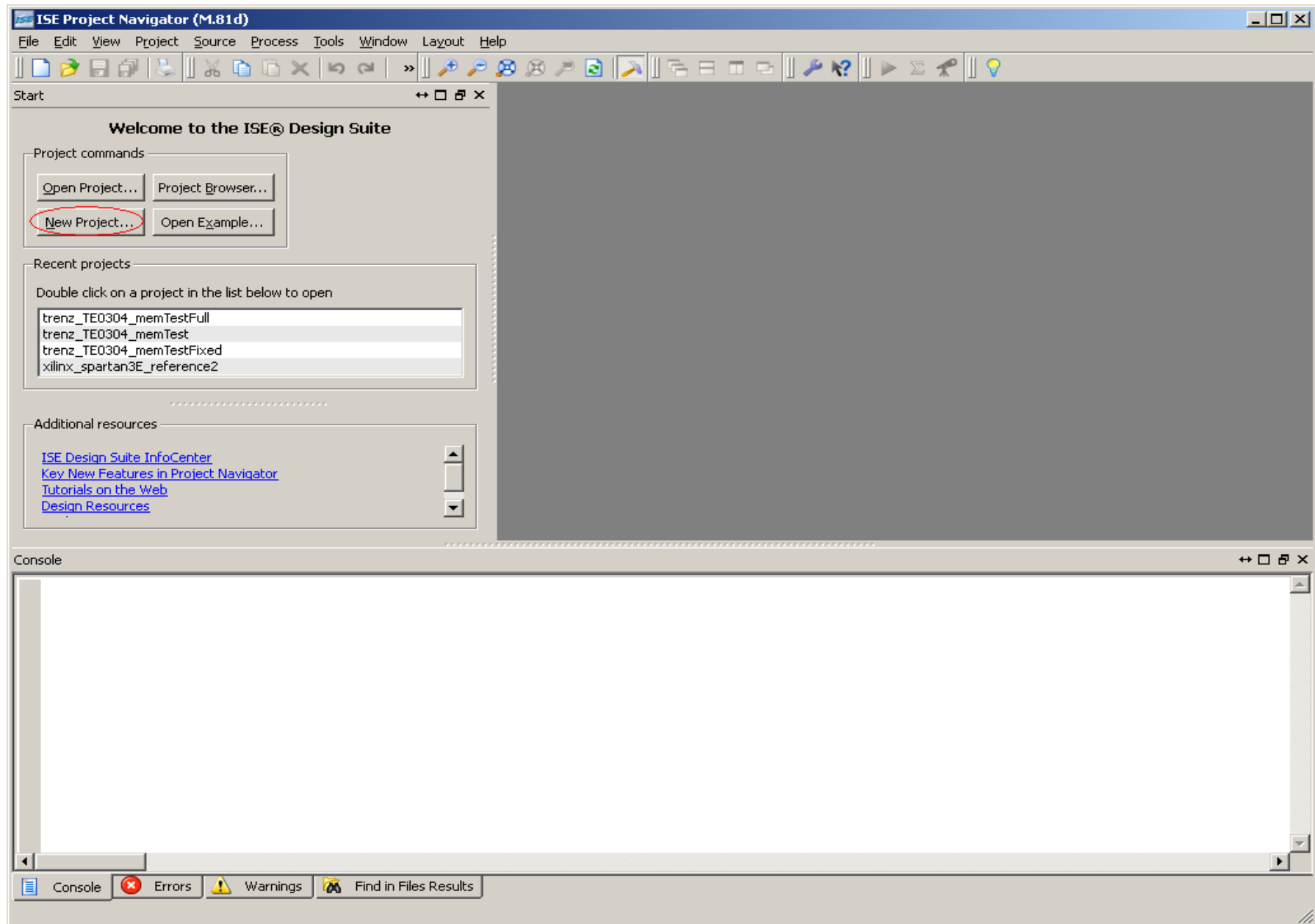


TE0630 platform

reference project creation sequence



start Xilinx ISE Project Navigator



click button to create a new project

New Project Wizard [X]

Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name:

Location: ...

Working Directory: ...

Description:

Select the type of top-level source for the project

Top-level source type:

[More Info](#) [Next >](#) [Cancel](#)

choose project name, then click Next

New Project Wizard

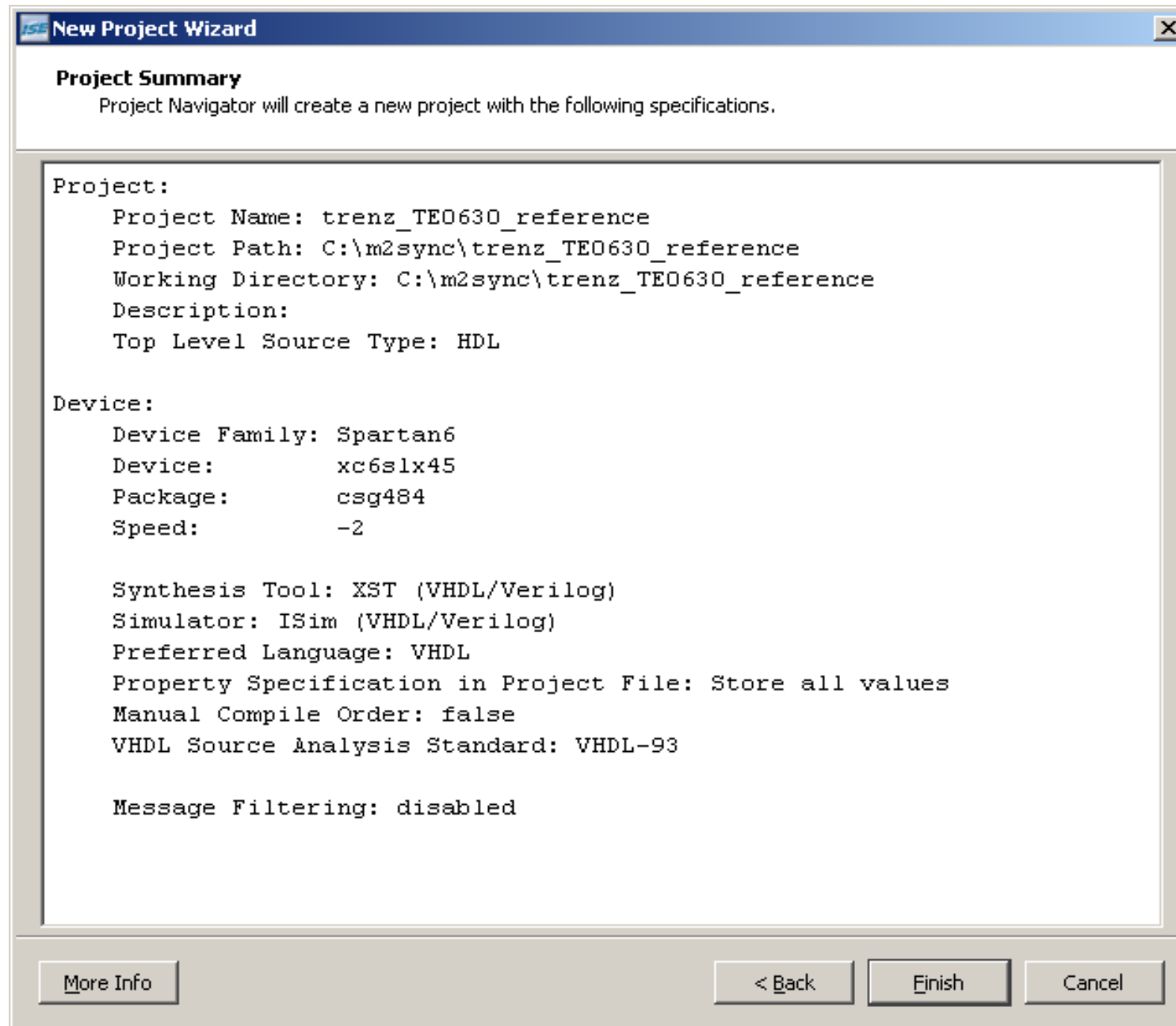
Project Settings
Specify device and project properties.

Select the device and design flow for the project

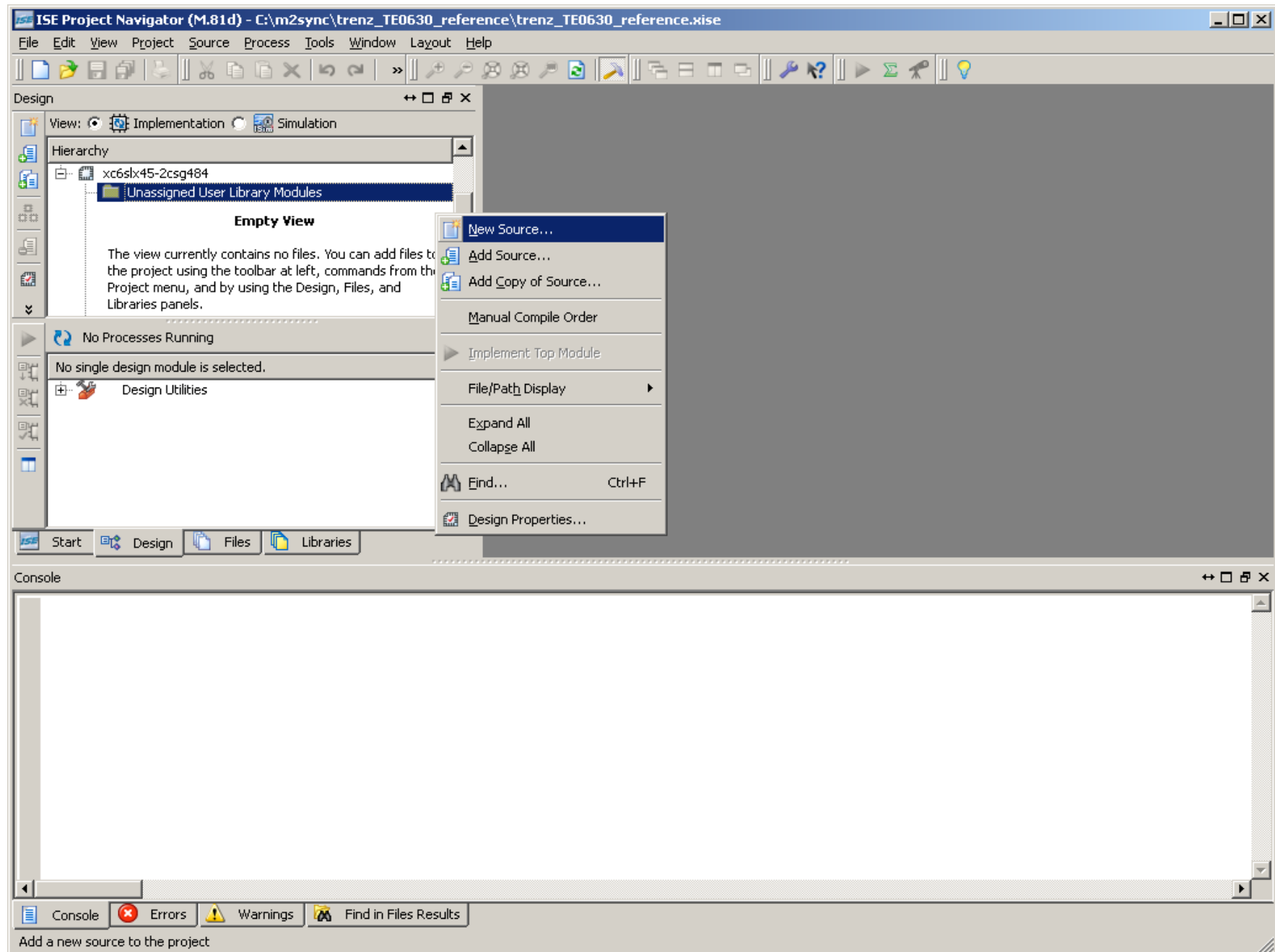
Property Name	Value
Product Category	All
Family	Spartan6
Device	XC6SLX45
Package	CSG484
Speed	-2
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

[More Info](#) [< Back](#) [Next >](#) [Cancel](#)

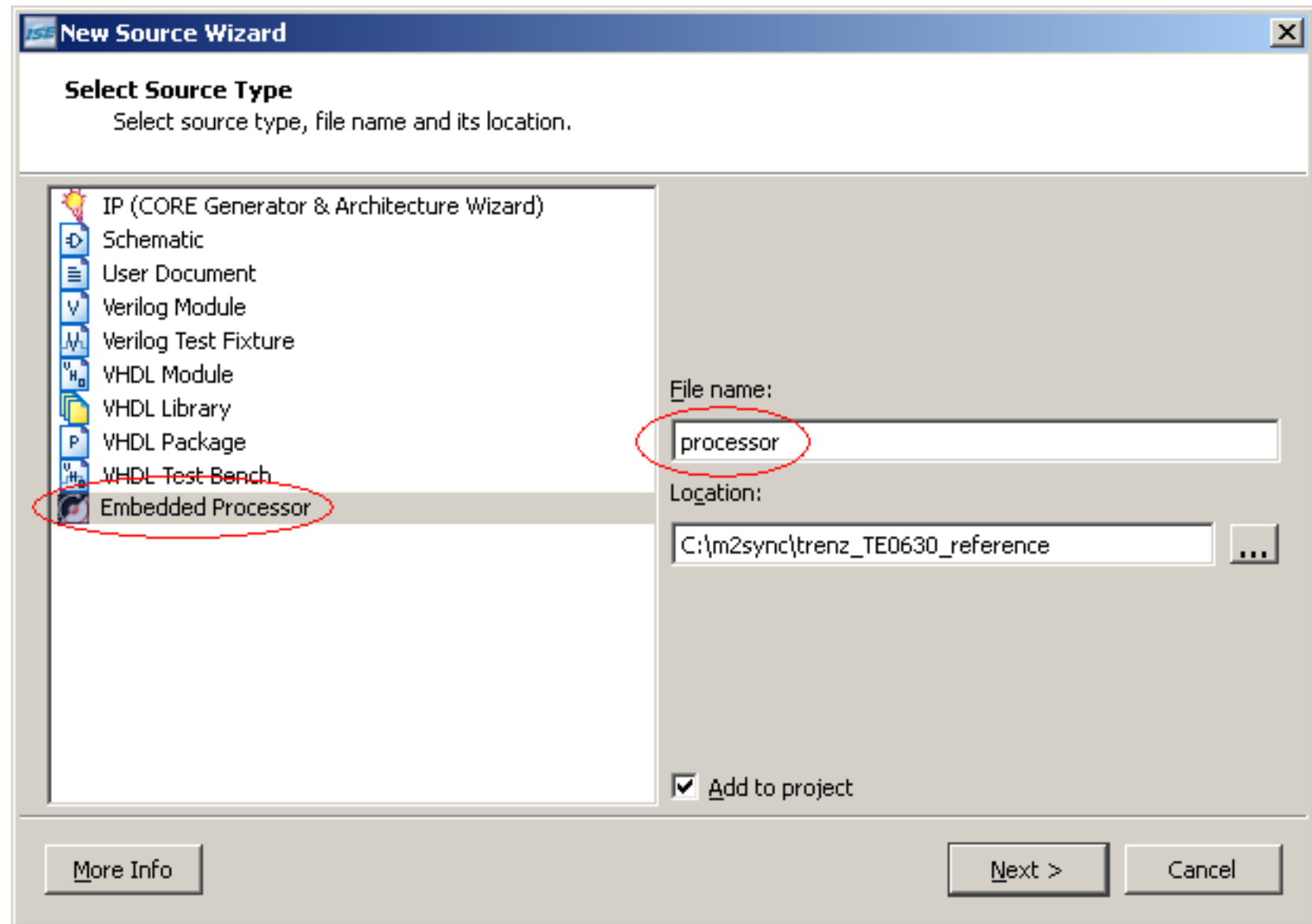
provide correct Family, Device, Package and Speed,
then click Next



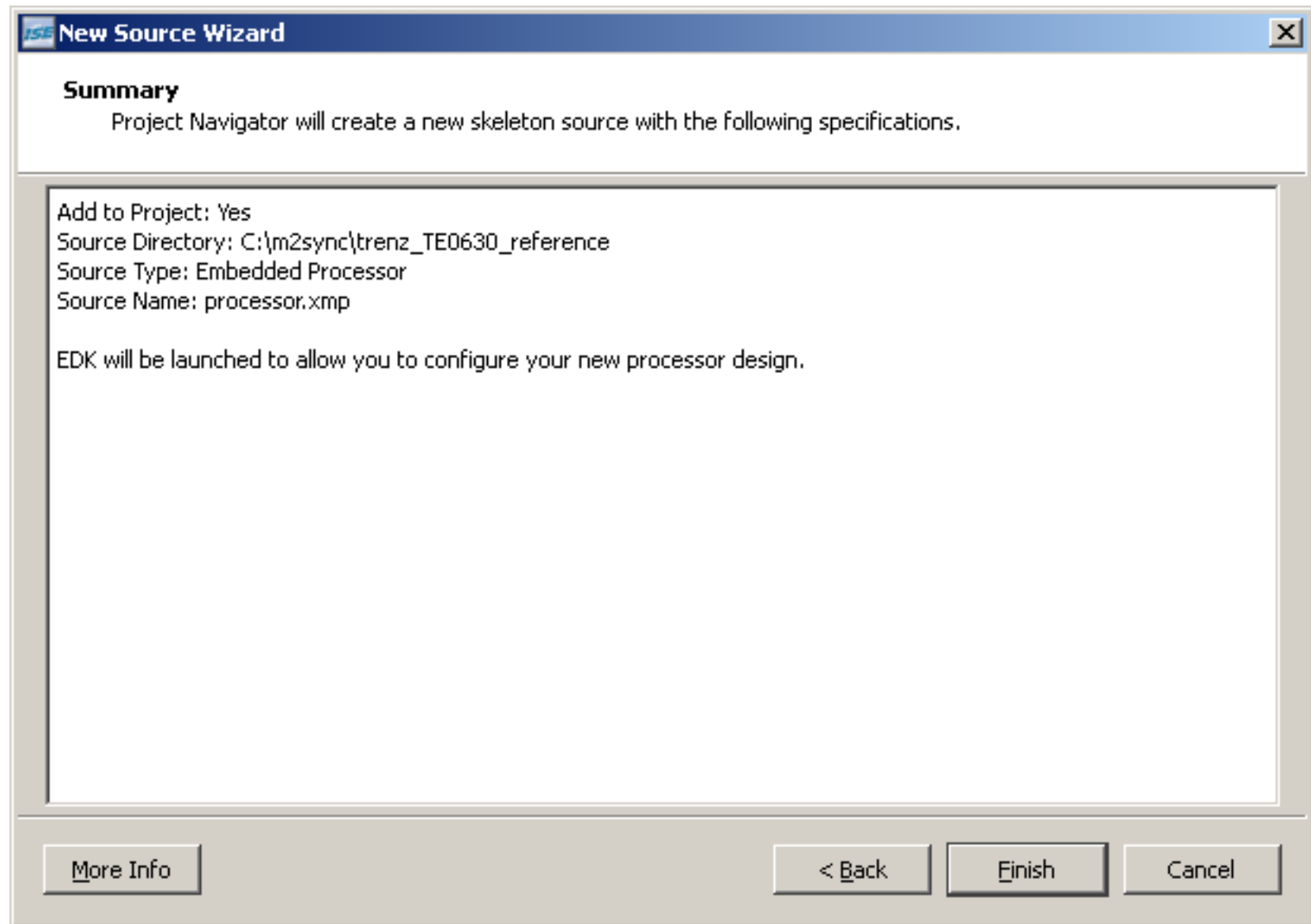
verify configuration and click Finish



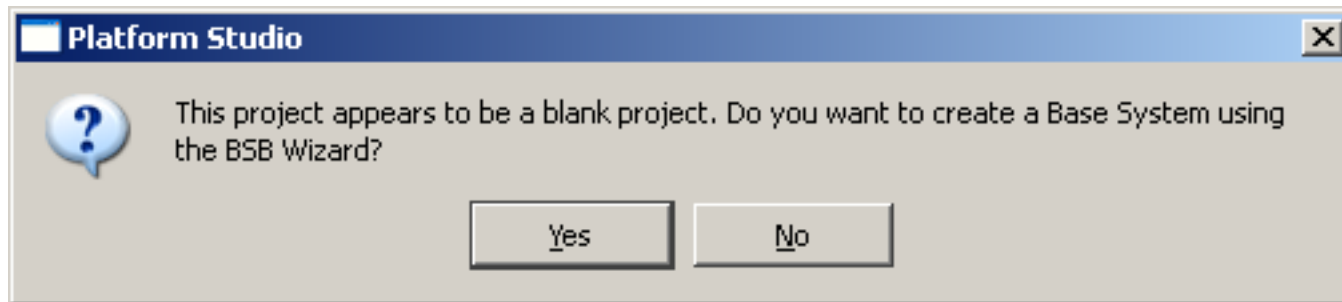
right button menu to add New Source



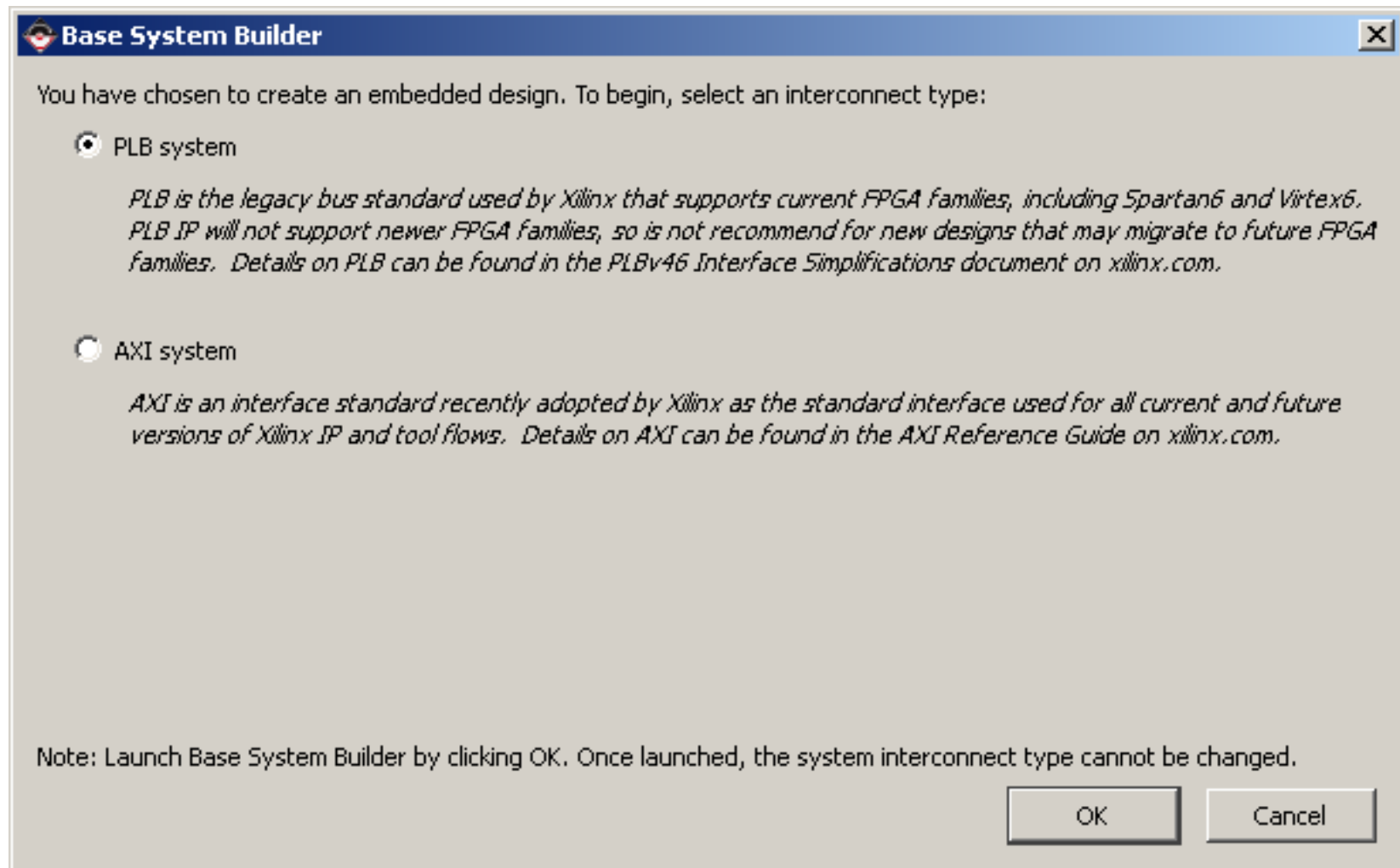
choose Embedded Processor, provide File name
then click Next



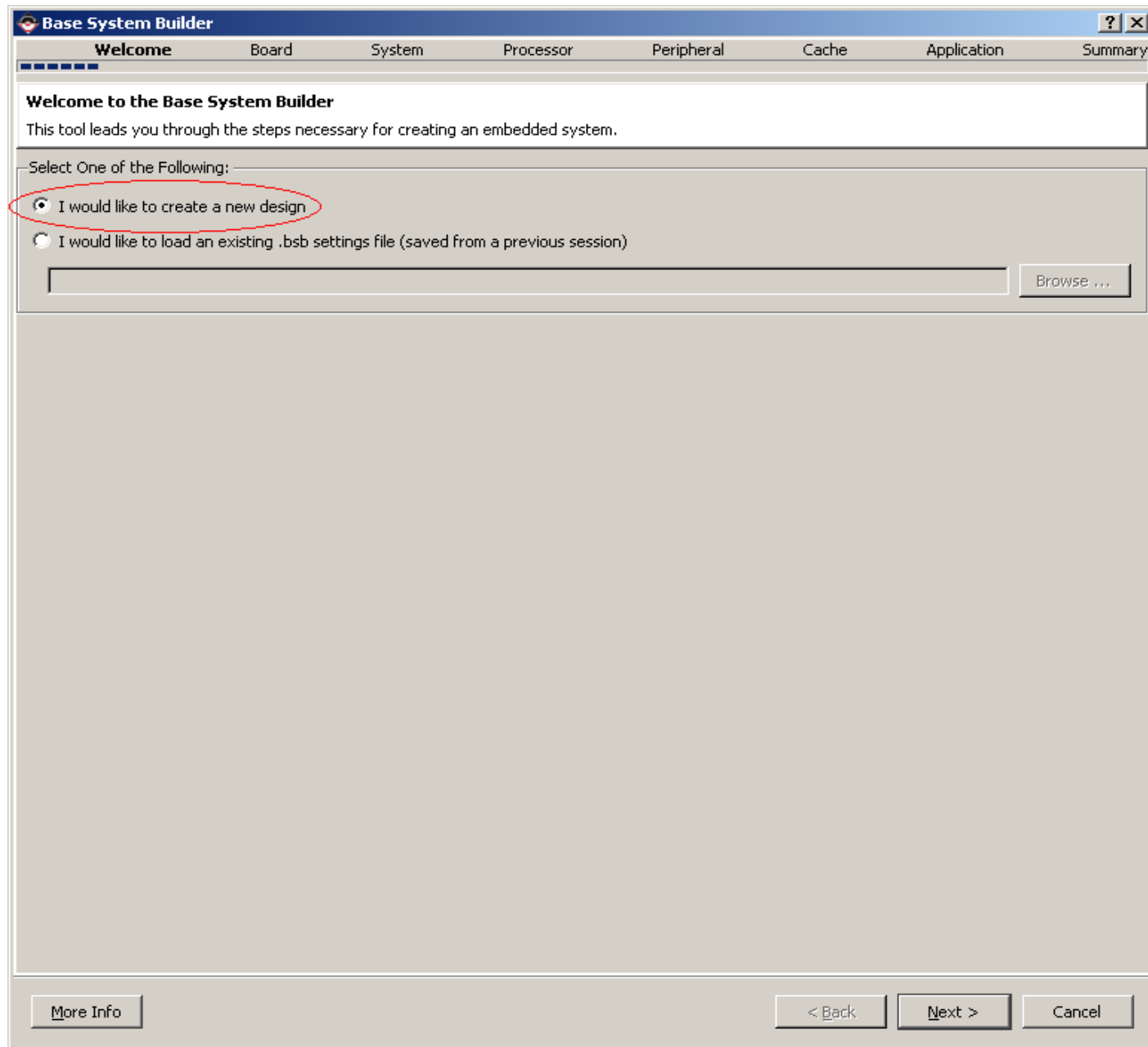
verify configuration then click Finish



confirm Yes to launch BSB Wizard



choose PLB system



choose create new design then click Next

Base System Builder

Welcome **Board** System Processor Peripheral Cache Application Summary

Board Selection

Select a target development board.

Board

☒ I would like to create a system for the following development board

Board Vendor: Trenz

Board Name: Micromodule Spartan-6 XC6SLX45-2CSG484C

Board Revision: 0

☐ I would like to create a system for a custom board

Board Information

Architecture: spartan6 Device: xc6slx45 Package: csg484 Speed Grade: -2

☐ Use Stepping

Reset Polarity: Active High

Related Information

[Vendor's Website](#)

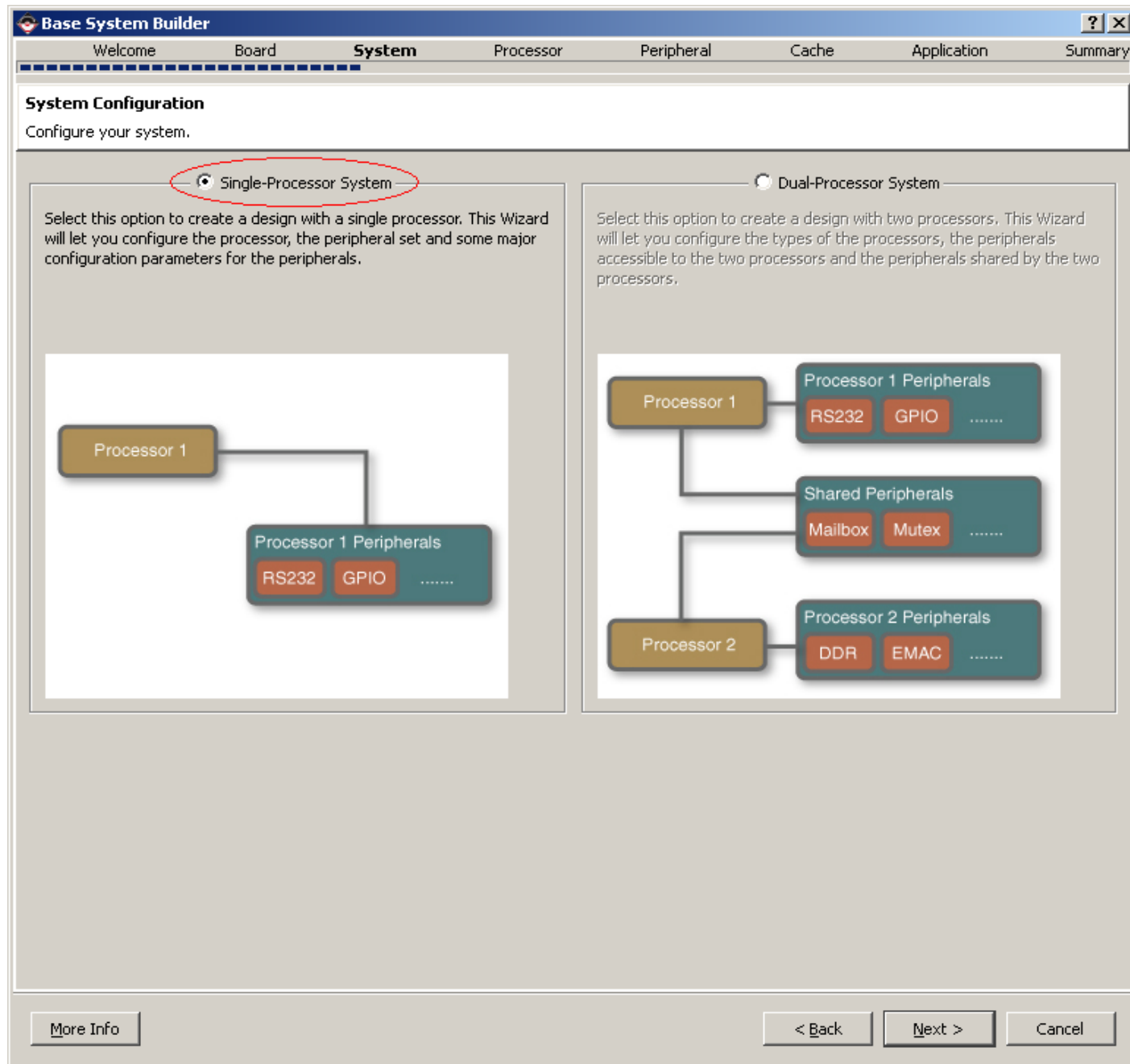
[Vendor's Contact Information](#)

[Third Party Board Definition Files Download Website](#)

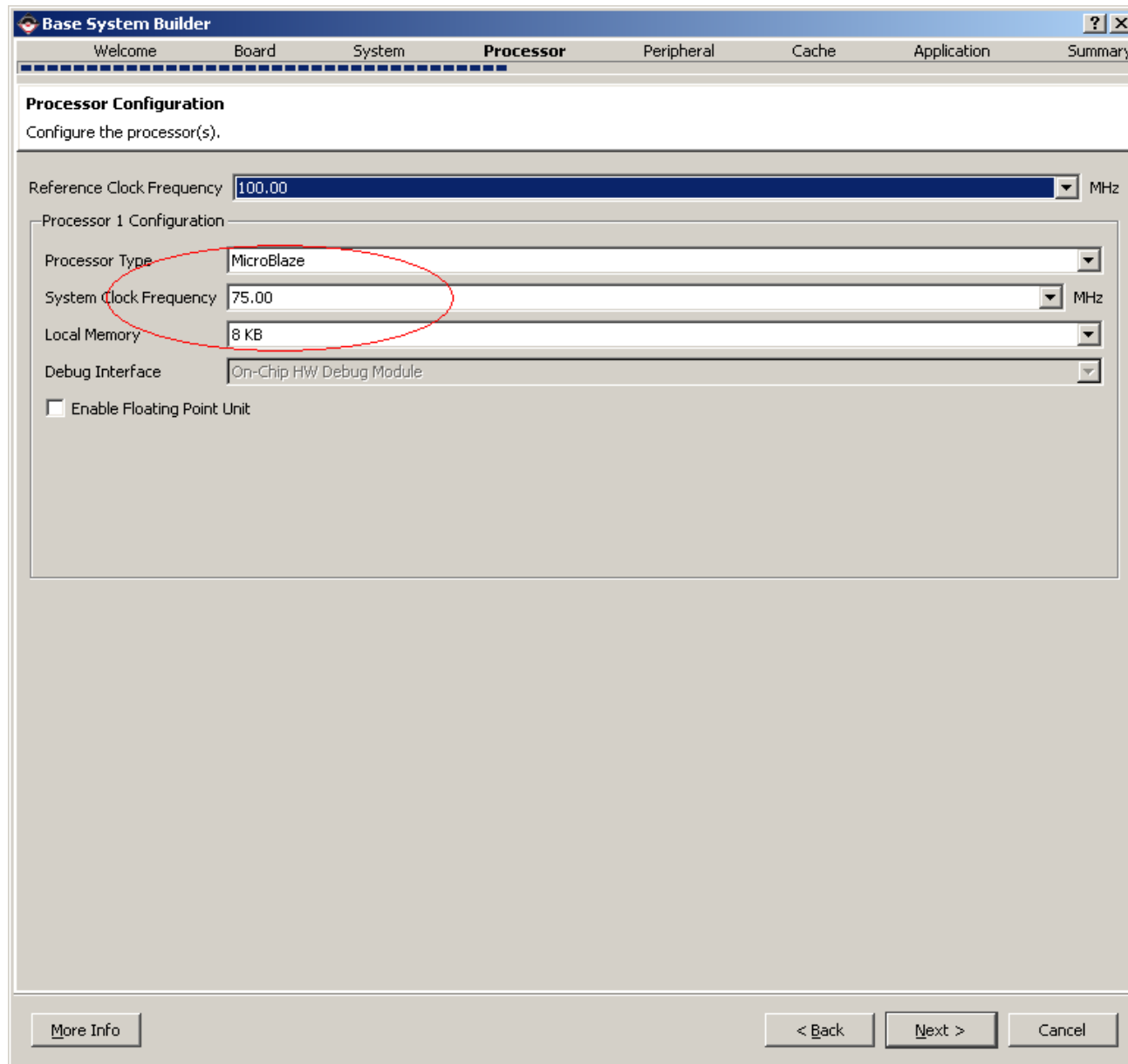
Trenz Electronic TE0630 series are industrial-grade FPGA micro-modules integrating a leading-edge Xilinx Spartan-6 FPGA, a mini-USB 2.0 device port, 1 Gbit (128-Mbyte) DDR3 SDRAM with 16-bit width, 8 Mbyte Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os are provided via rugged high-speed stacking connectors. TE0630 is fully mechanically and largely electrically backward compatible with Trenz Electronic TE0300 Xilinx Spartan-3E FPGA micro-modules.

More Info < Back Next > Cancel

choose correct Vendor, Name and Revision then
click Next



choose Single-Processor System then click Next



The image shows a screenshot of the 'Base System Builder' application window, specifically the 'Processor' tab. The window has a title bar with a question mark and a close button. Below the title bar is a tabbed interface with tabs for 'Welcome', 'Board', 'System', 'Processor' (selected), 'Peripheral', 'Cache', 'Application', and 'Summary'. The main content area is titled 'Processor Configuration' and contains the instruction 'Configure the processor(s)'. It features several configuration options: 'Reference Clock Frequency' set to '100.00' MHz, 'Processor 1 Configuration' section with 'Processor Type' set to 'MicroBlaze', 'System Clock Frequency' set to '75.00' MHz, 'Local Memory' set to '8 KB', and 'Debug Interface' set to 'On-Chip HW Debug Module'. There is also an unchecked checkbox for 'Enable Floating Point Unit'. At the bottom of the window are three buttons: 'More Info', '< Back', and 'Next >', along with a 'Cancel' button.

Base System Builder

Welcome Board System **Processor** Peripheral Cache Application Summary

Processor Configuration
Configure the processor(s).

Reference Clock Frequency 100.00 MHz

Processor 1 Configuration

Processor Type MicroBlaze

System Clock Frequency 75.00 MHz

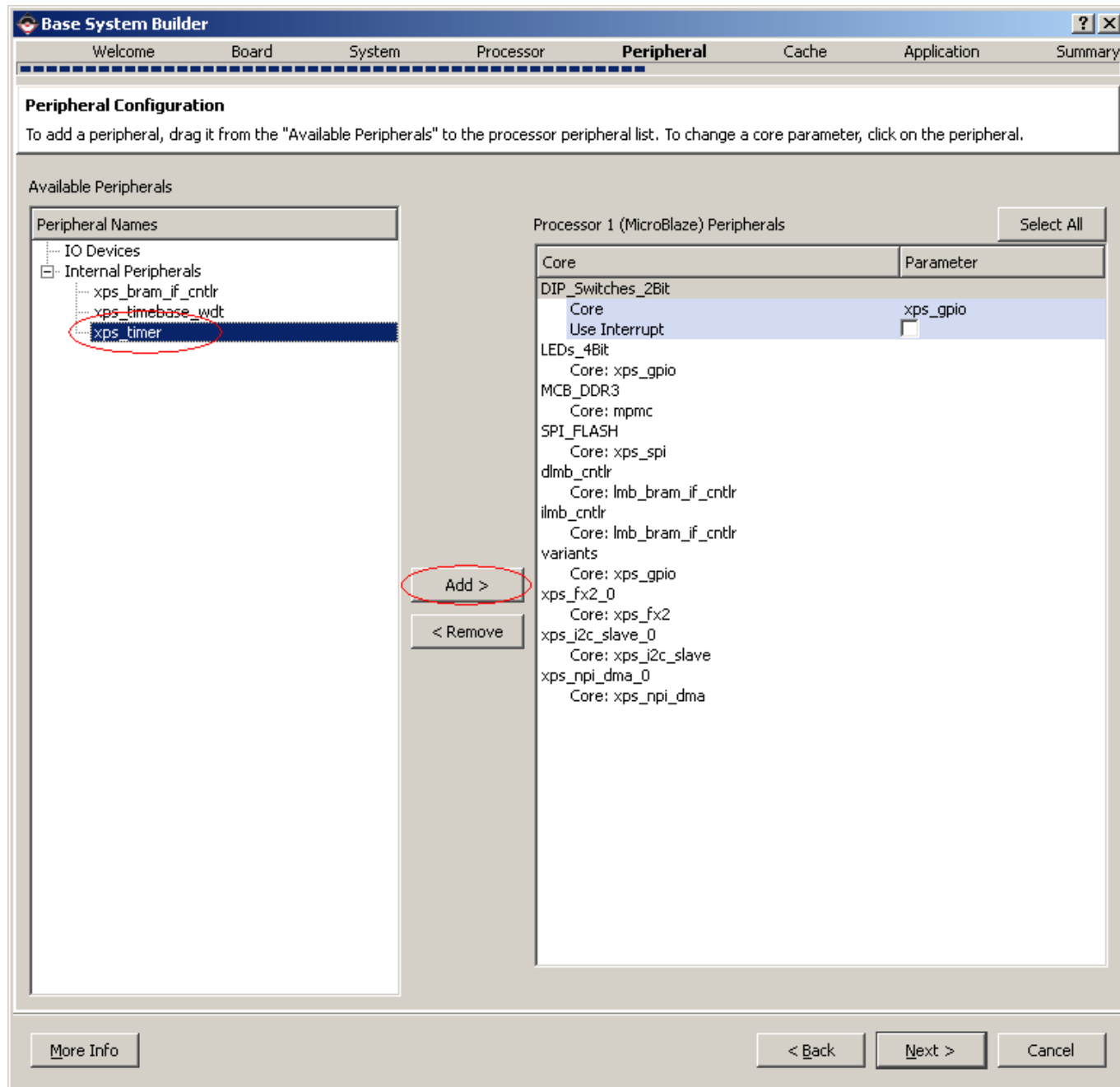
Local Memory 8 KB

Debug Interface On-Chip HW Debug Module

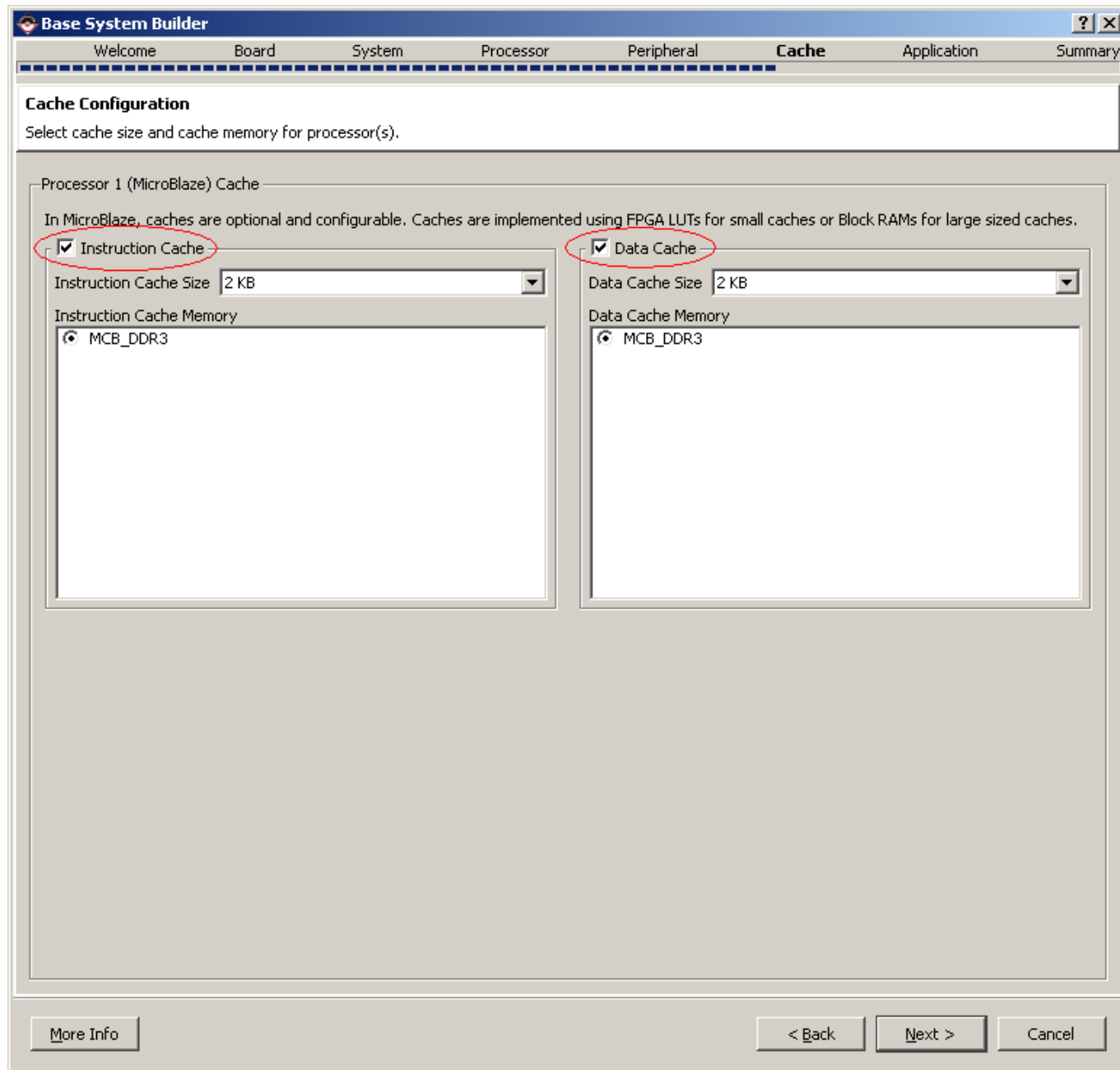
☐ Enable Floating Point Unit

More Info < Back Next > Cancel

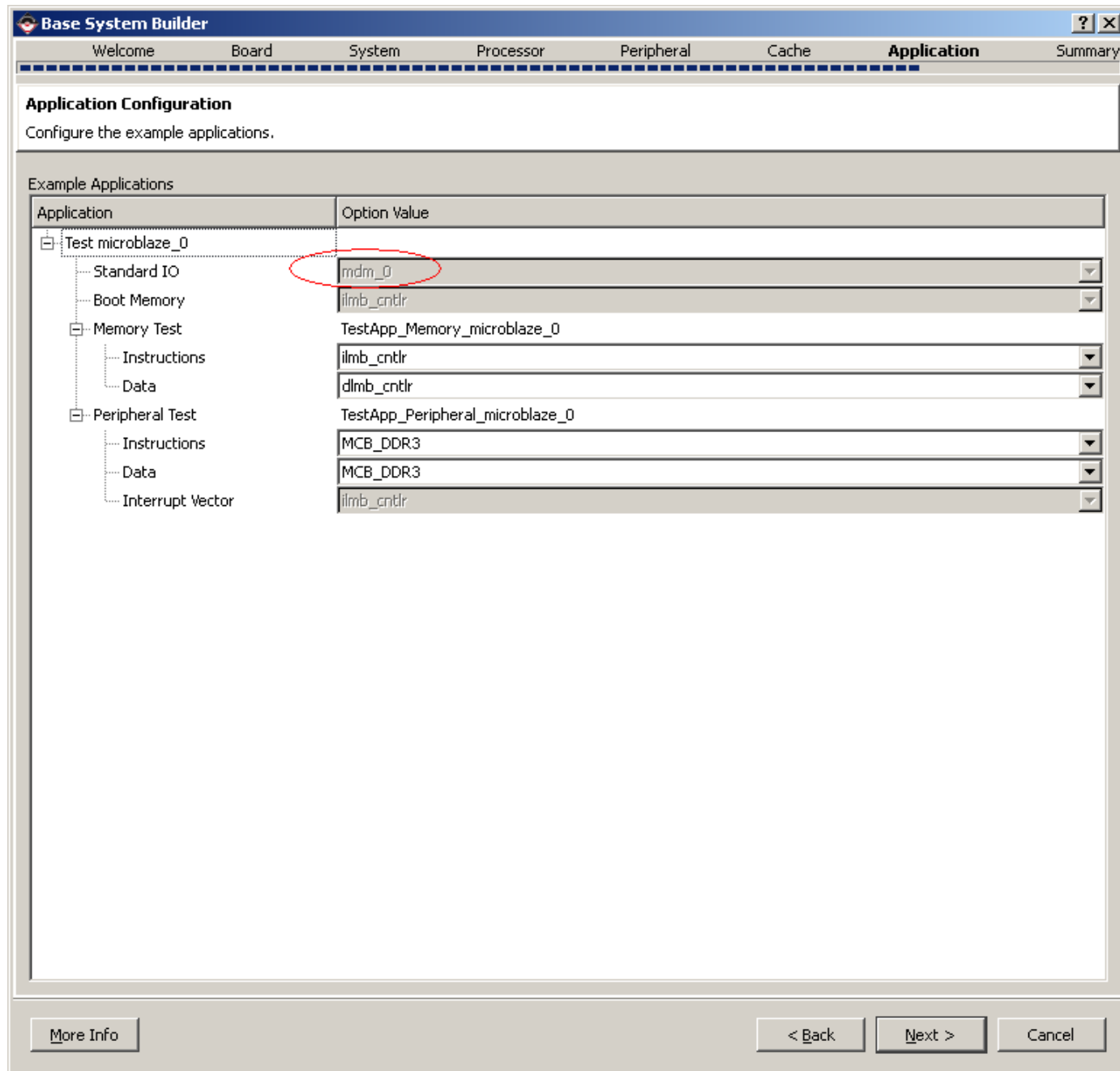
choose default Processor Type, System Clock Frequency (it will be fixed later) and Local Memory size then click Next



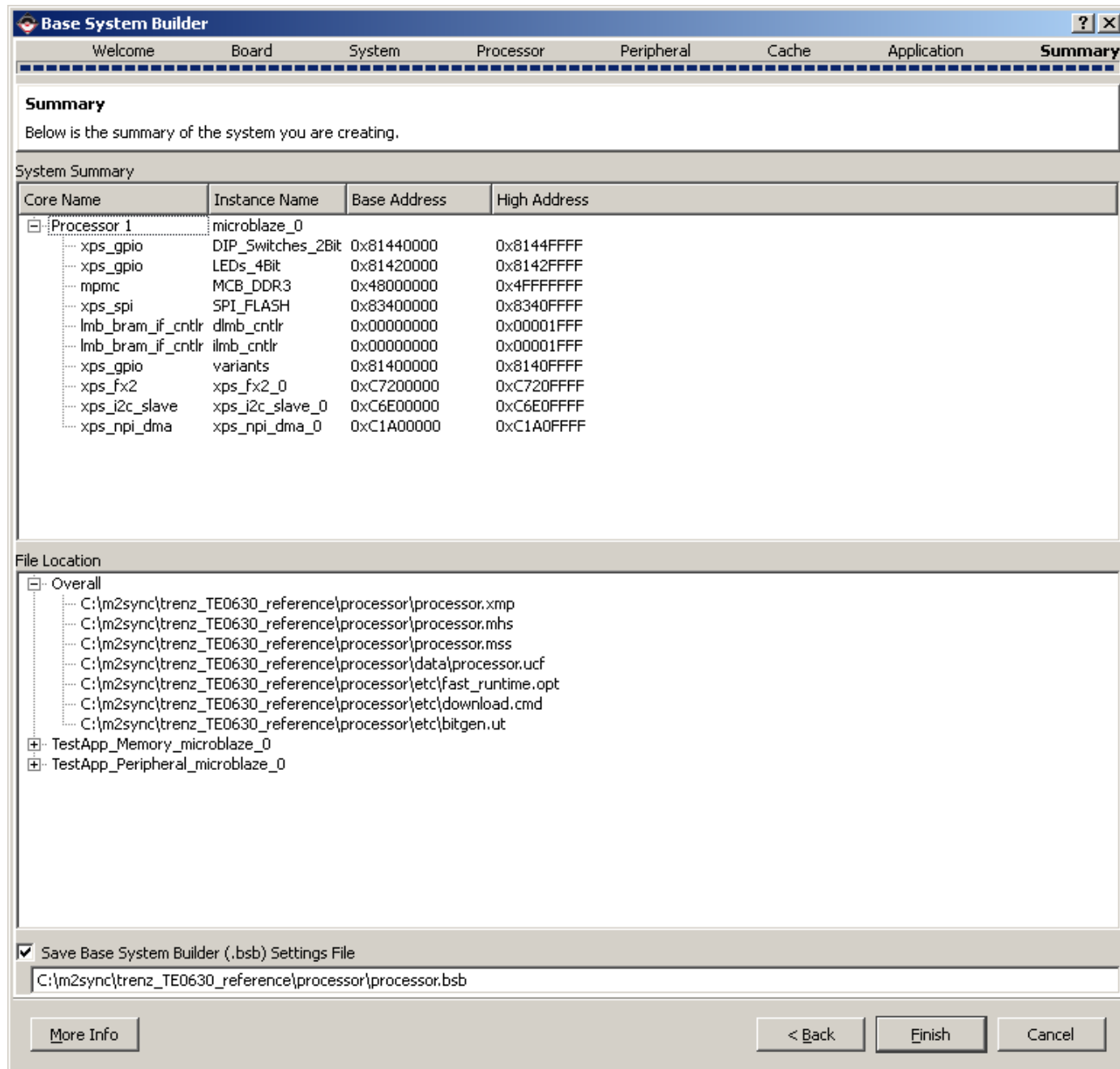
add xps_timer (XilKernel required), then click Next



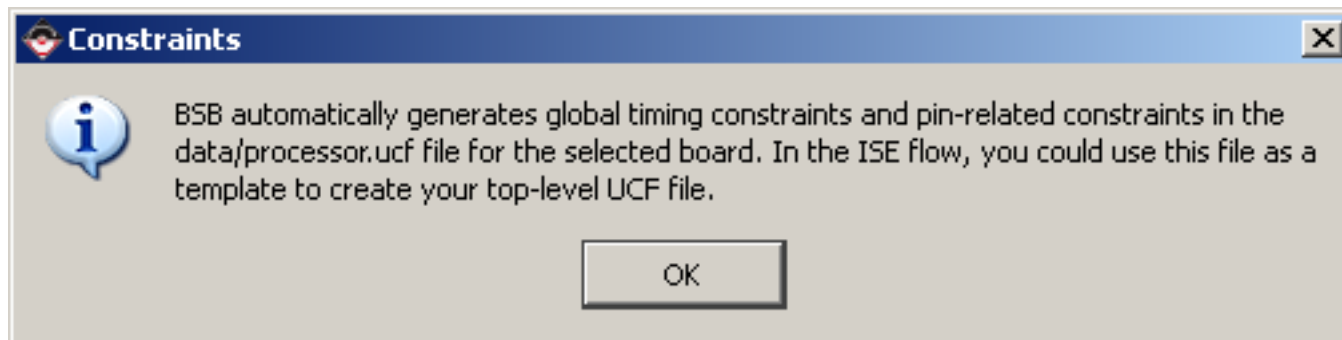
enable Instruction and Data Caches then click Next



verify if mdm_0 choosen as Standard IO then click
Next



verify created configuration then click Finish



confirm UCF file creation

Xilinx Platform Studio - C:\m2sync\trenz_TE0630_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project Platform

Project Files

- MHS File: processor.mhs
- MSS File: processor.mss
- UCF File: data/processor.ucf
- IMPACT Command File: etc/do
- Implementation Options File: e
- Bitgen Options File: etc/bitger

Project Options

- Device: xc6slx45csg484-2
- Netlist: SubModule
- Implementation: Project Navig
- HDL: vhdl
- Sim Model: BEHAVIORAL

Design Summary

Legend

- Master Slave Master/Slave Target Initiator
- Connected Unconnected Monitor
- Production License (paid) License (eval) Local Pre Production Beta Development
- Superseded Discontinued

Bus Interfaces

Name	Bus Name	IP Type	IP Vers
dmb		lmb_v10	1.00.a
ilmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.05.a
microblaze_0		microblaze	8.00.b
lmb_bram		bram_block	1.00.a
dmb_cntlr		lmb_bram_if...	2.10.b
ilmb_cntlr		lmb_bram_if...	2.10.b
MCB_DDR3		mpmc	6.02.a
mdm_0		mdm	2.00.a
xps_fx2_0		xps_fx2	1.30.a
SPLB	mb_plb		
FIFO_IN	xps_npi_dma_0_DMA_OUT		
FIFO_OUT	xps_fx2_0_FIFO_OUT		
DIP_Switches_28it		xps_gpio	2.00.a
LEDs_48it		xps_gpio	2.00.a
variants		xps_gpio	2.00.a
xps_i2c_slave_0		xps_i2c_slave	1.20.a
xps_npi_dma_0		xps_npi_dma	3.00.a
SPLB	mb_plb		
DMA_IN	xps_fx2_0_FIFO_OUT		
DMA_OUT	xps_npi_dma_0_DMA_OUT		
MPMC_PIM	xps_npi_dma_0_MPMC_PIM		

Bus Interface Filters

- By Connection
 - Connected
 - Unconnected
- By Bus Standard
 - LMB
 - PLBV46
- Xilinx Point To Point
 - XIL_BRAM
 - XIL_BSCAN
 - XIL_MBDEBUG3
 - XIL_MBTRACE2
 - XIL_MEMORY_C...
 - XIL_NPI
- User Defined
- By Interface Type
 - Slaves
 - Masters
 - Master Slaves
 - Monitors
 - Targets
 - Initiators

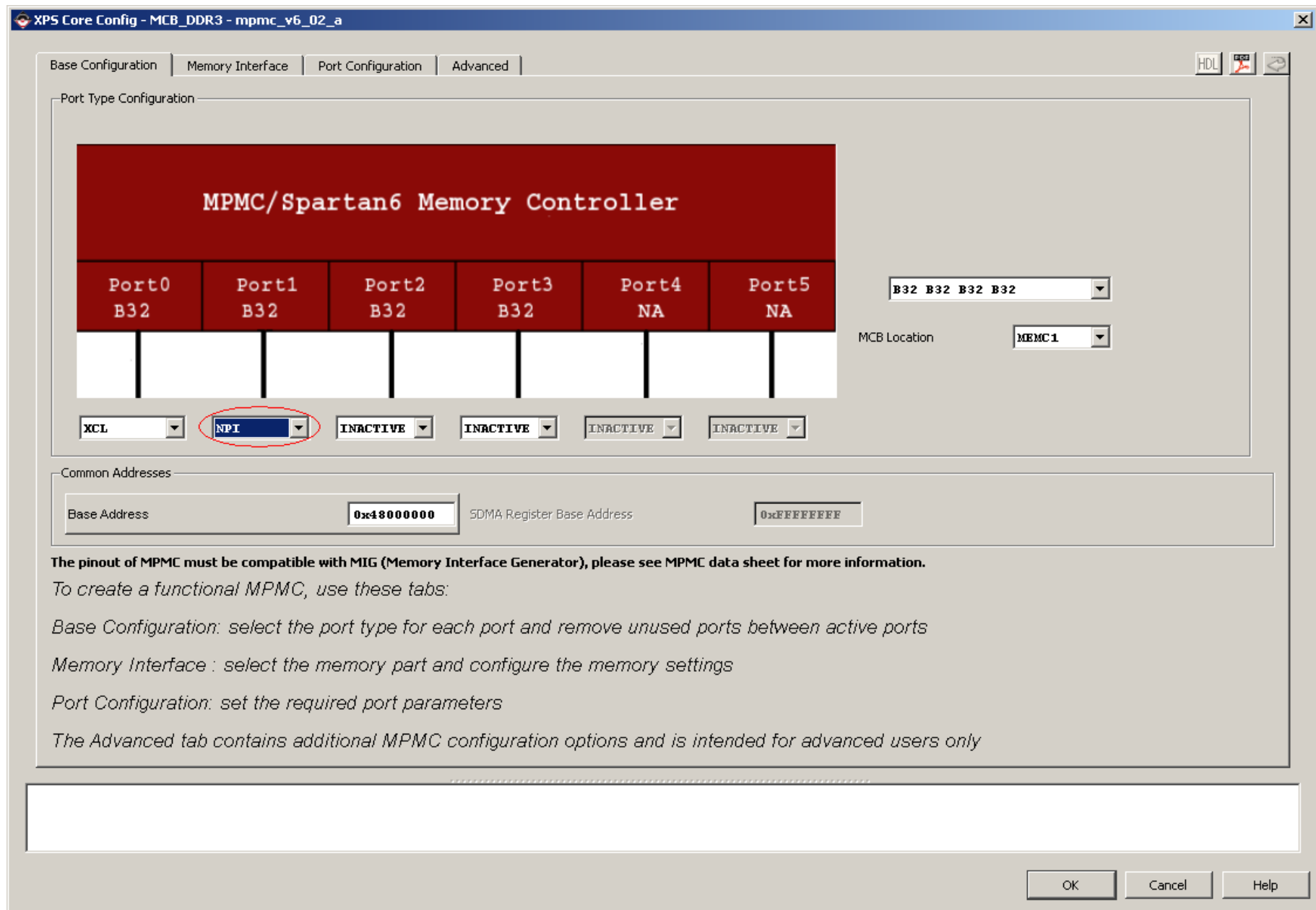
Console

```

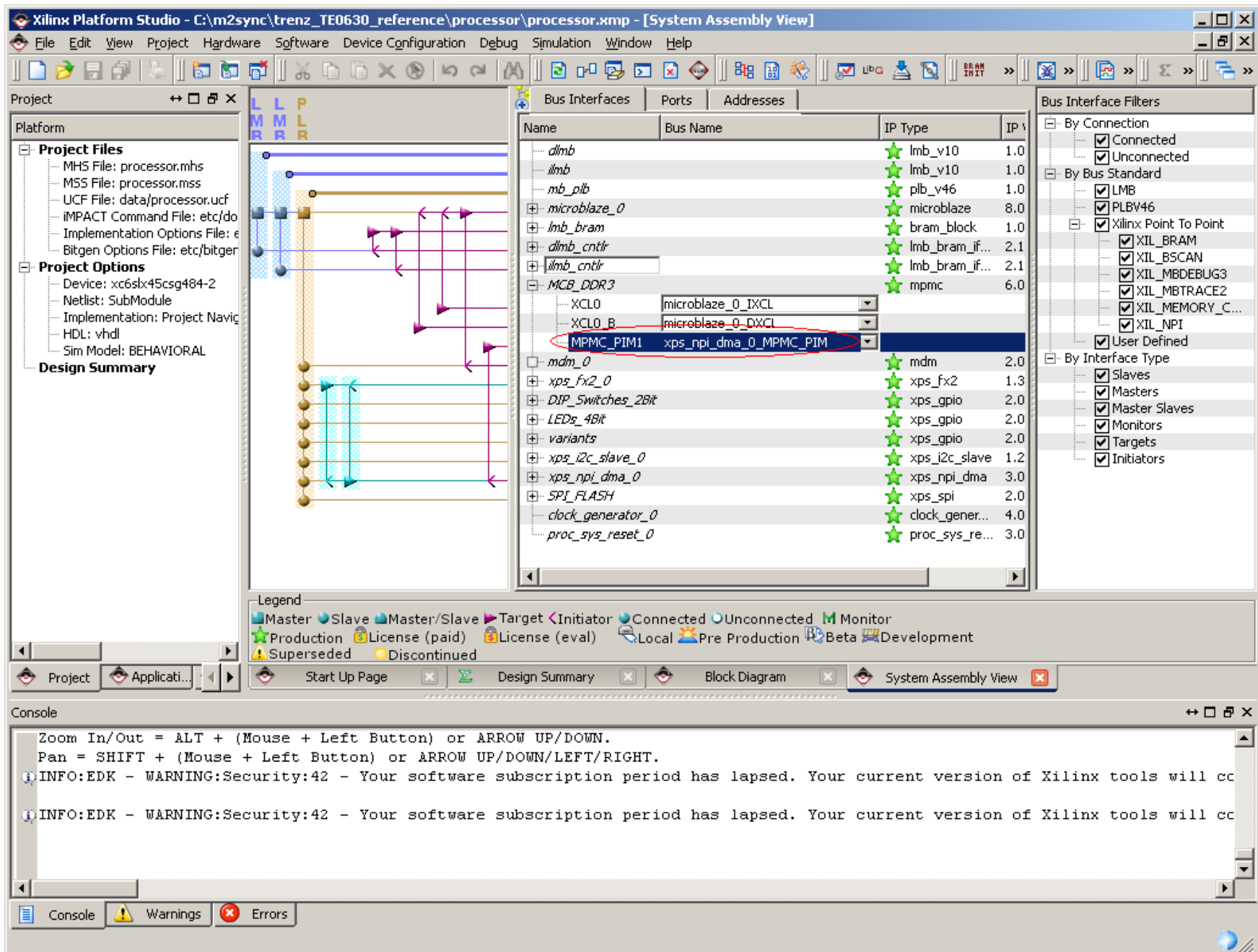
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
  
```

Console Warnings Errors

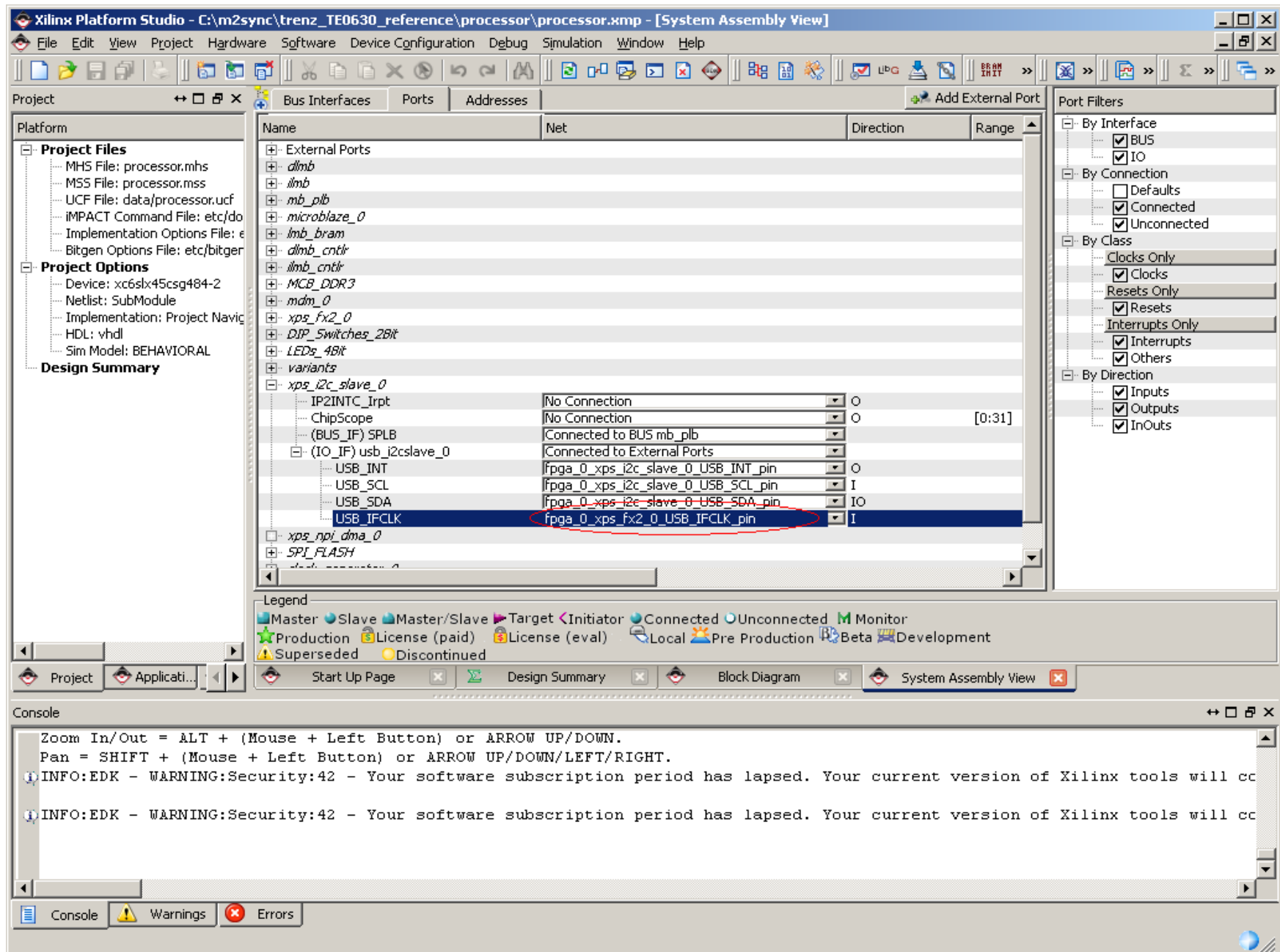
connect np_i_dma and fx2 pcores to each other



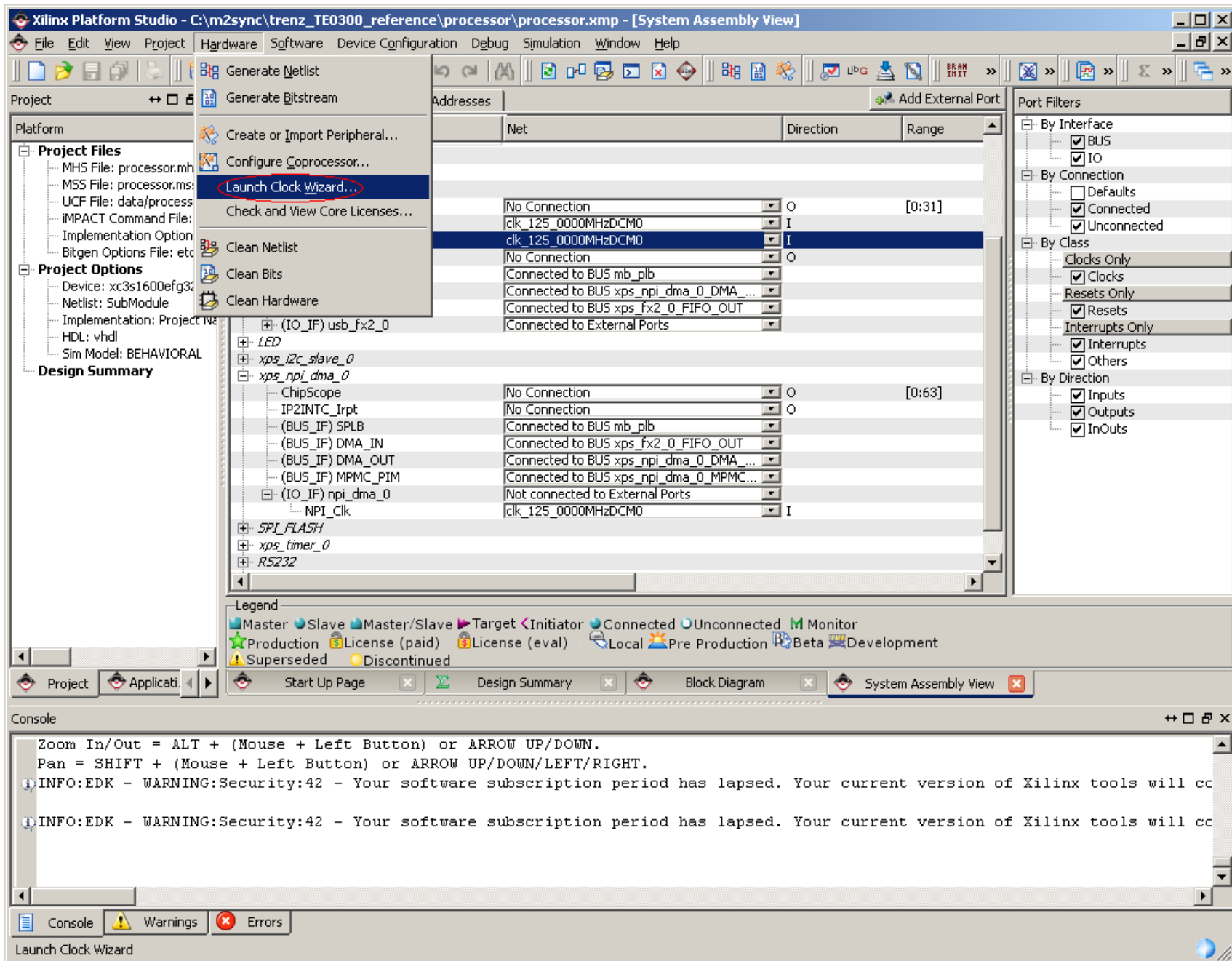
double click on MCB_DDR3 pcore and configure NPI port



connect mpmc and npi_dma pcores



switch to Ports tab and connect xps_i2c clock signal



launch Clock Wizard

Clock Wizard

System | Ports Overview

Input Clock
 Net name: Frequency: MHz

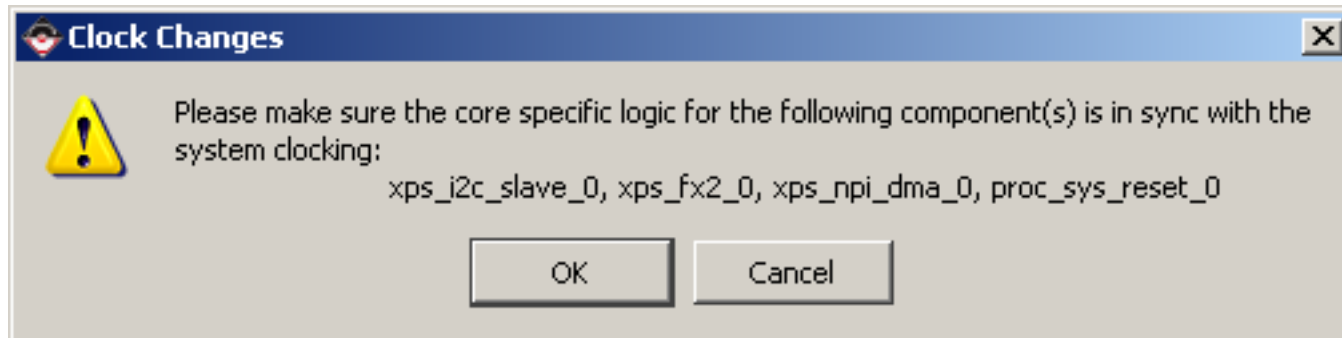
☐ Enable full dynamic range of clock frequencies (allow 1 MHz to 1000 MHz for spartan6-2).

Component	Frequency (MHz)	Phase	Buffered	Minimum Frequency	Maximum
Buses					
Peripherals					
MCB_DDR3	75.000000	0	TRUE	1.000000	100.000000
MPMC_Clk_Mem_2x	600.000000	0	FALSE	600.000000	625.000000
MPMC_Clk_Mem_2x_180	600.000000	180	FALSE	600.000000	625.000000
xps_i2c_slave_0	0.000000	0	TRUE	0.000000	1000.000000
USB_IFCLK	0.000000	0	TRUE	0.000000	1000.000000
xps_fx2_0	0.000000	0	TRUE	0.000000	1000.000000
USB_IFCLK	0.000000	0	TRUE	0.000000	1000.000000
TX_FIFO_Clk	100.000000	0	TRUE	0.000000	1000.000000
RX_FIFO_Clk	100.000000	0	TRUE	0.000000	1000.000000
xps_npi_dma_0	100.000000	0	TRUE	0.000000	1000.000000
NPI_Clk	100.000000	0	TRUE	0.000000	1000.000000
proc_sys_reset_0					

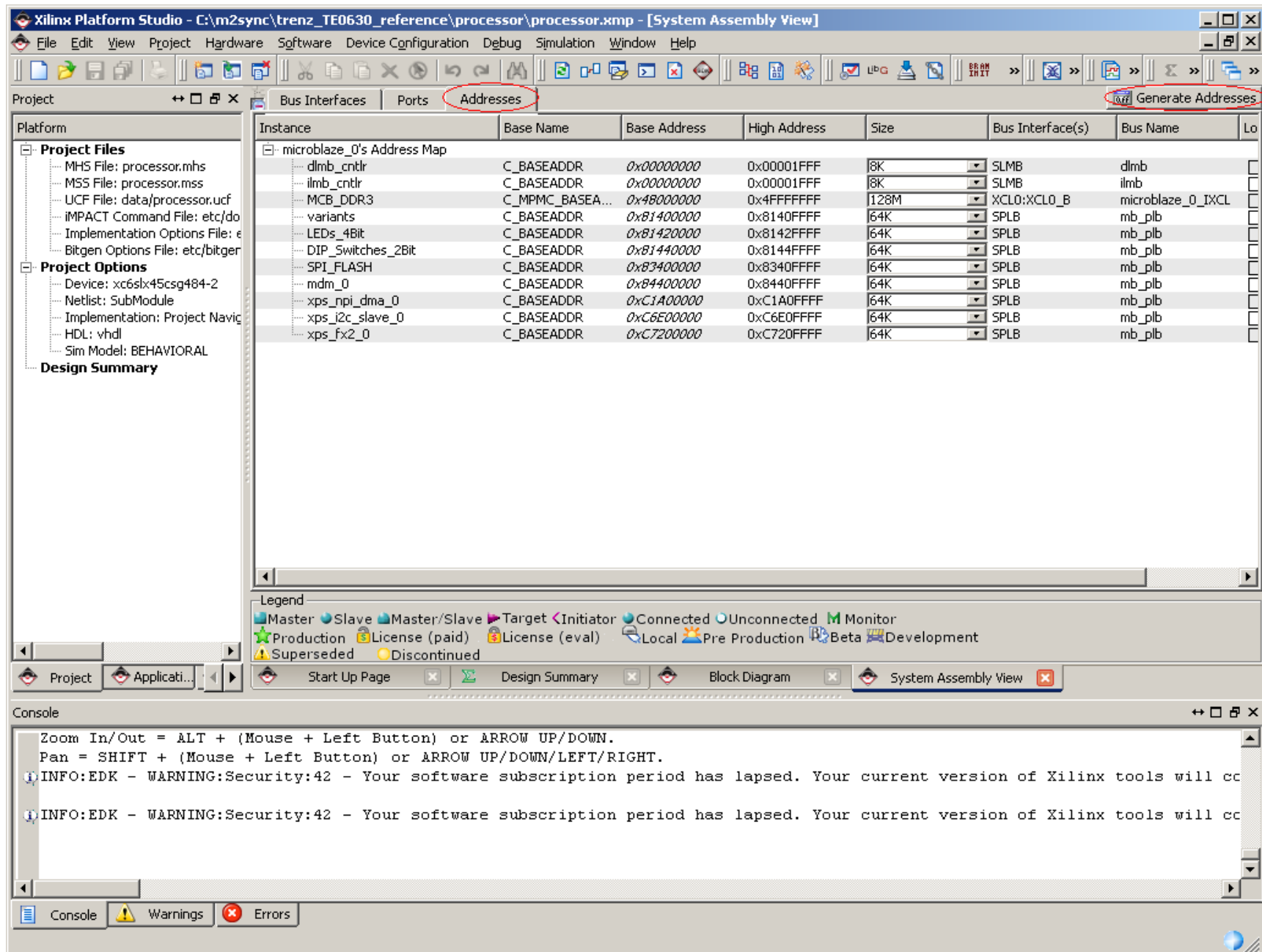
Clock configuration status: Clocks are configured, but need to be validated.

NOTE: The MicroBlaze processor and its buses run at the same speed, therefore, only the MicroBlaze needs configuration.

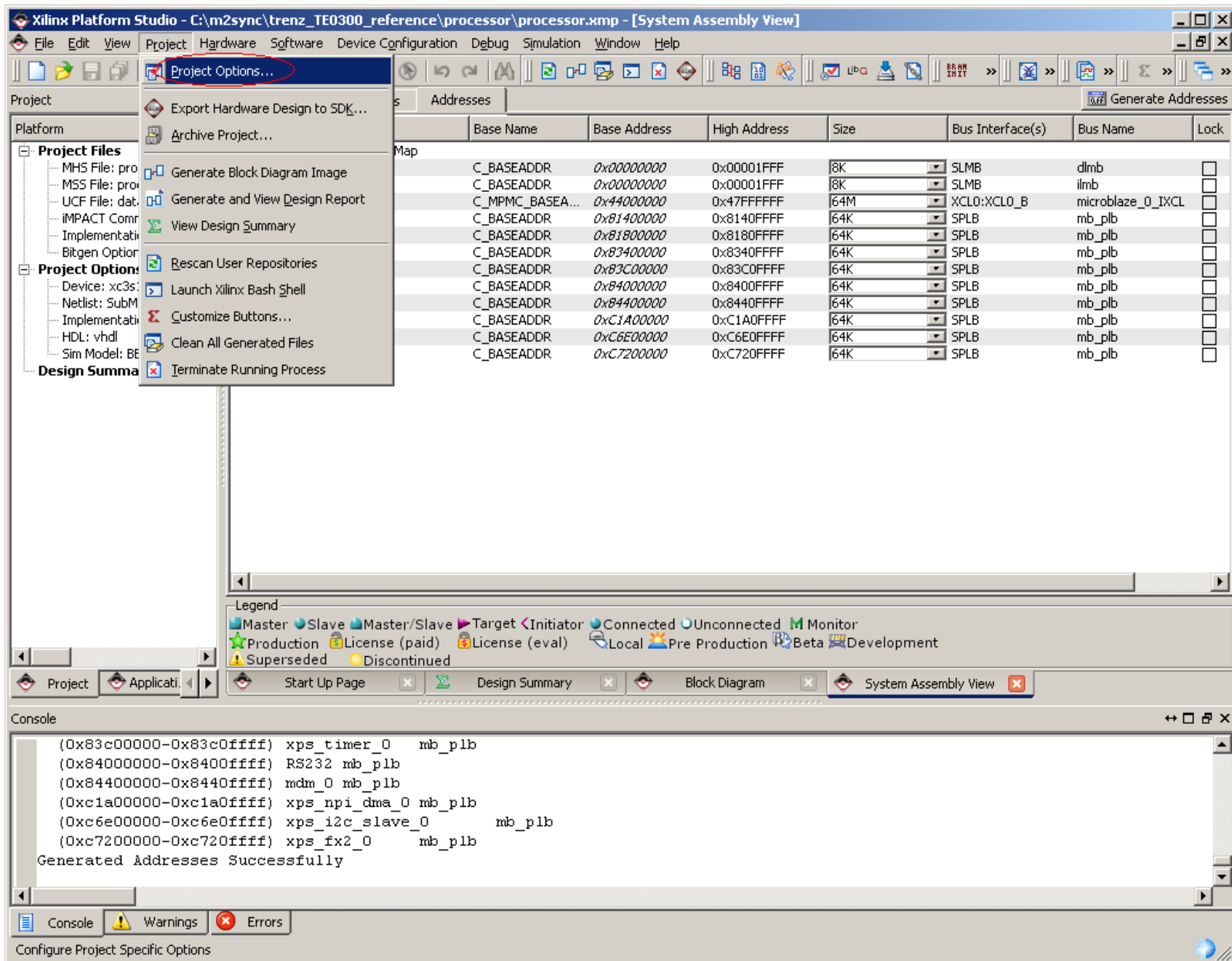
specify clocks for xps_fx2 and xps_npi_dma pcores,
 validate them, then click OK



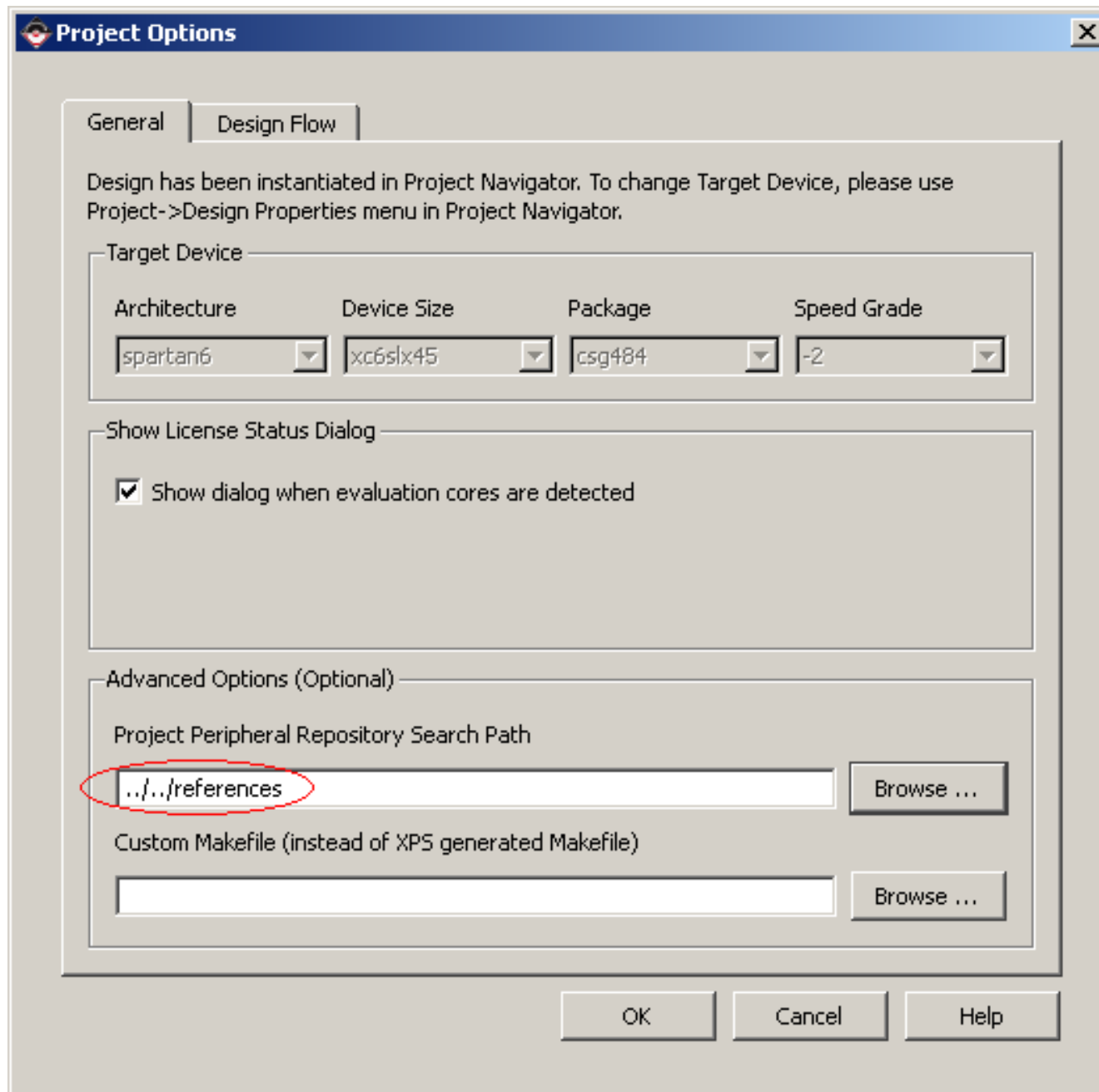
confirm Clock Changes



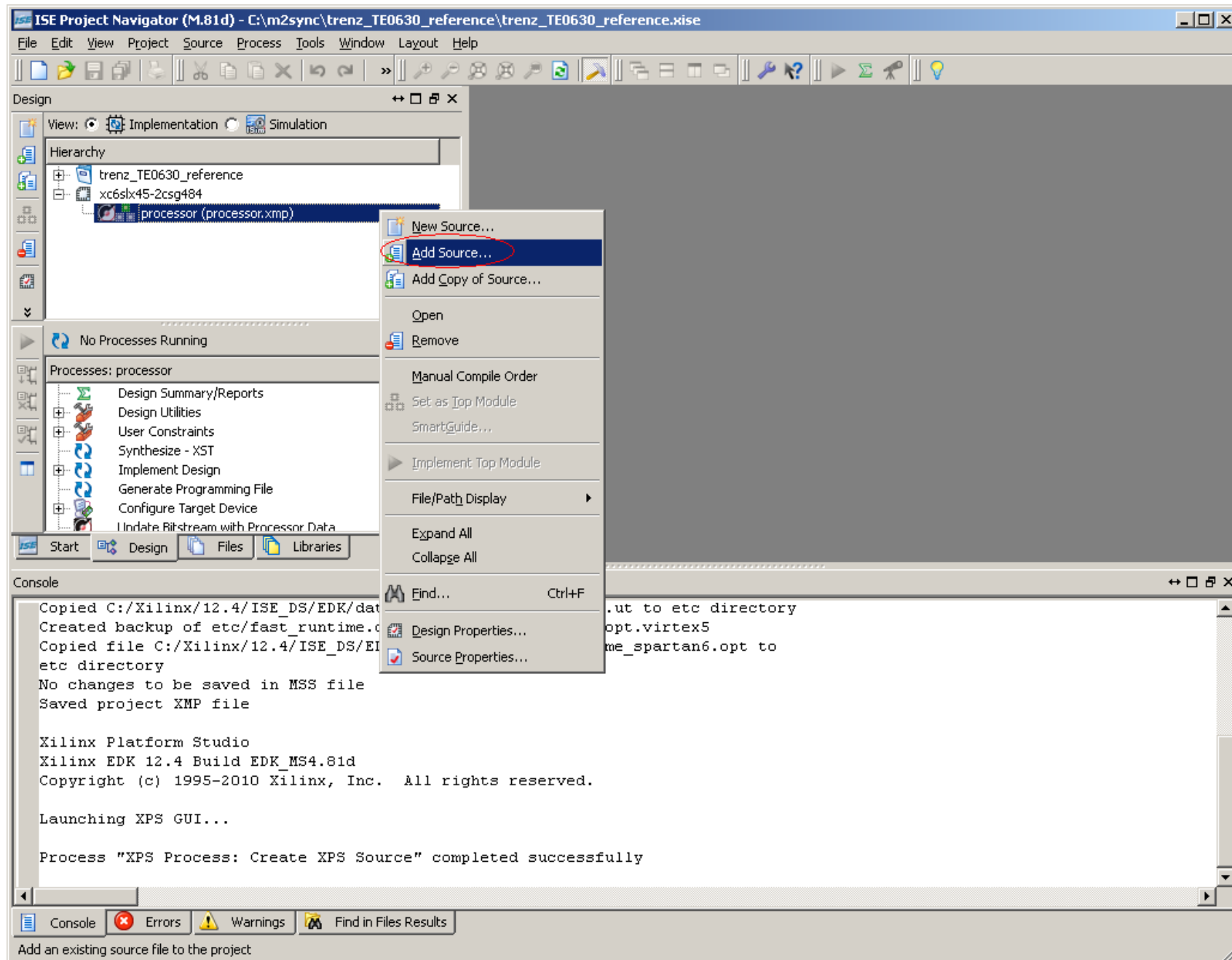
switch to Addresses tab and re-generate addresses



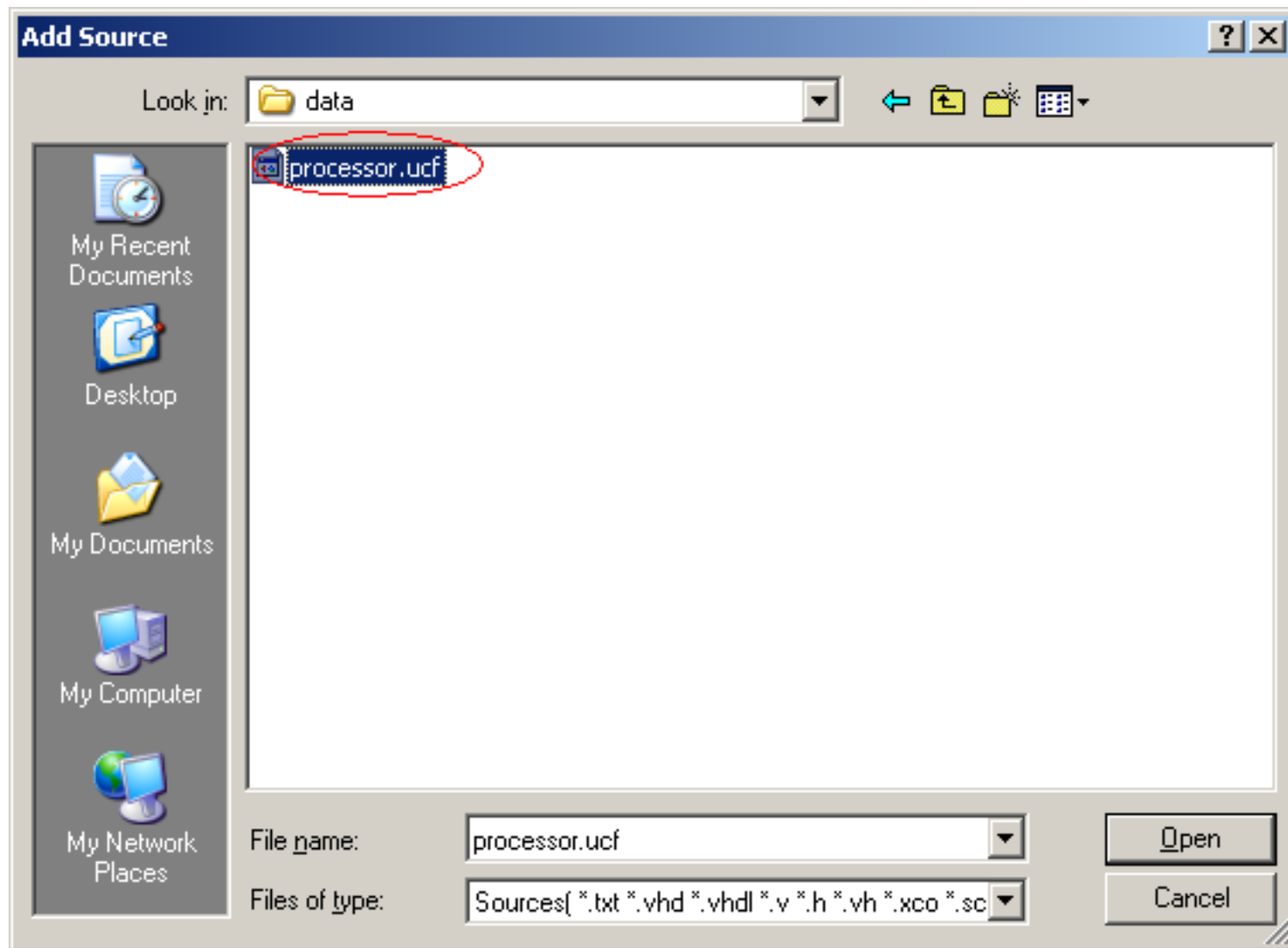
launch Project Options



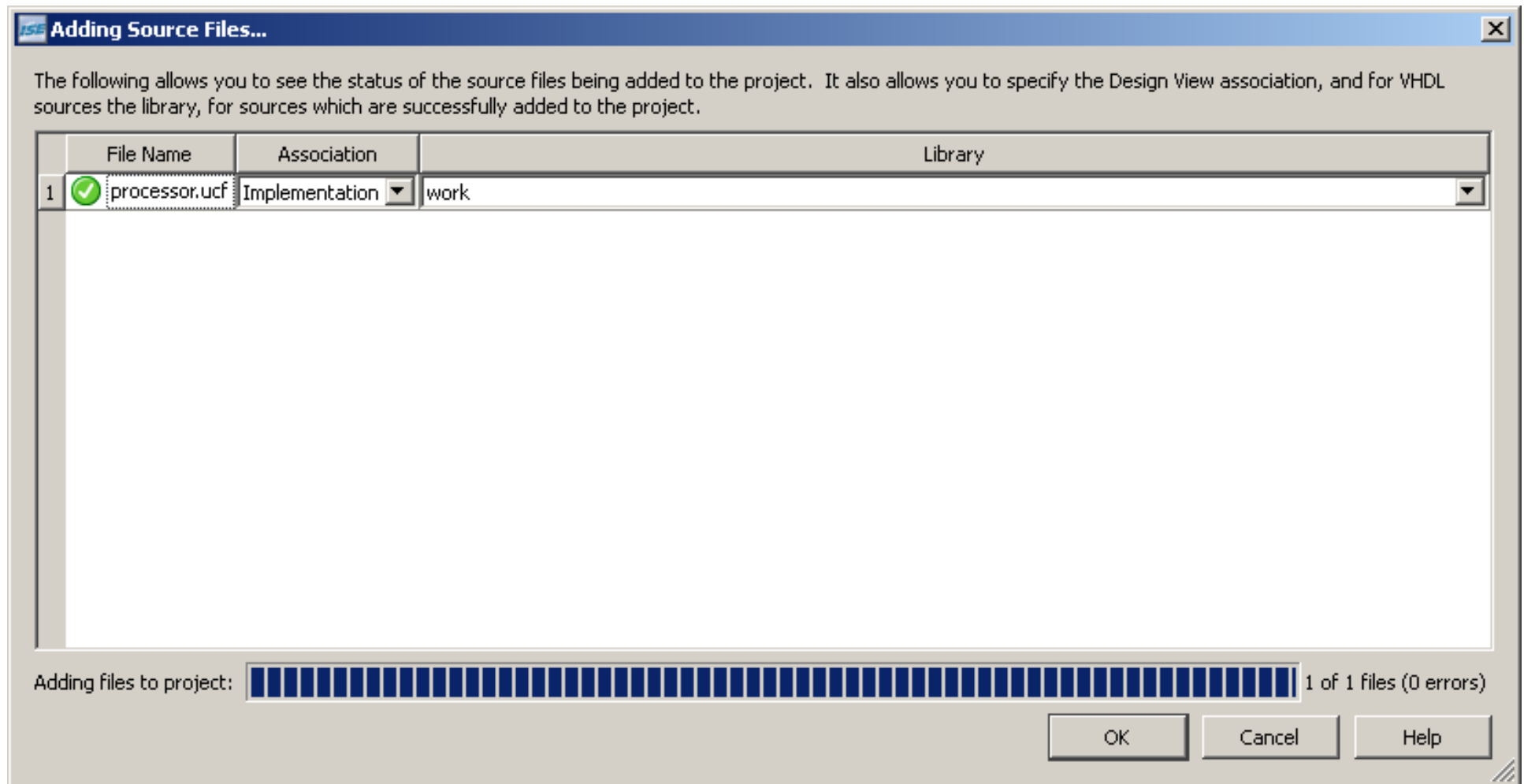
provide path to the private pcores (npi_dma, fx2, i2c_slave) then click OK



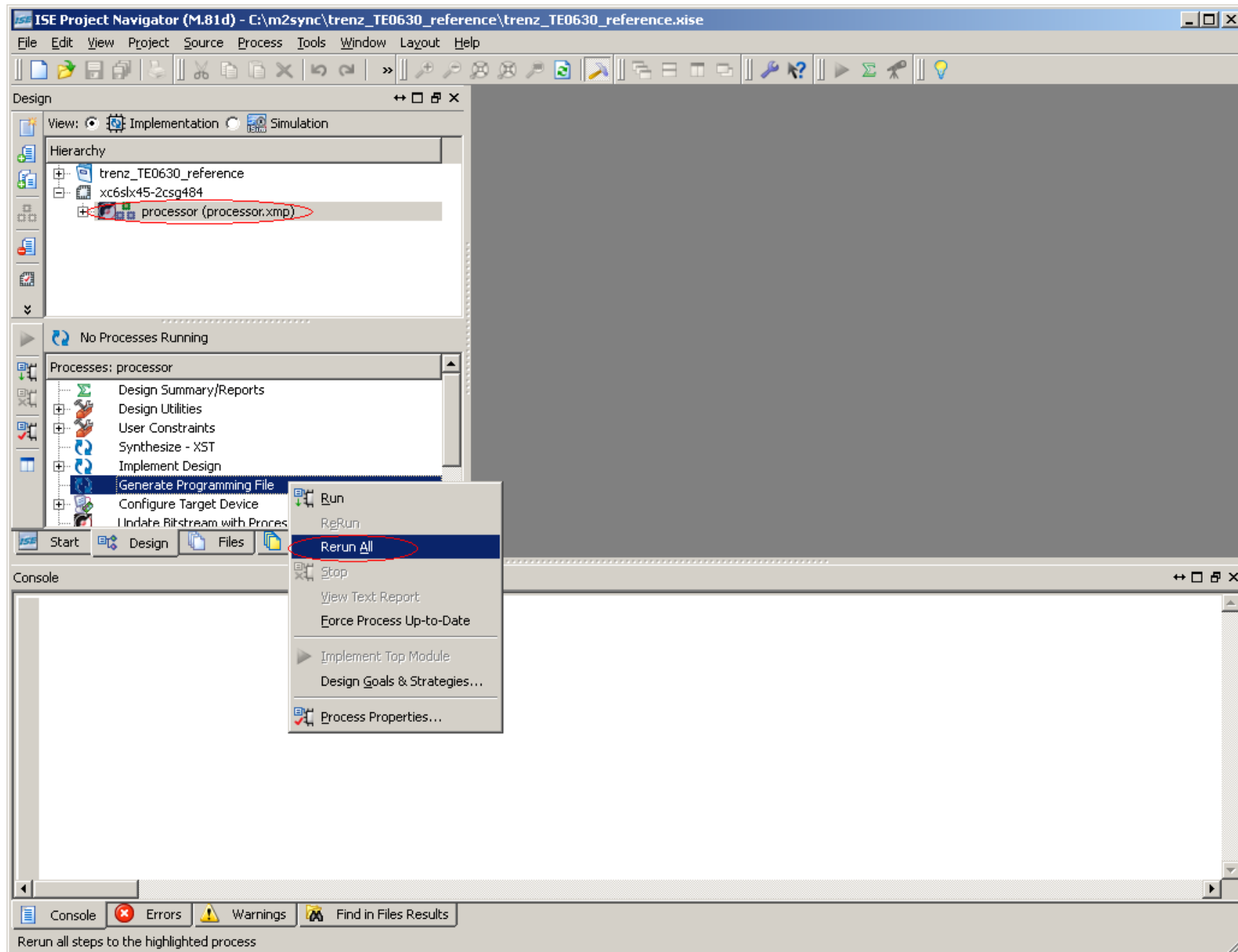
return to ISE Project Navigator and add Source



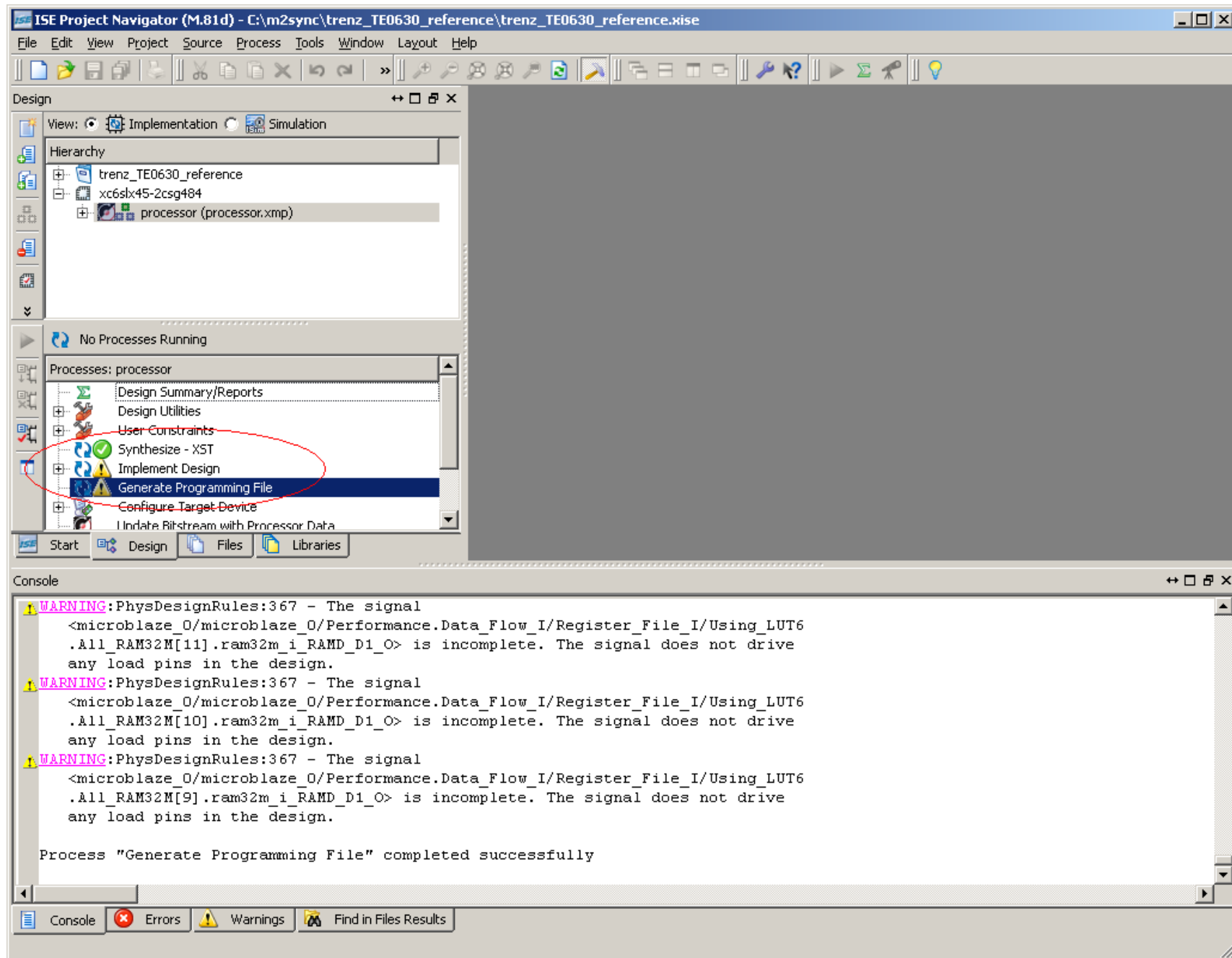
choose processor.ucf from processor/data/ subfolder
then click Open



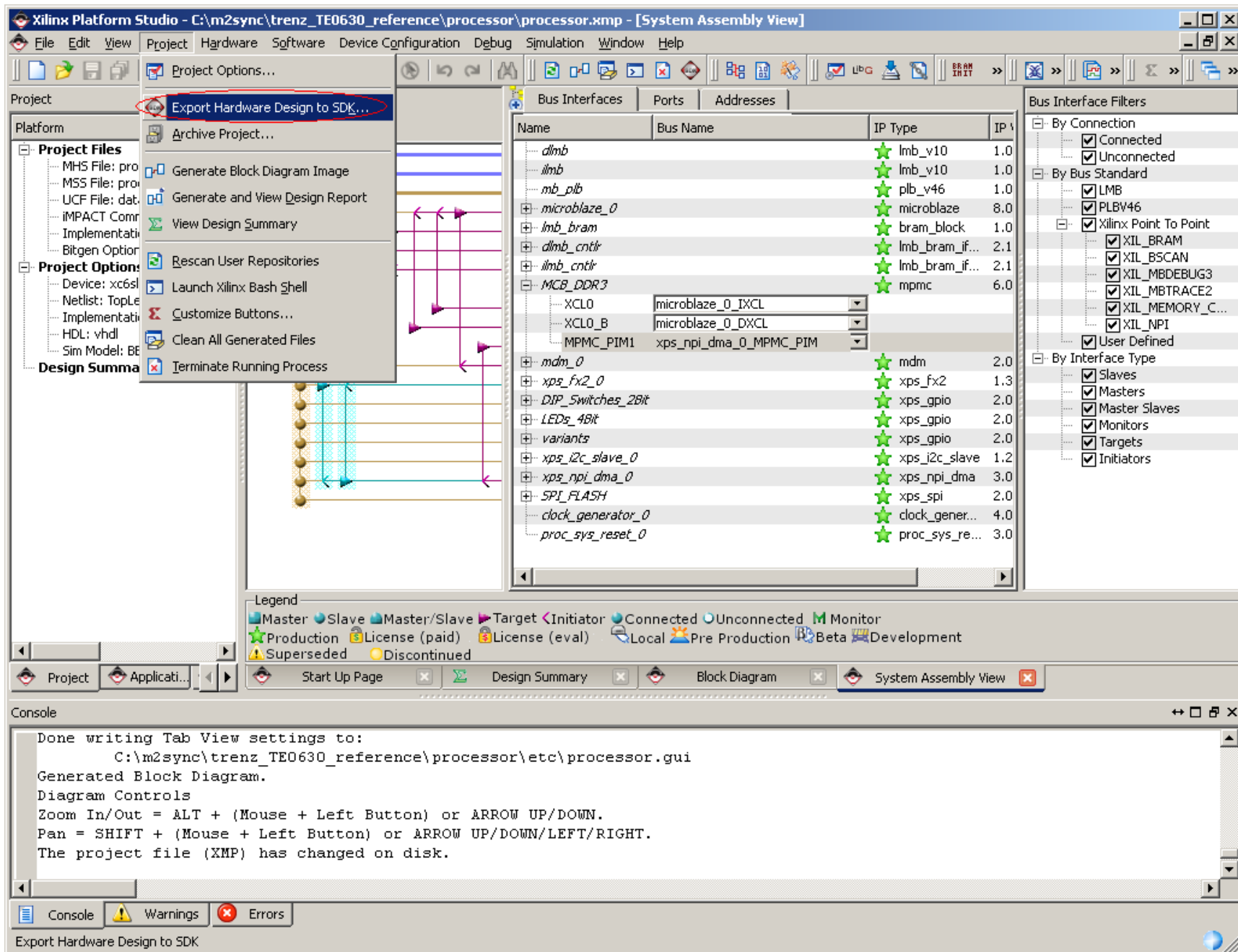
confirm adding Source File by clicking OK



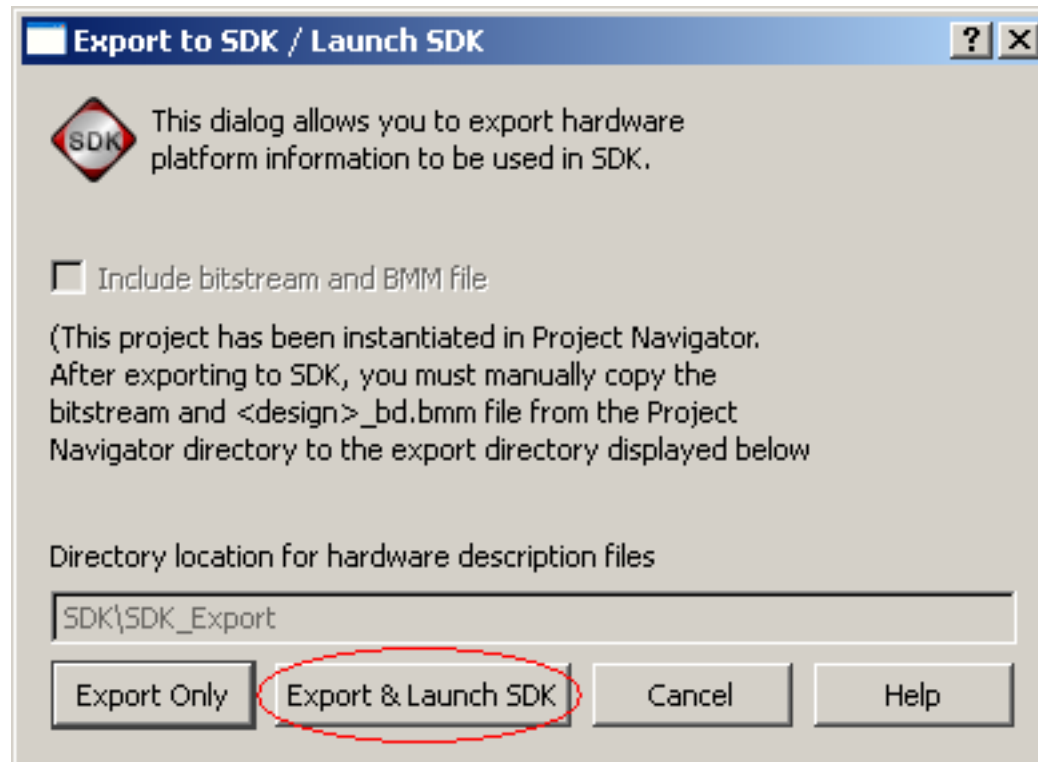
step on processor.xmp, choose Generate Programming File and click Rerun All



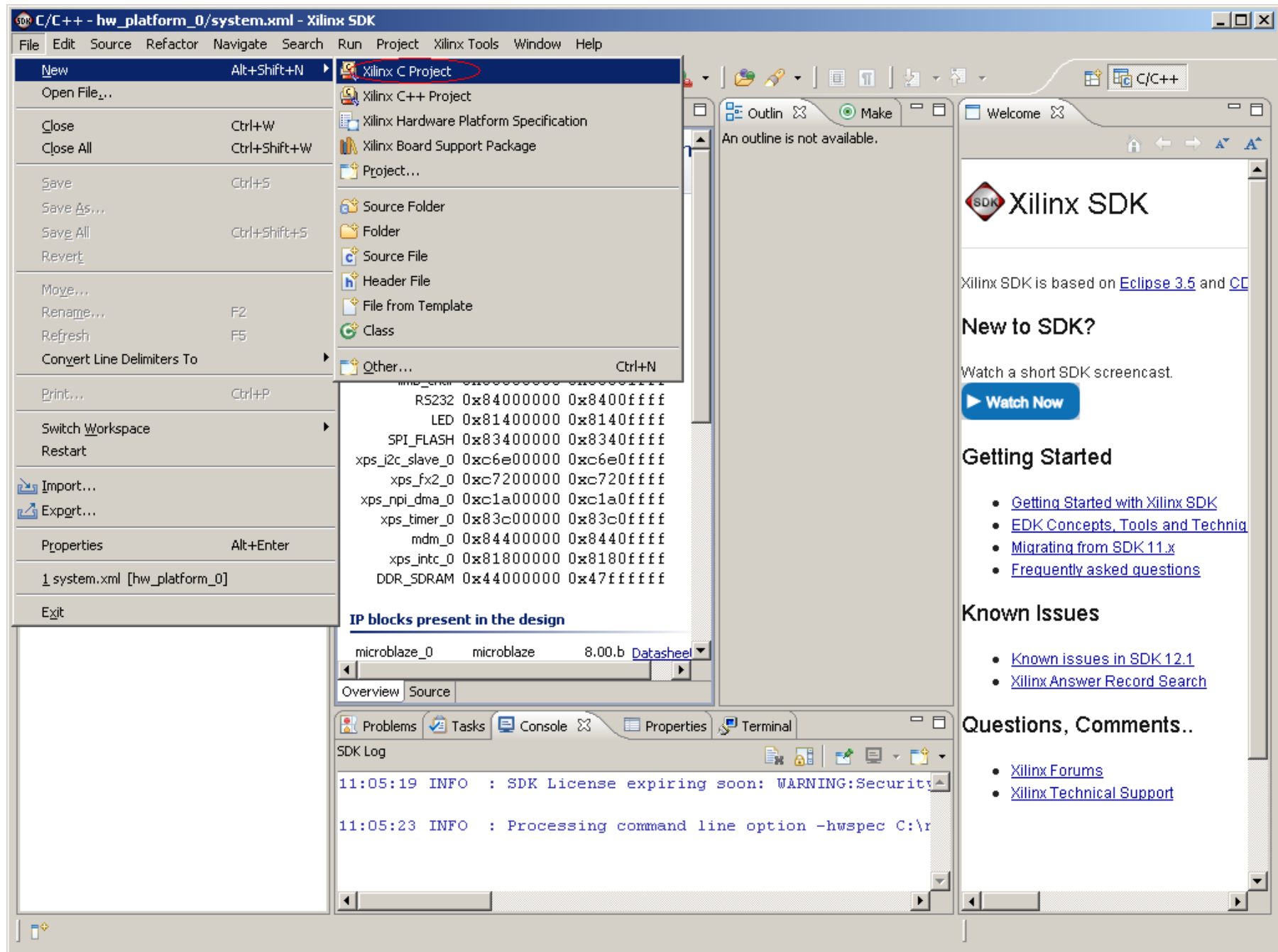
confirm generation success and return to Xilinx Platform Studio



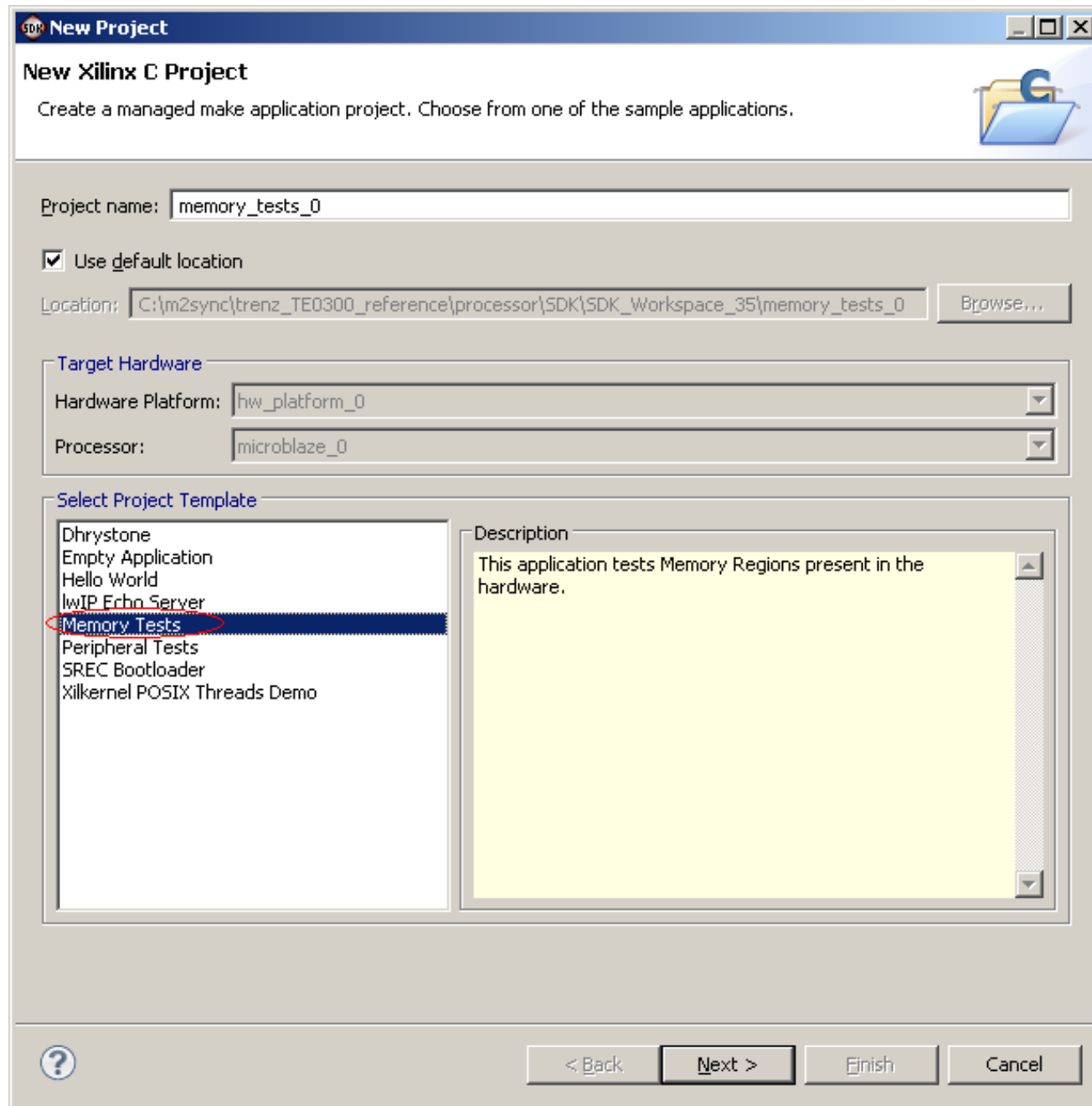
choose from menu Export Hardware Design to SDK



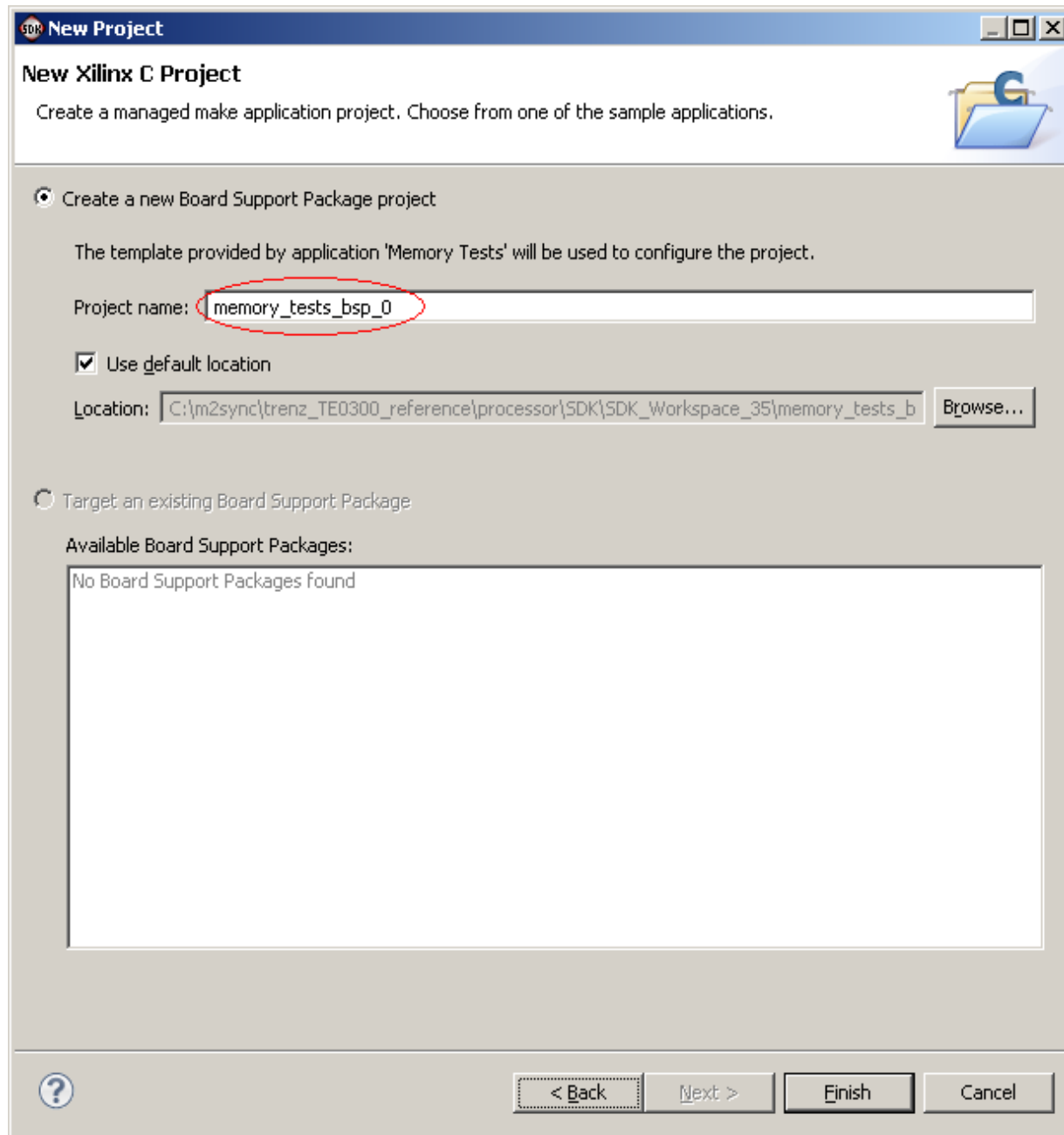
because Xilinx SDK isn't running yet, choose Export & Launch SDK button



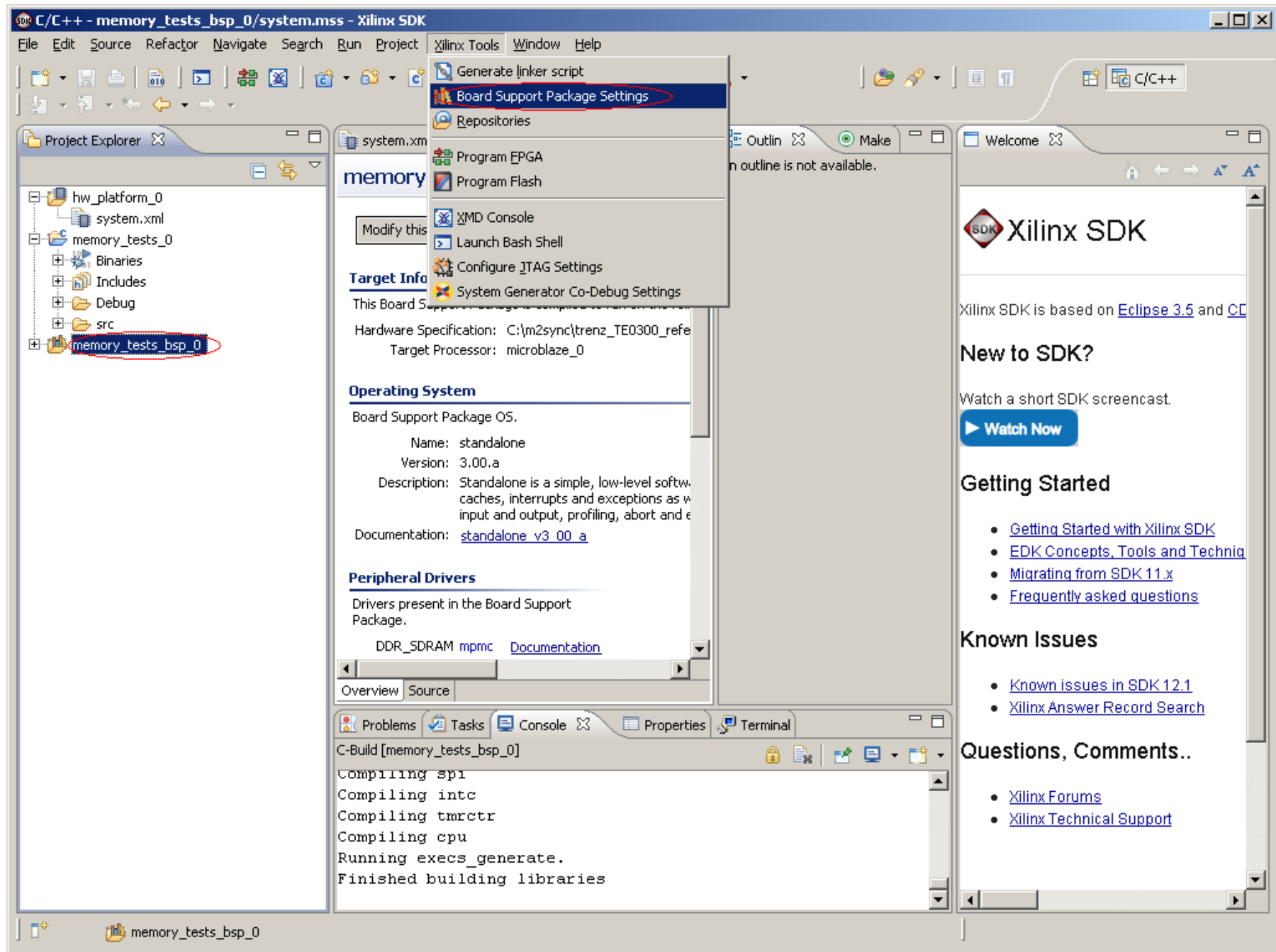
from SDK menu choose to create New Xilinx C Project



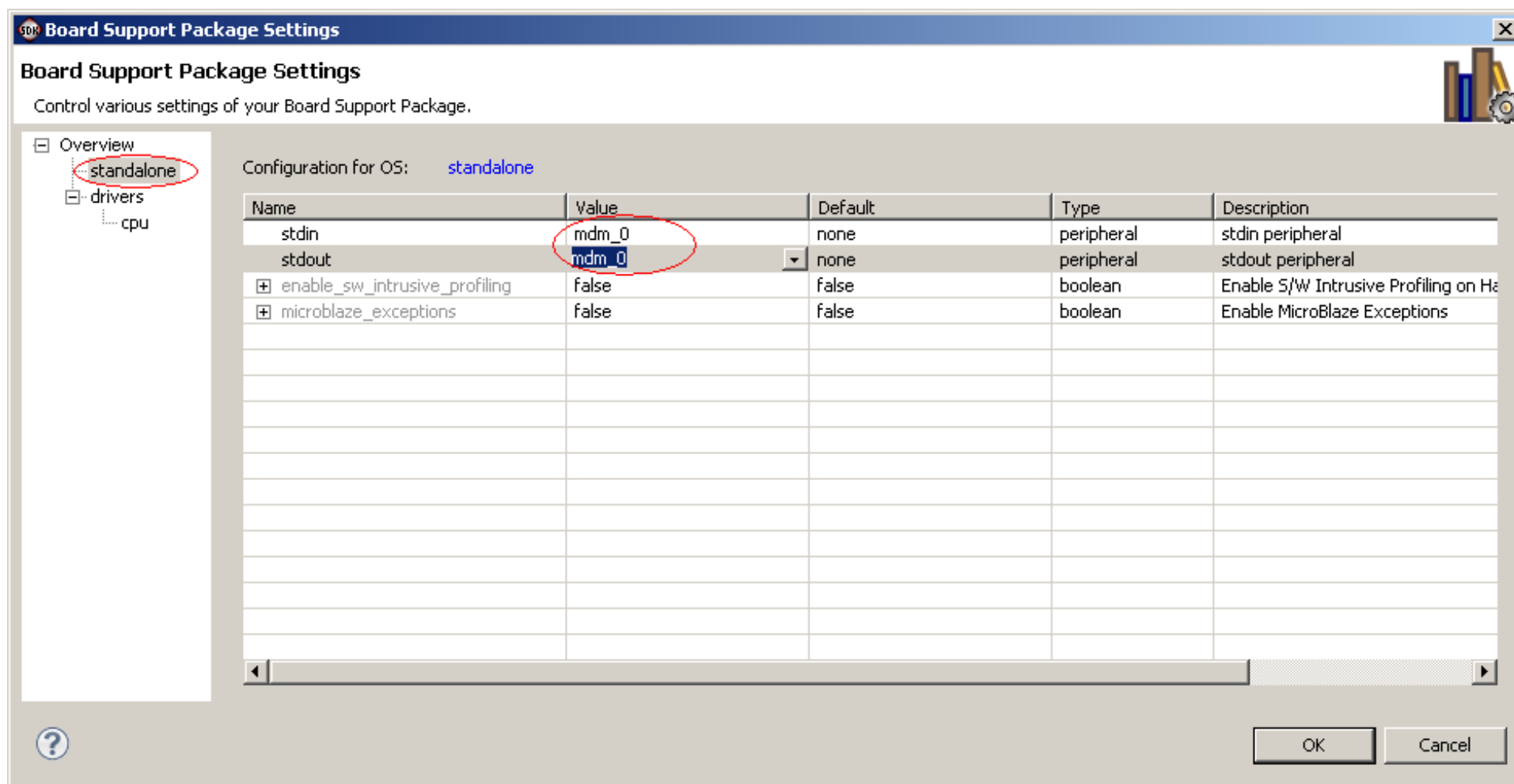
choose Memory Tests template and click Next



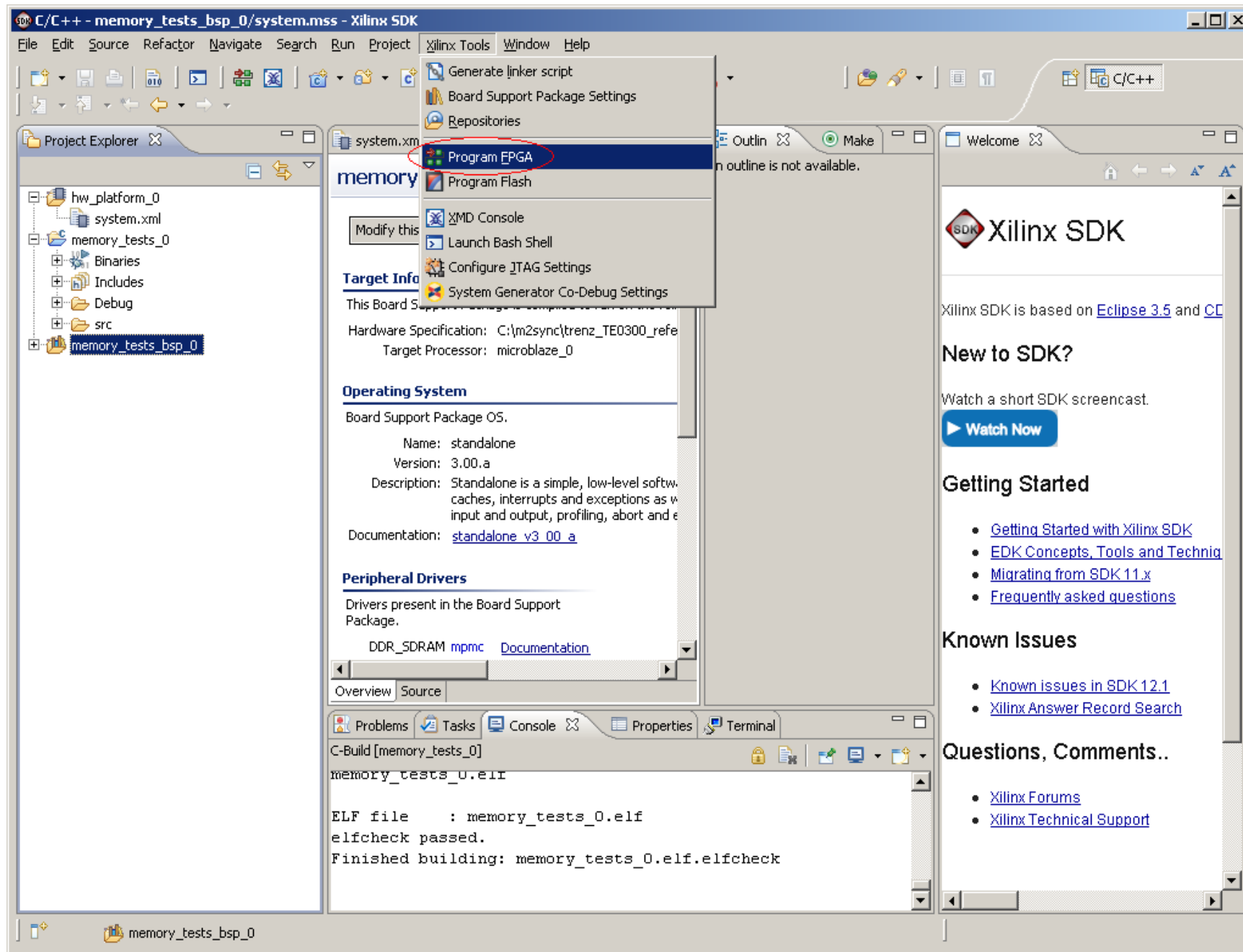
keep default BSP project name
memory_tests_bsp_0 and click Finish



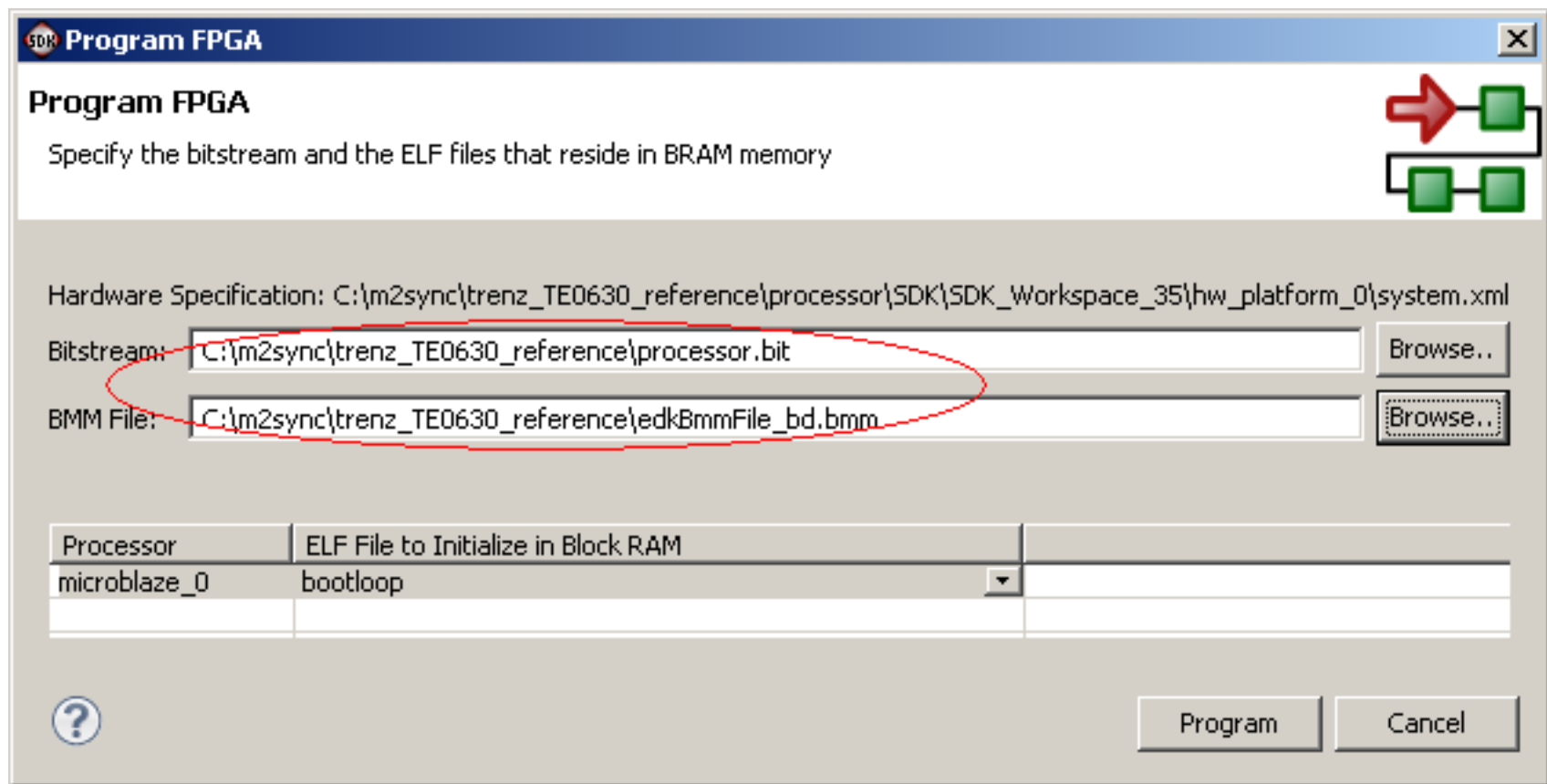
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



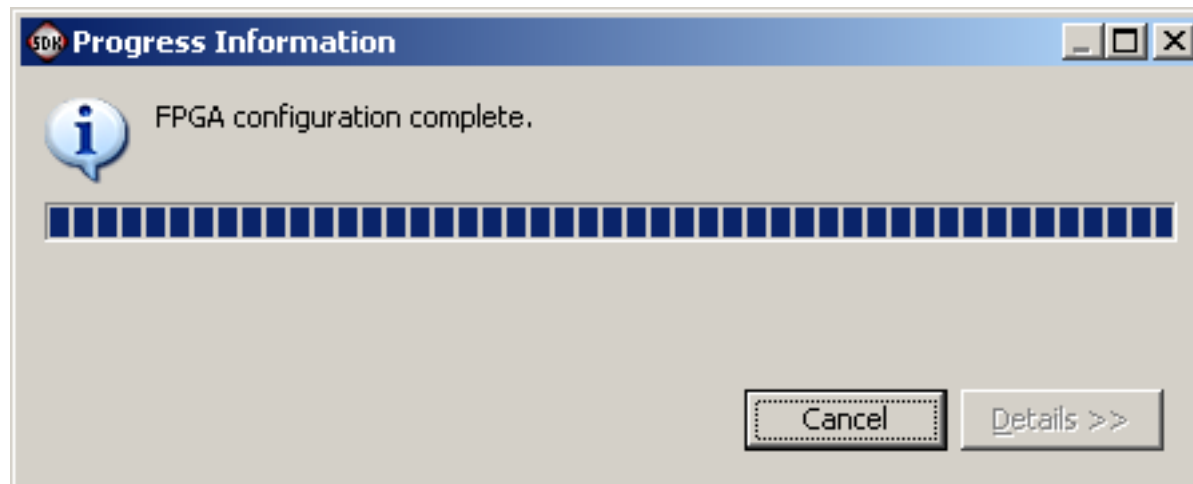
from standalone section apply mdm_0 to stdin and
stdout then click OK



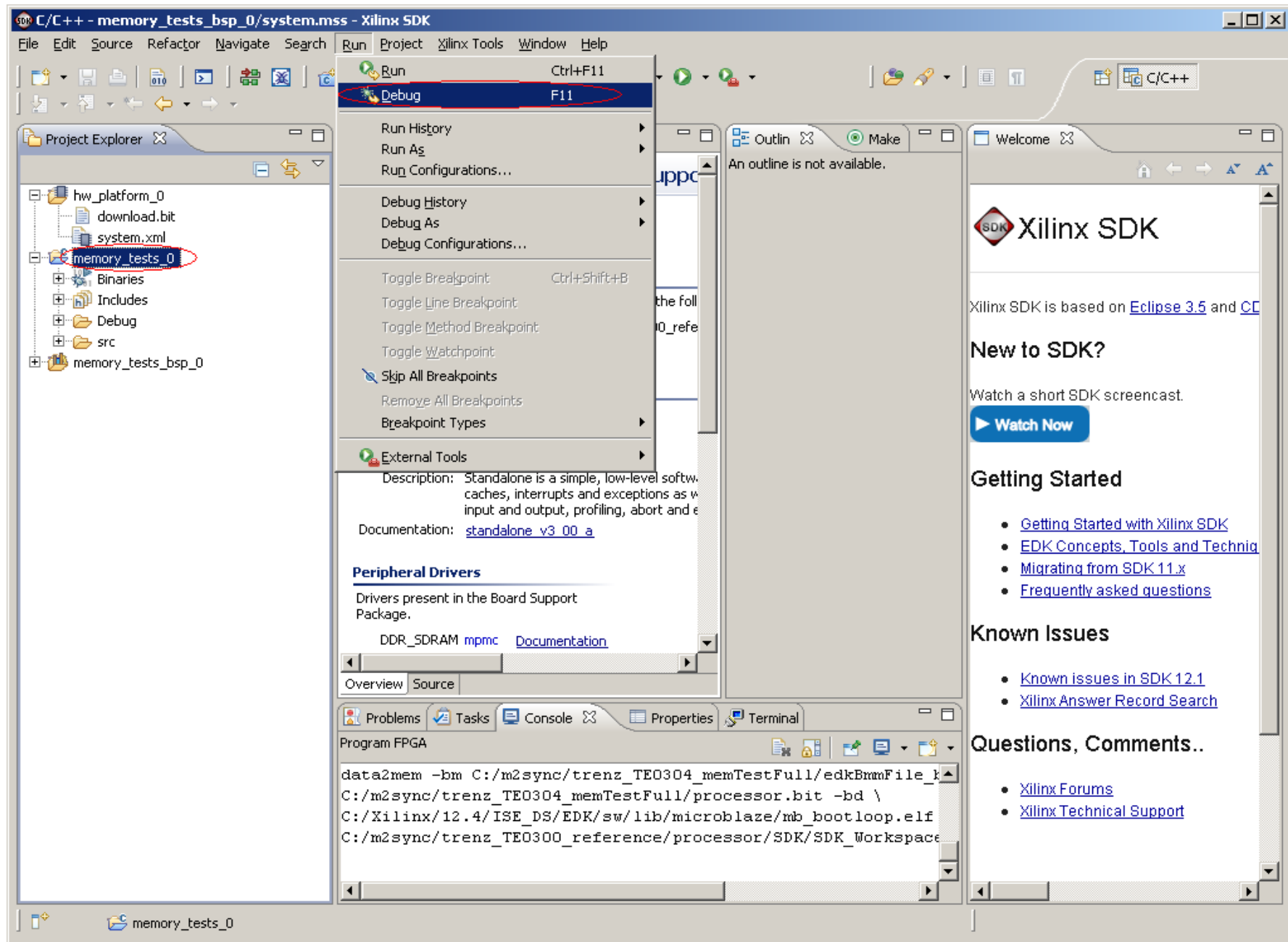
connect the prototype board TE0300 and choose
Program FPGA from menu



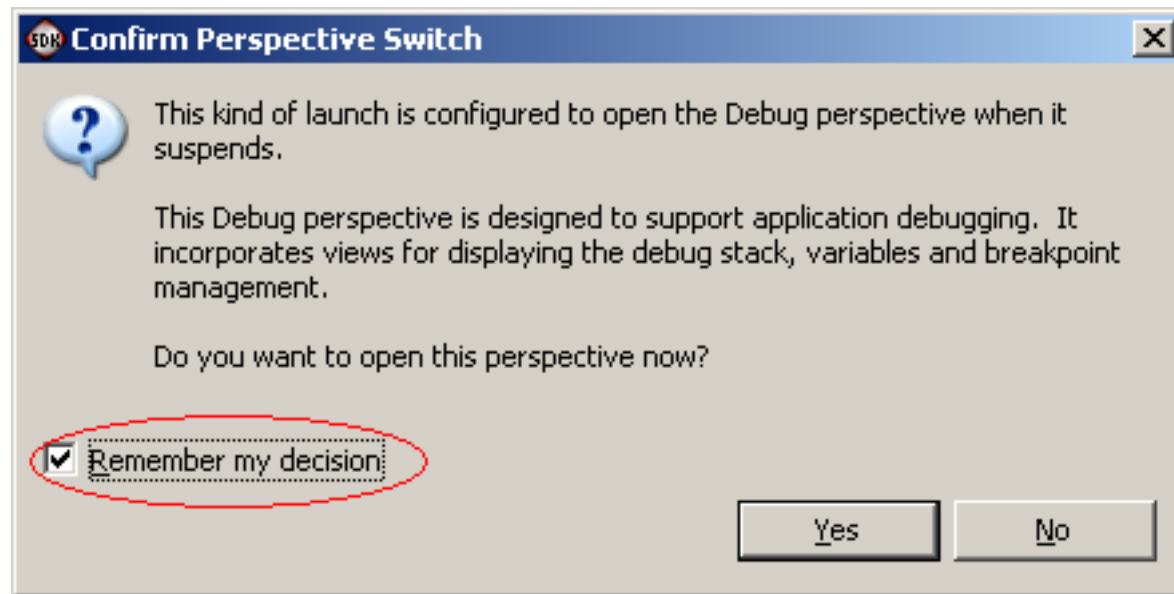
provide correct Bistream and BMM files then click
Program



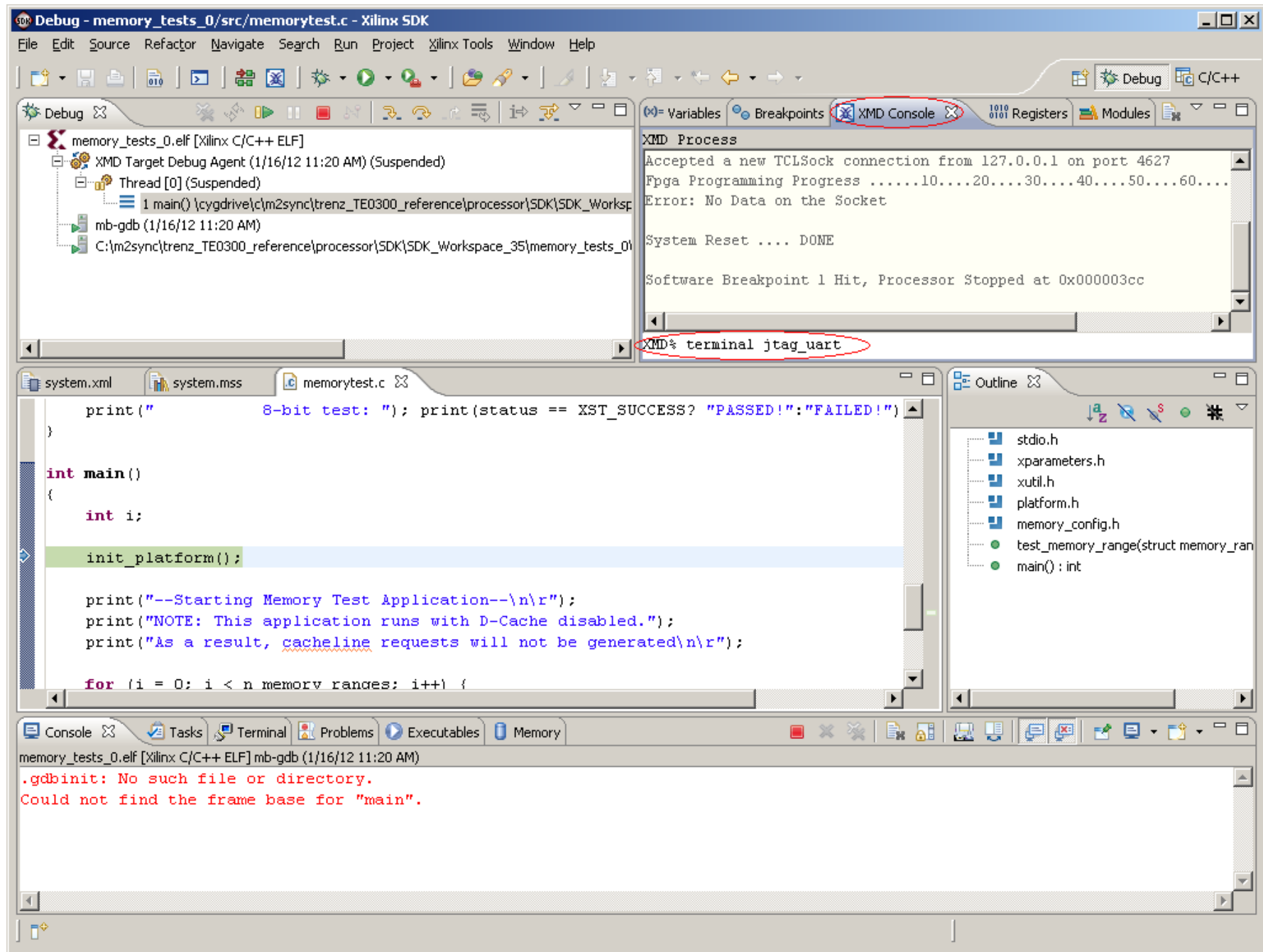
wait for FPGA programming completion



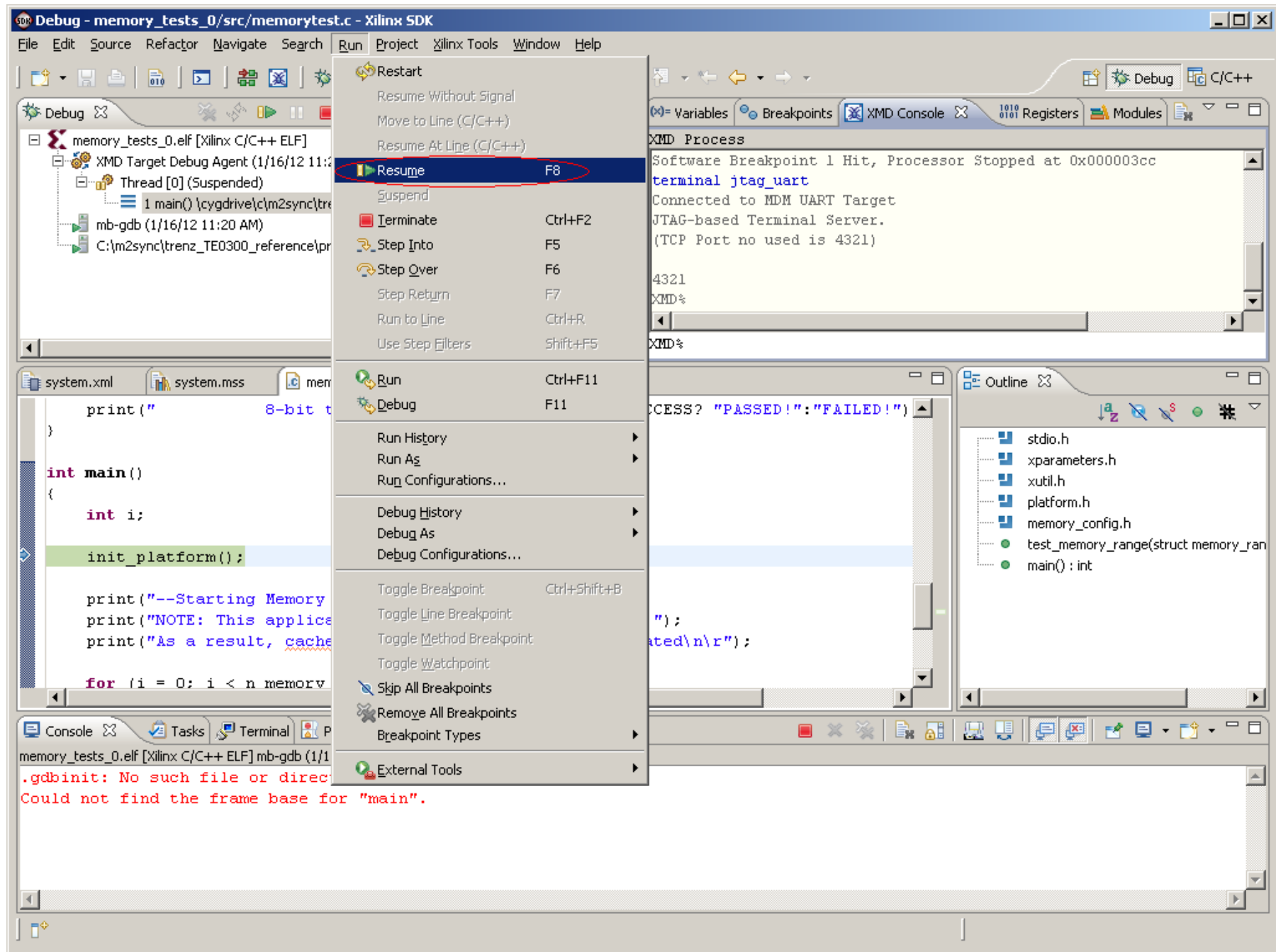
step on memory_tests_0 application and choose
Debug menu



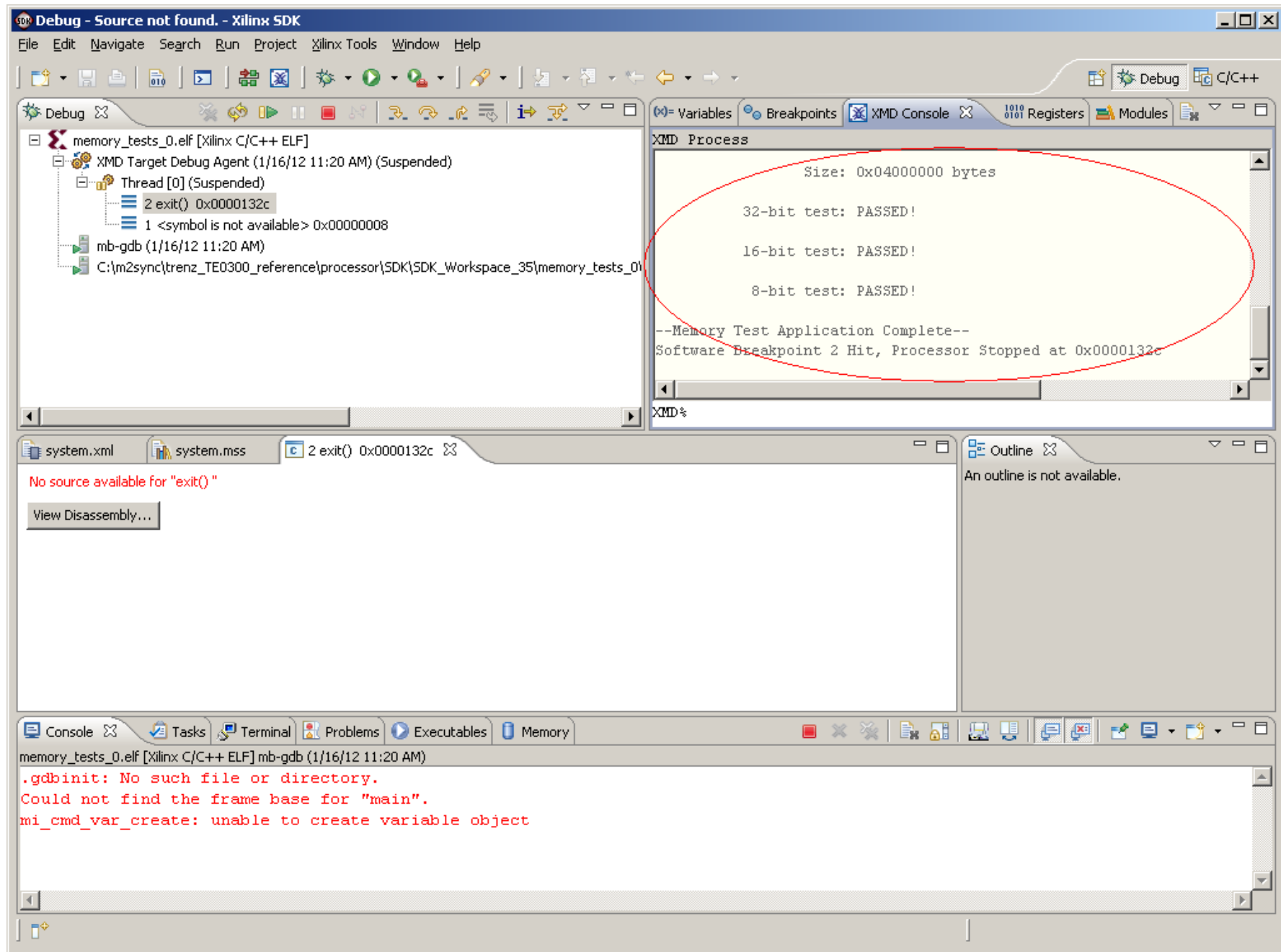
choose remember decision and confirm switching to Debug design by clicking Yes button



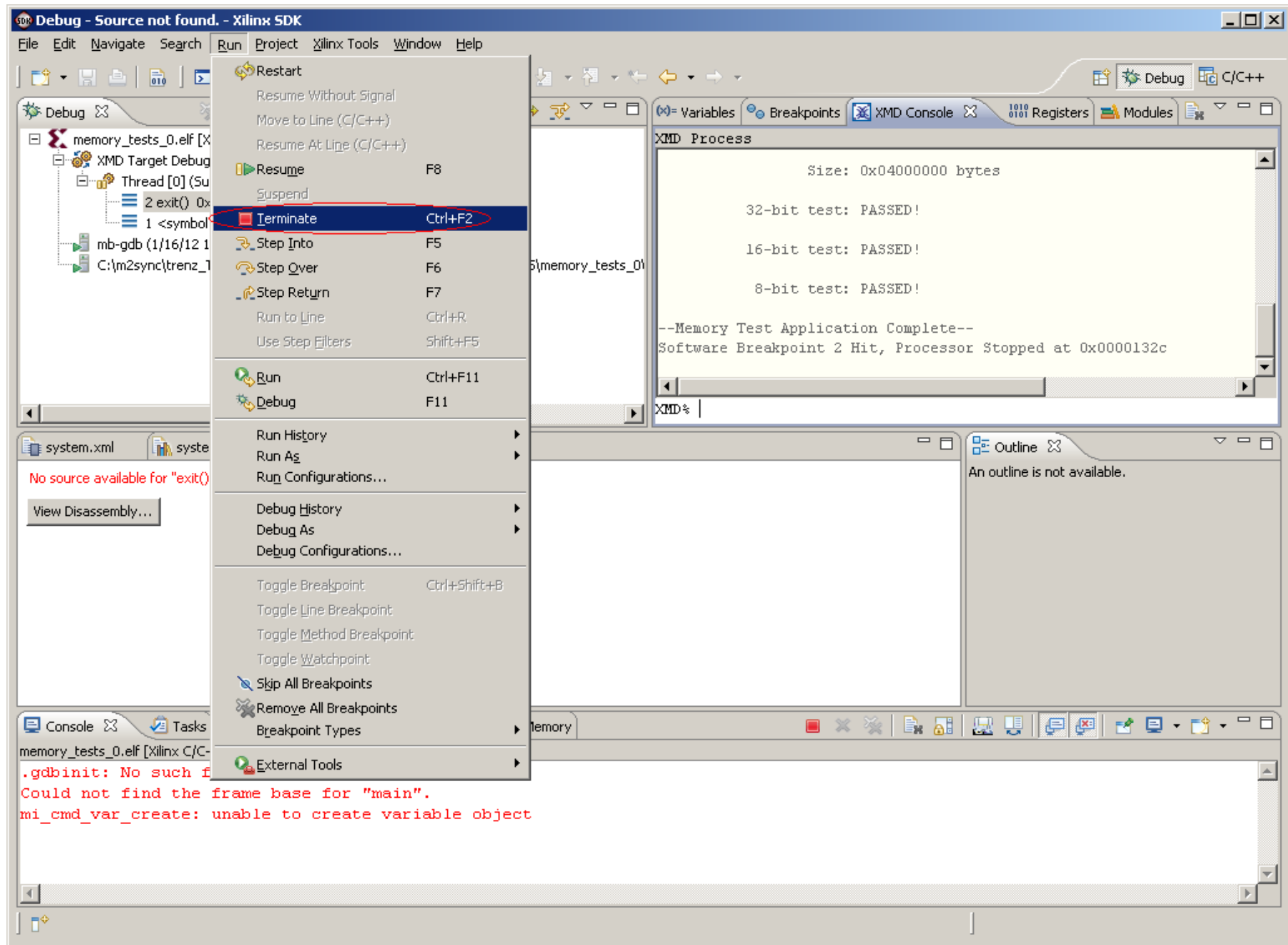
switch to XMD Console tab and type command
"terminal jtag_uart"



resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application

TE0630 board configuration complete

external memory configuration
confirmed with test application