TE0600 platform

reference project creation sequence

PLB bus based

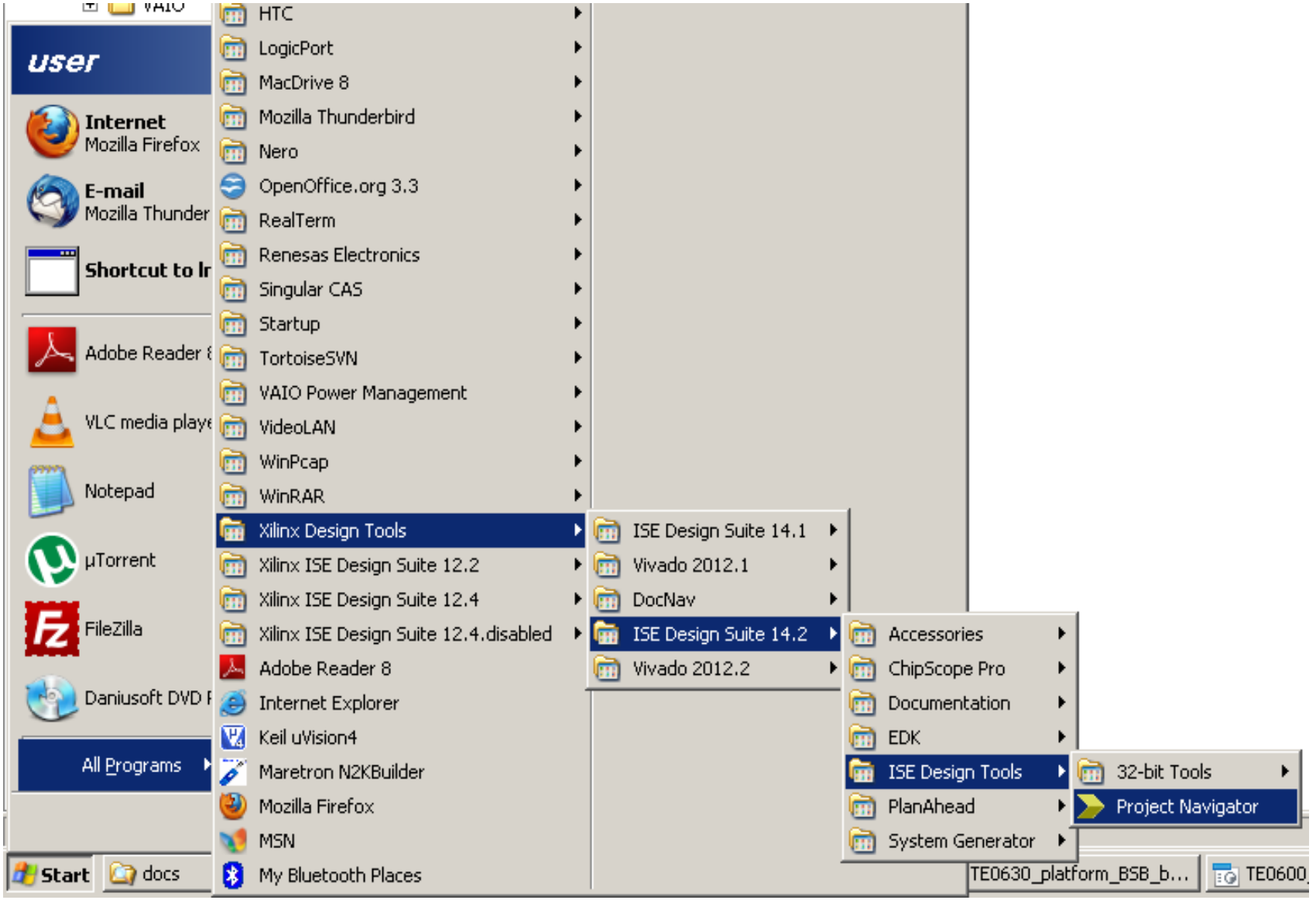
Special Note:

Make sure BSB files are copied into
\Xilinx\14.2\ISE_DS\EDK\data\board

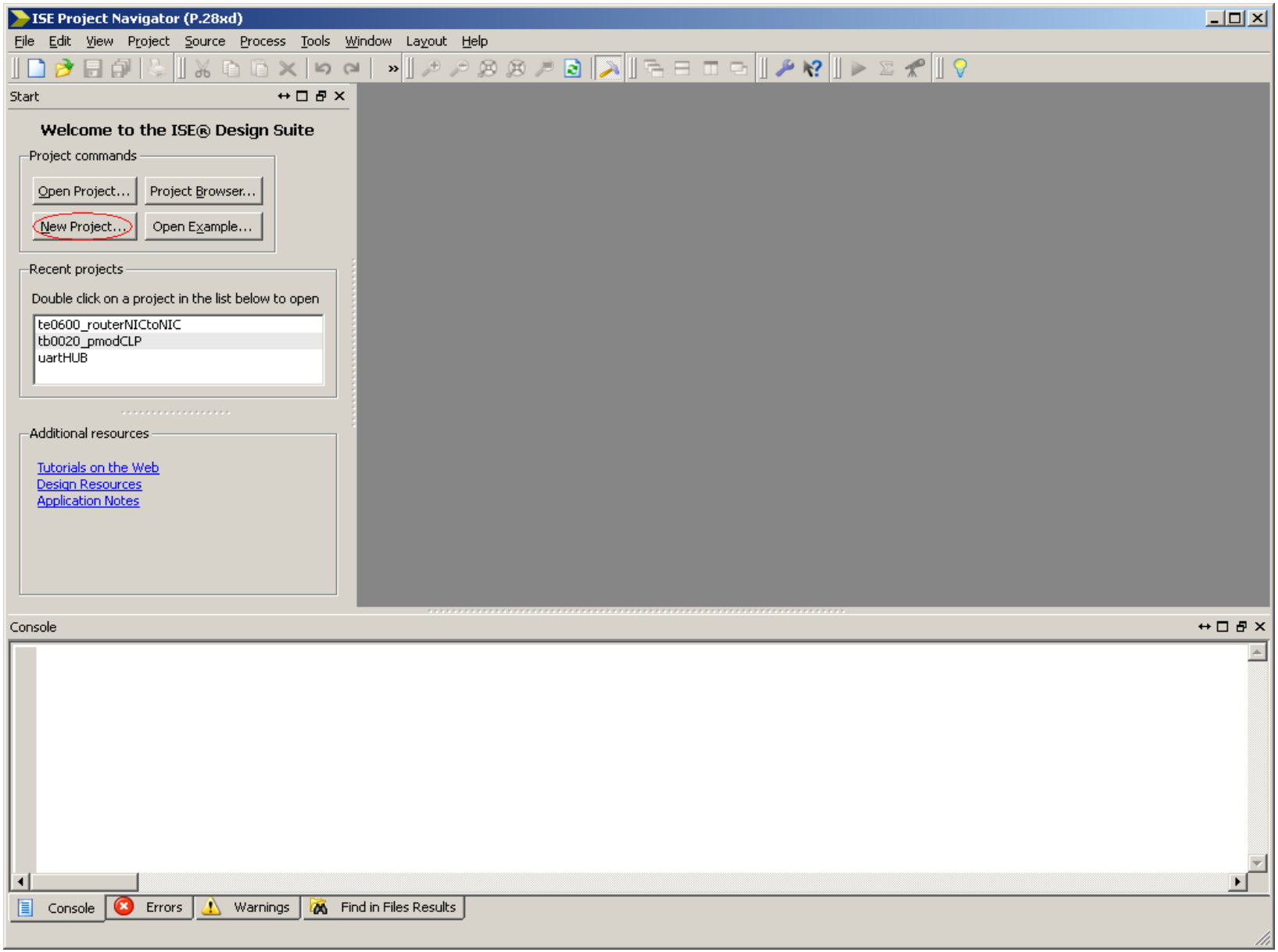
Make sure private pcores are copied into
\Xilinx\14.2\ISE_DS\EDK\data\wizards\BsbCores\pcores

Before running this manual

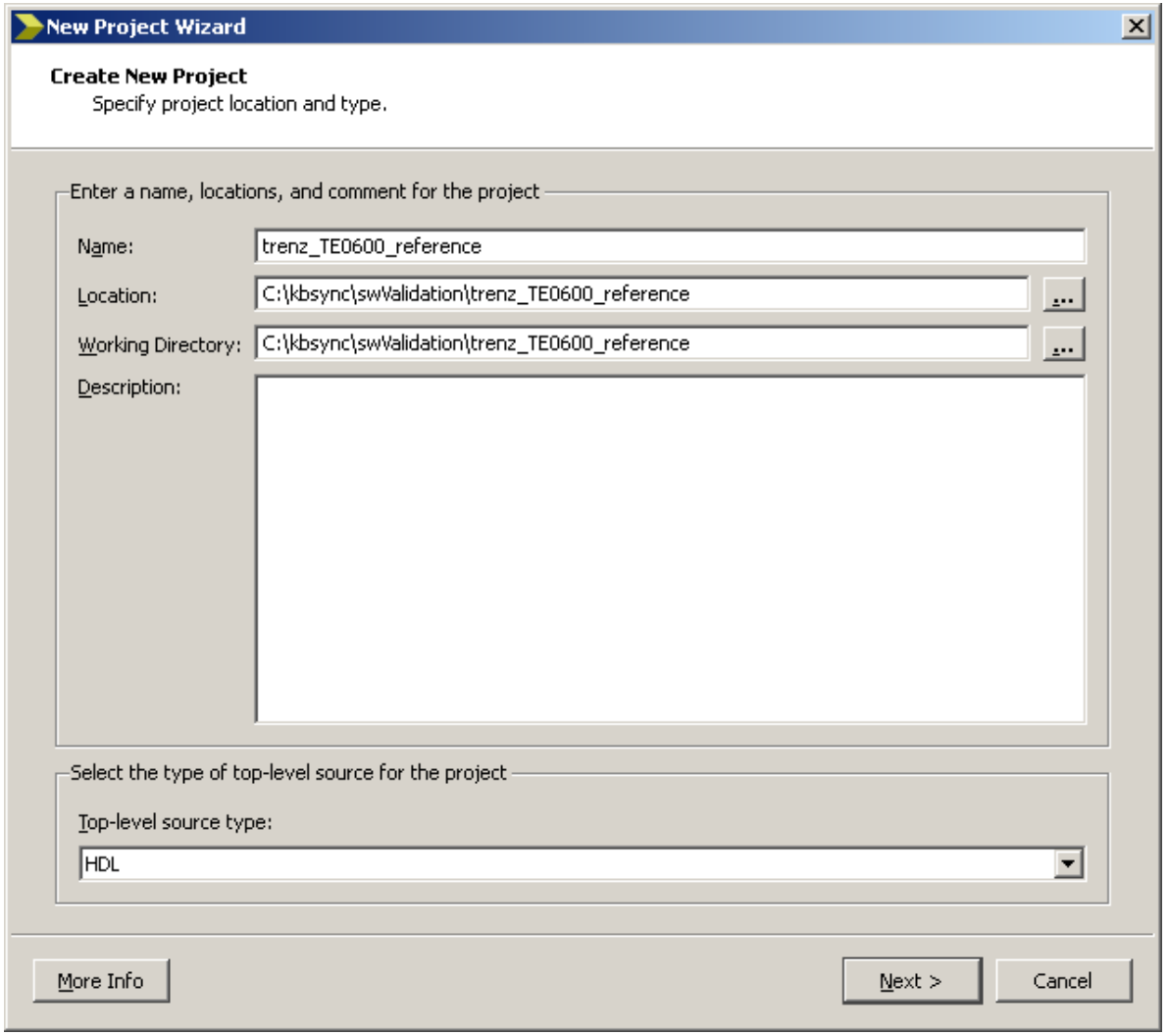
start Xilinx ISE 14 Project Navigator



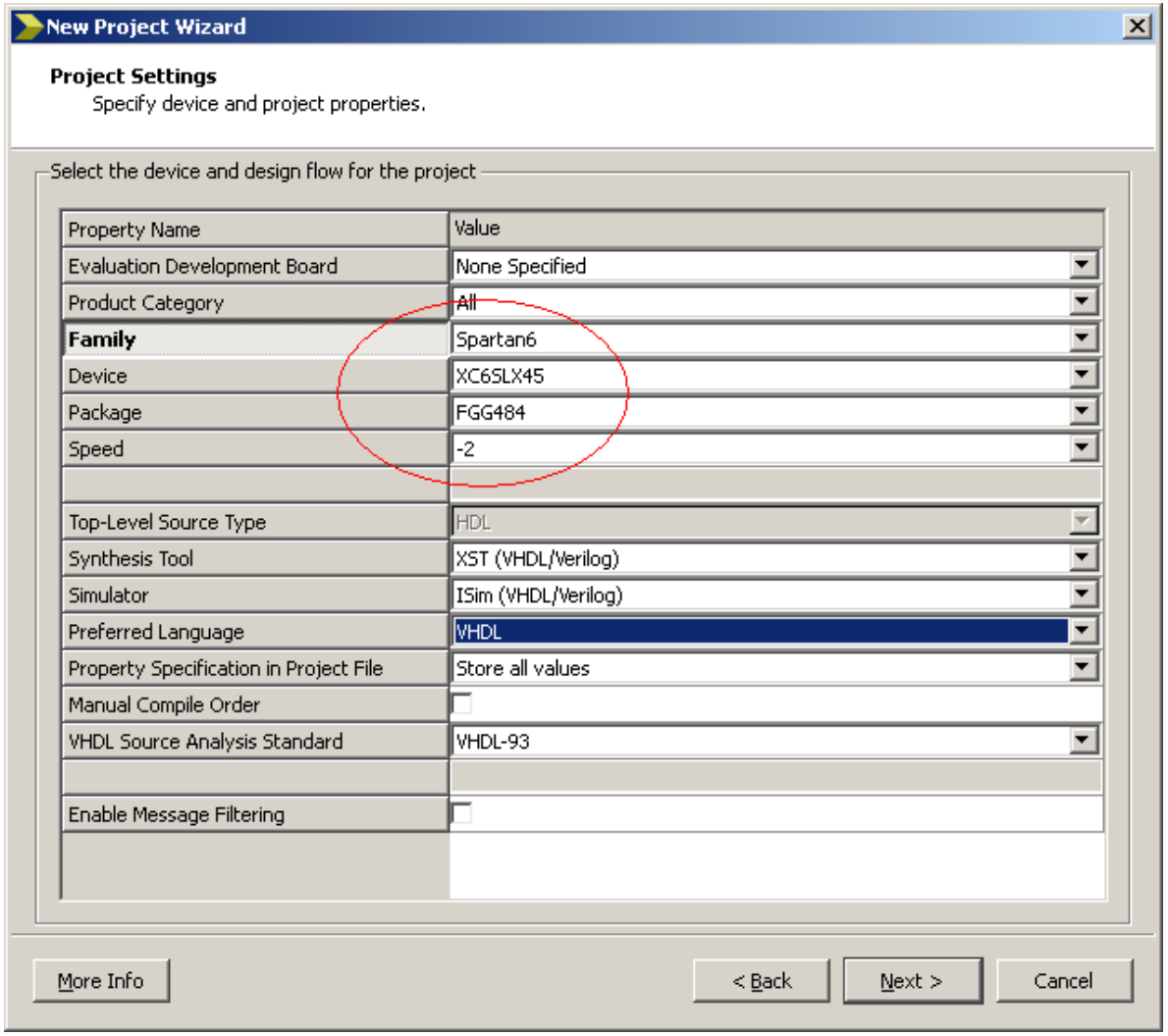
click button to create a new project



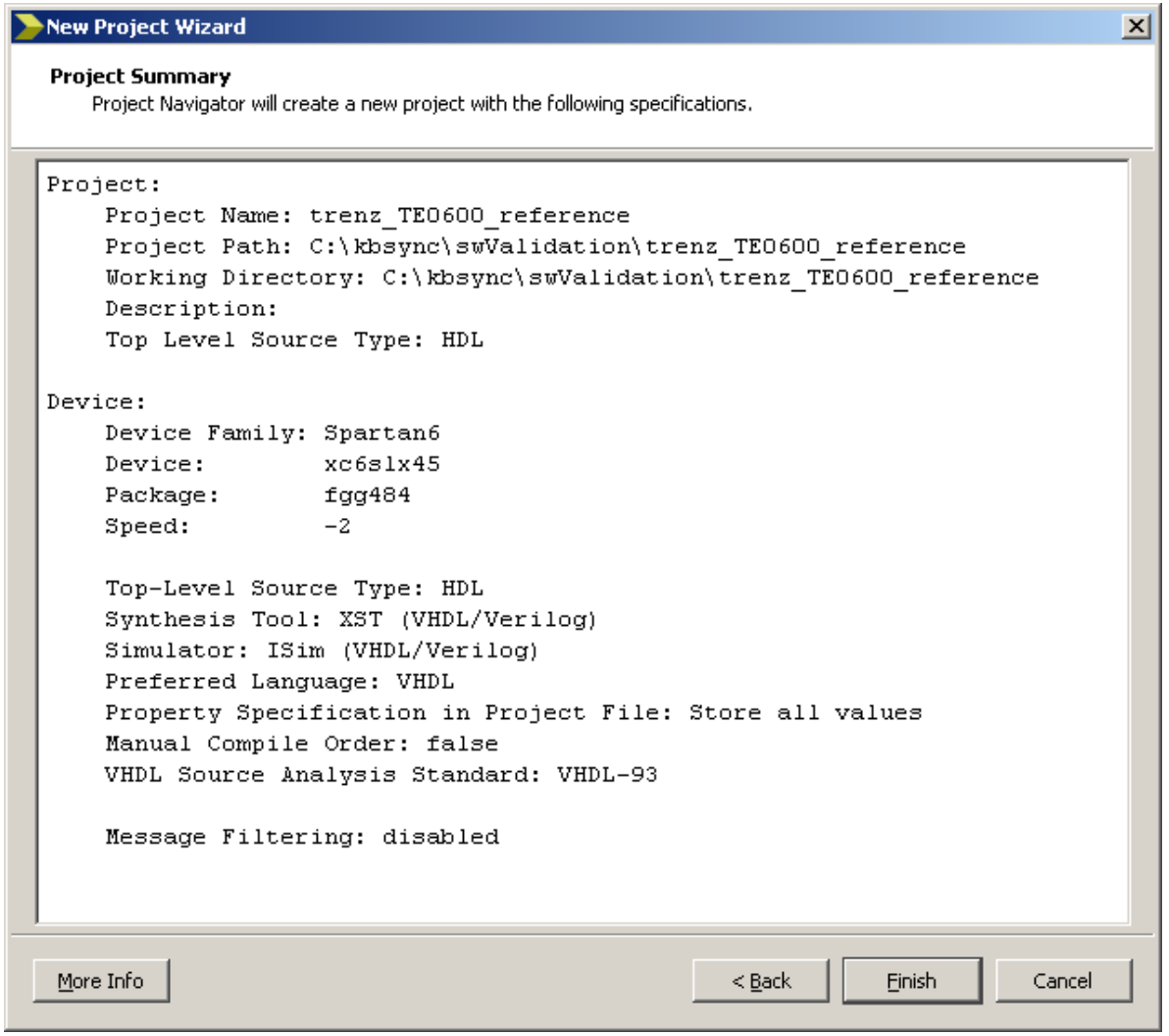
choose project name, then click Next



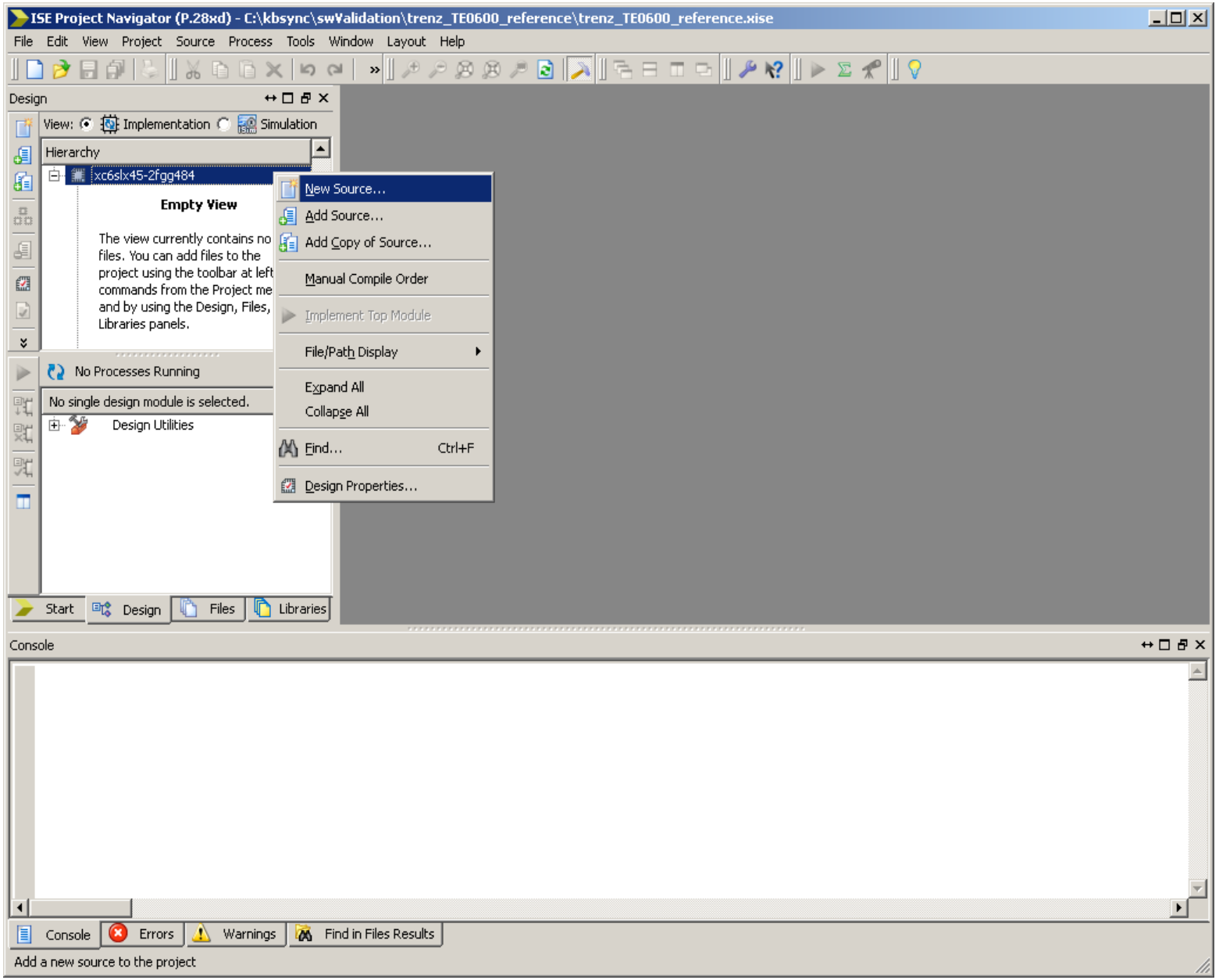
provide correct Family, Device, Package and Speed,
then click Next



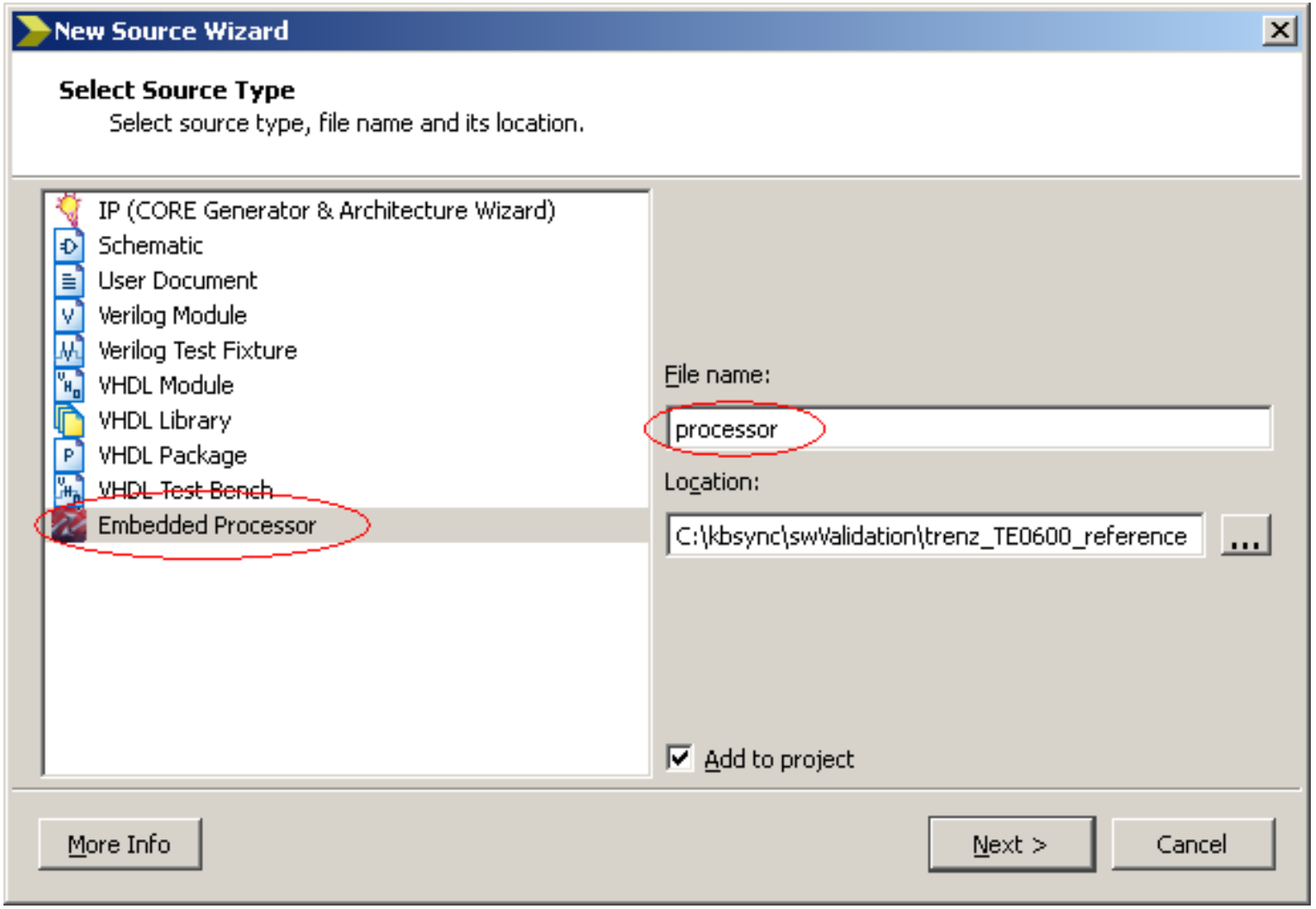
verify configuration and click Finish



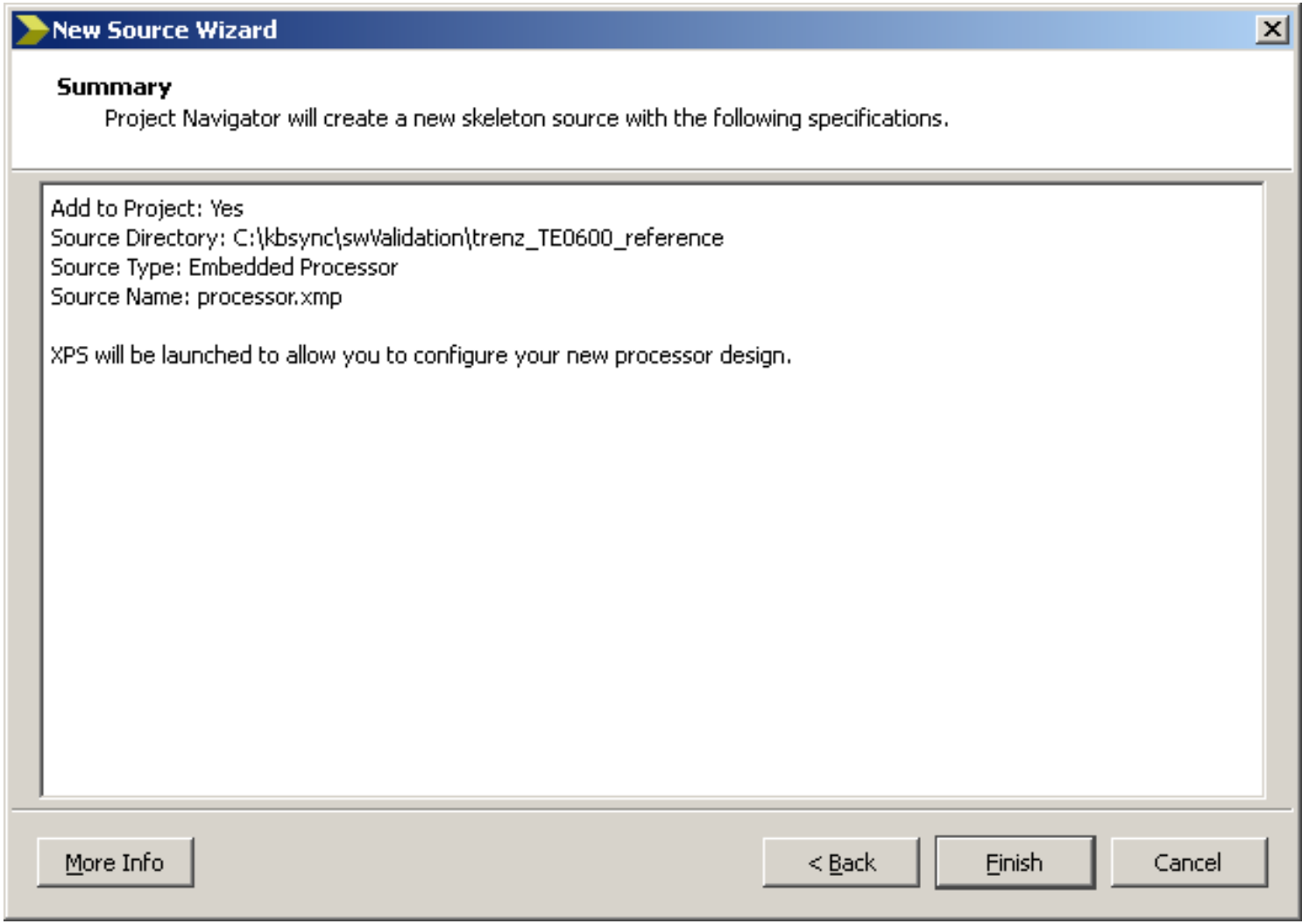
right button menu to add New Source



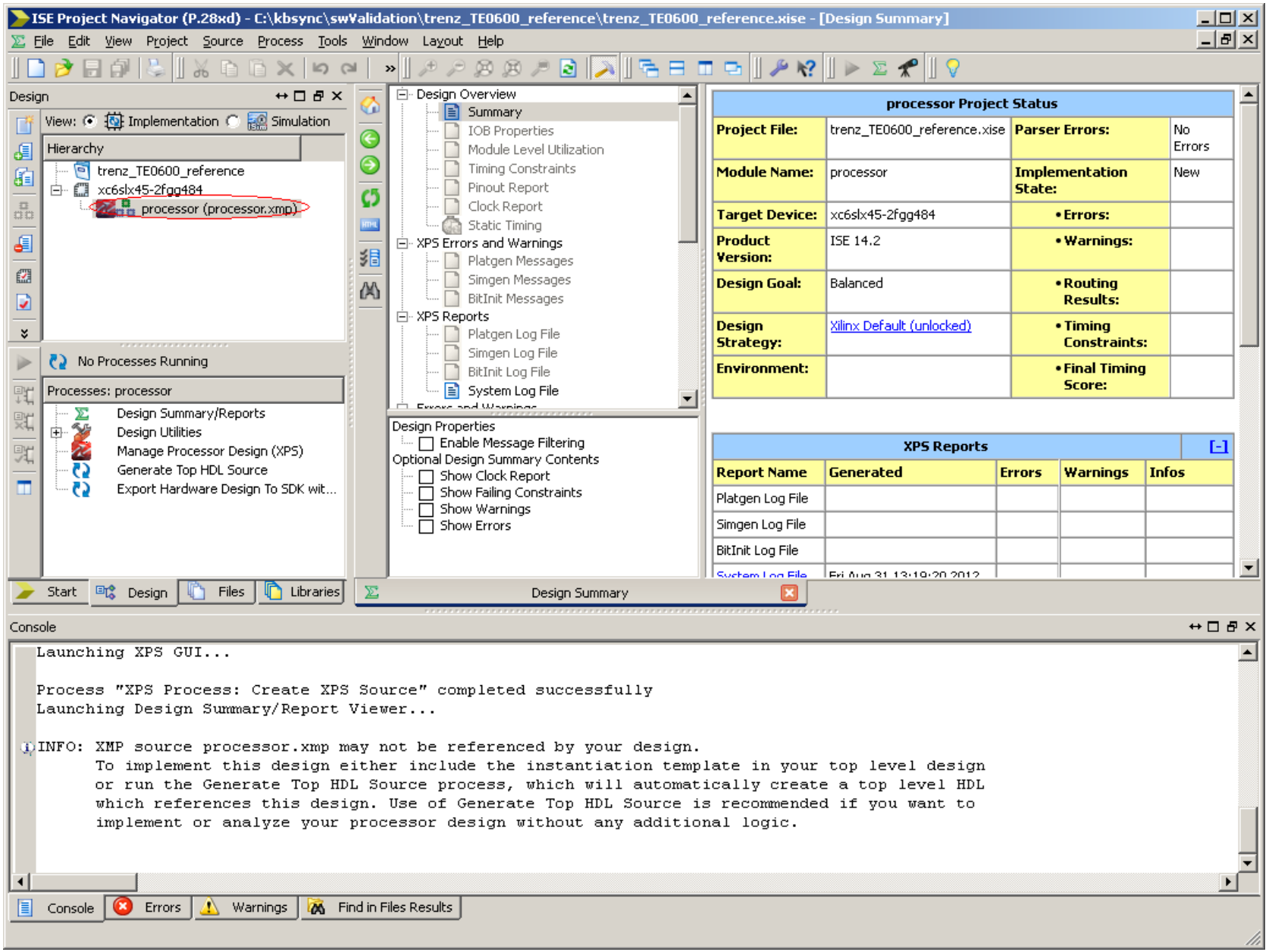
choose Embedded Processor, provide File name then click Next



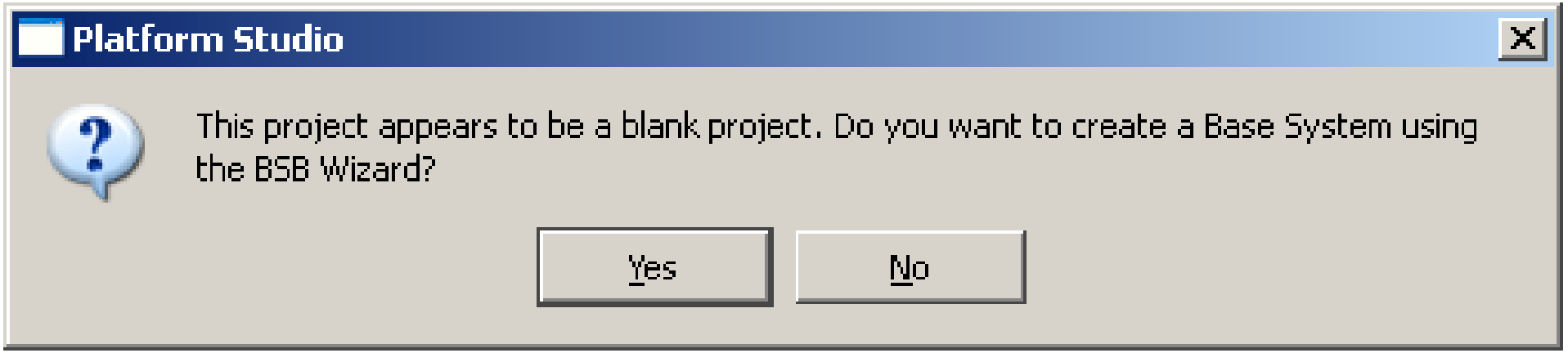
verify configuration then click Finish



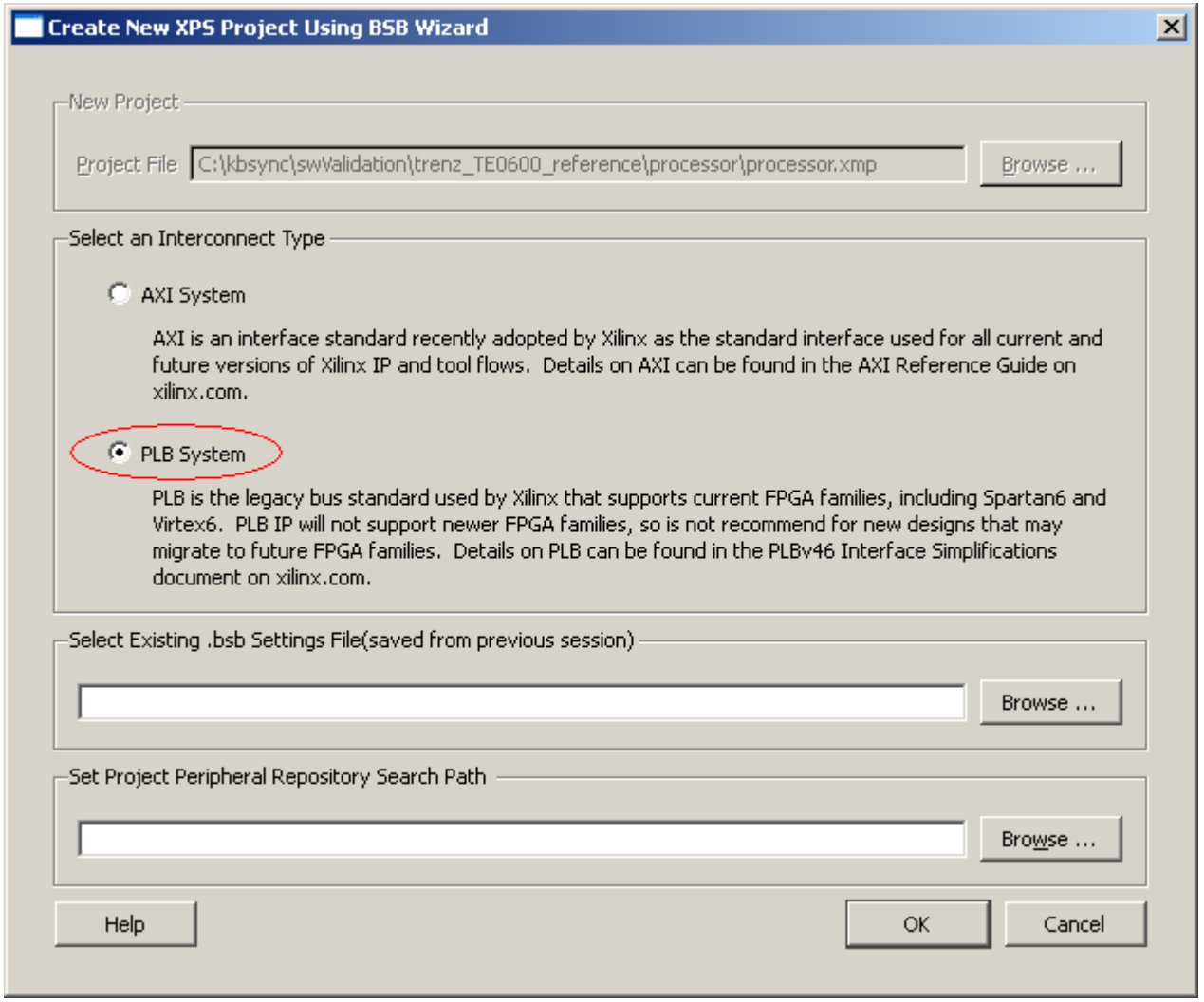
Double click on processor.xmp



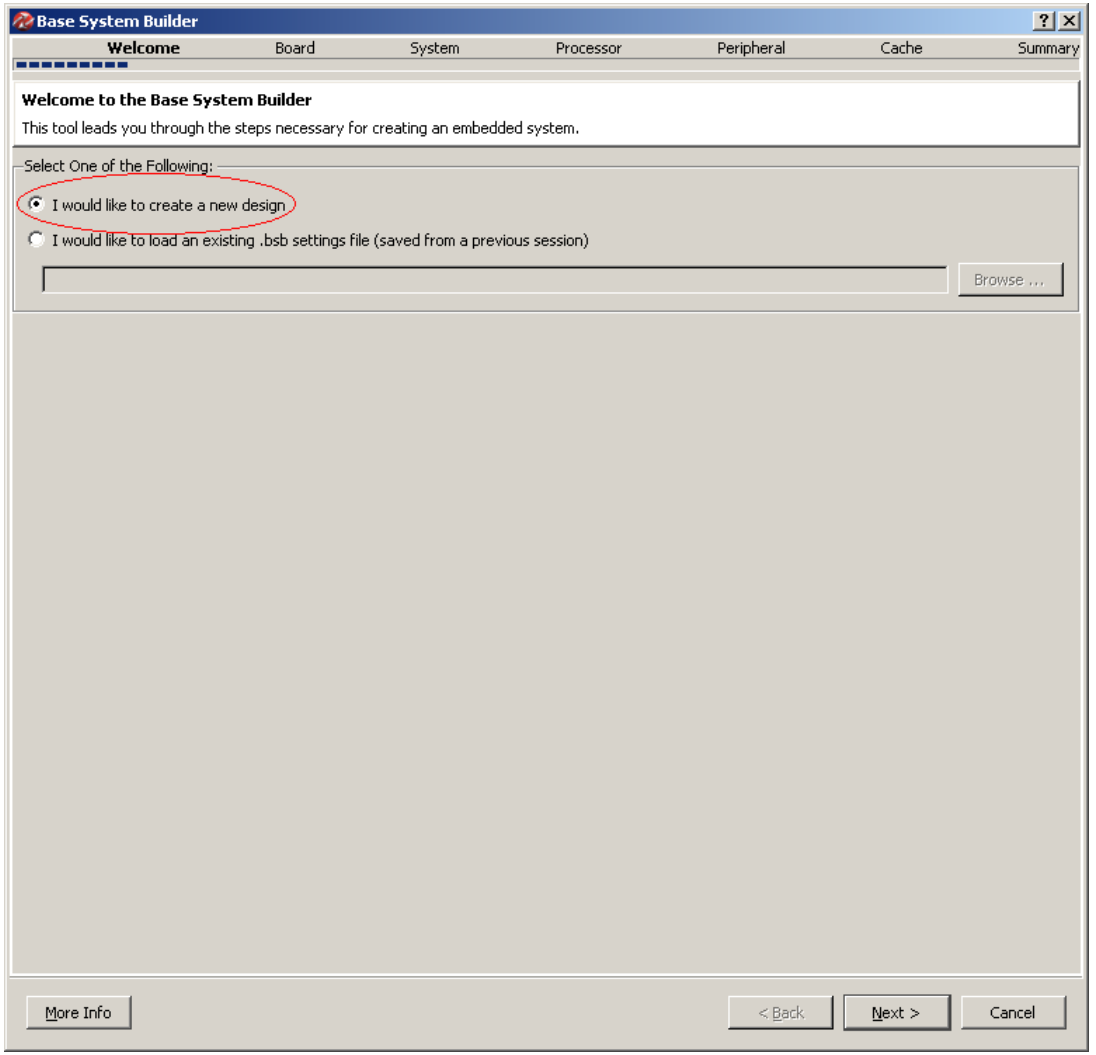
confirm Yes to launch BSB Wizard



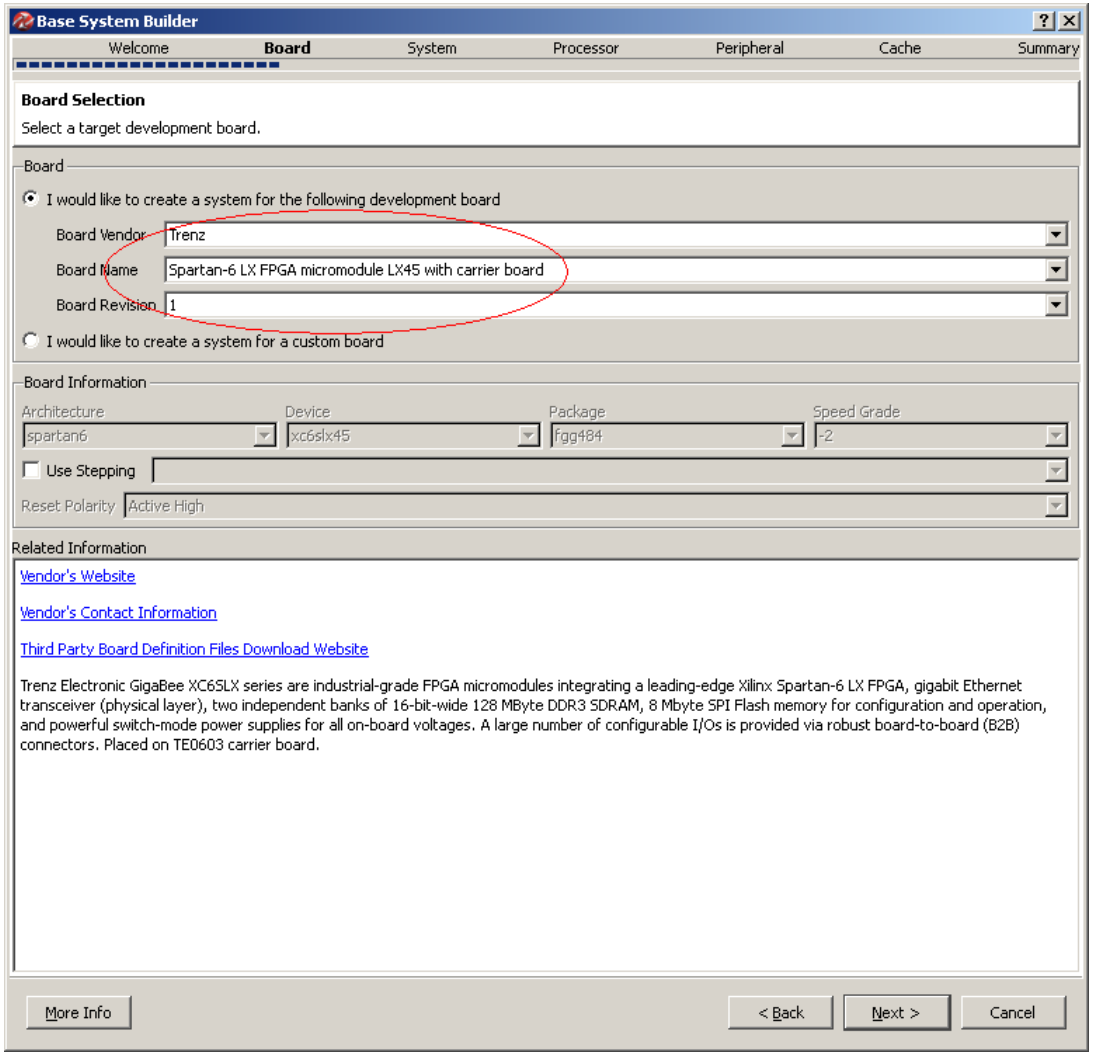
choose PLB system



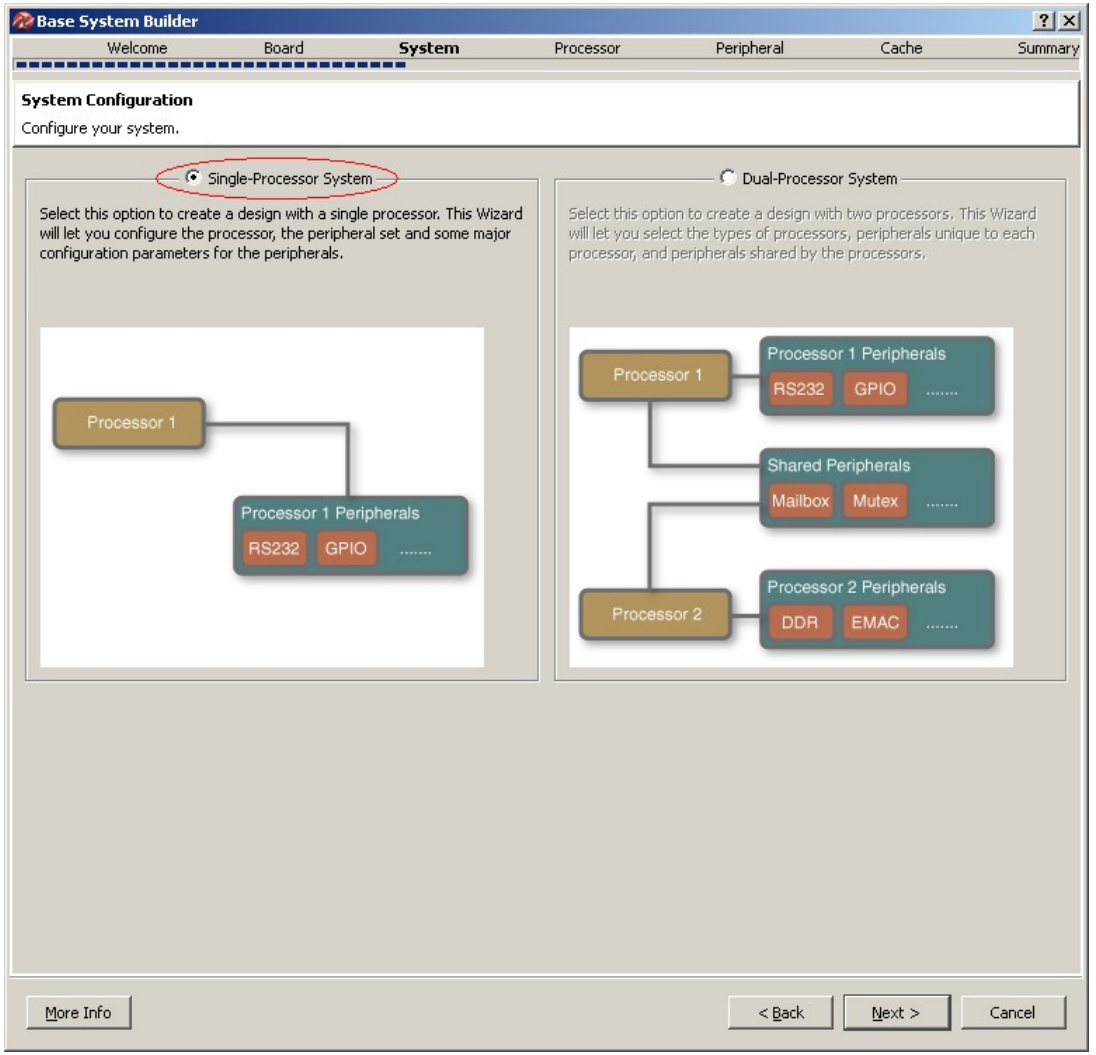
choose create new design then click Next



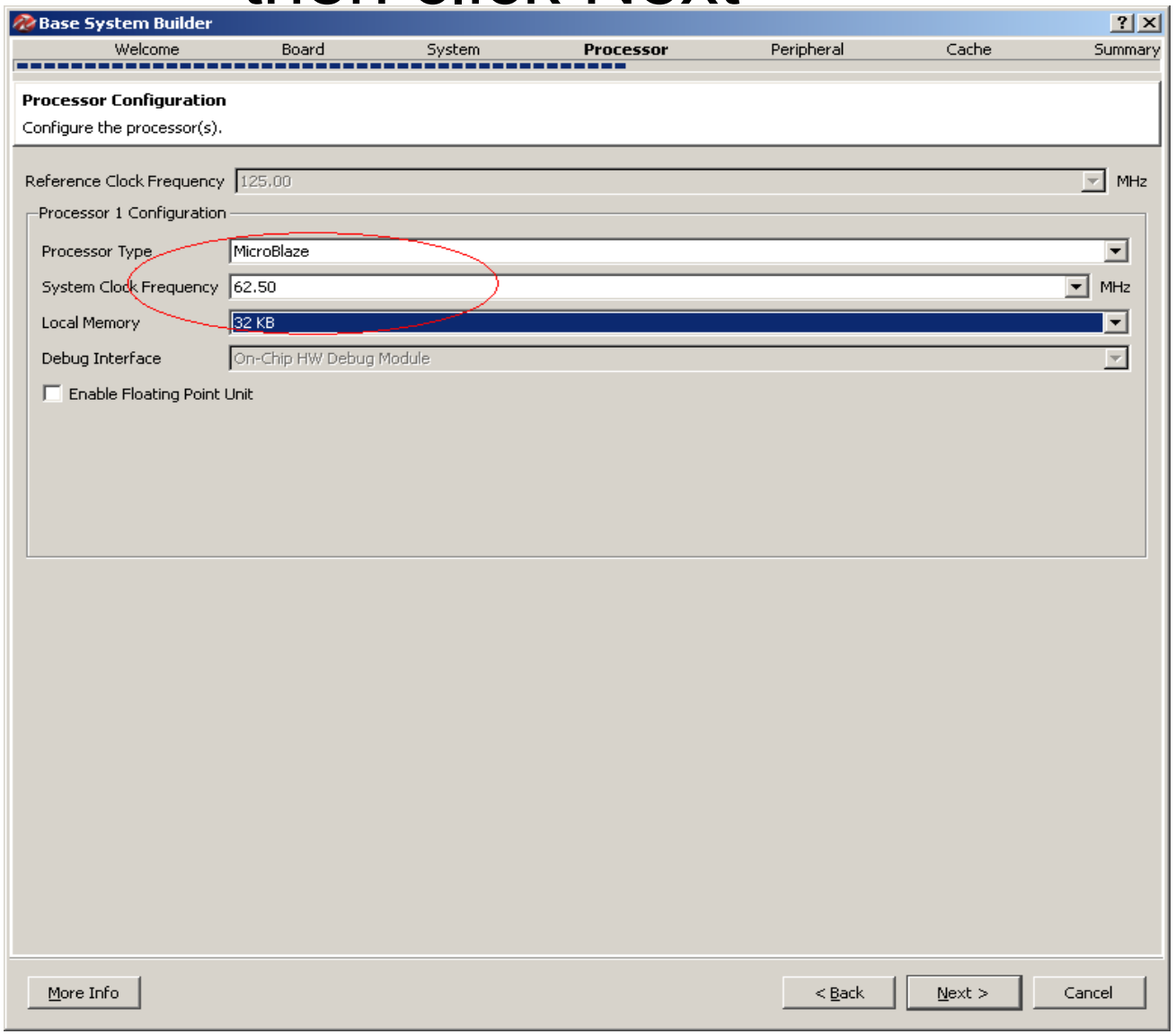
choose correct Vendor, Name and Revision then click Next



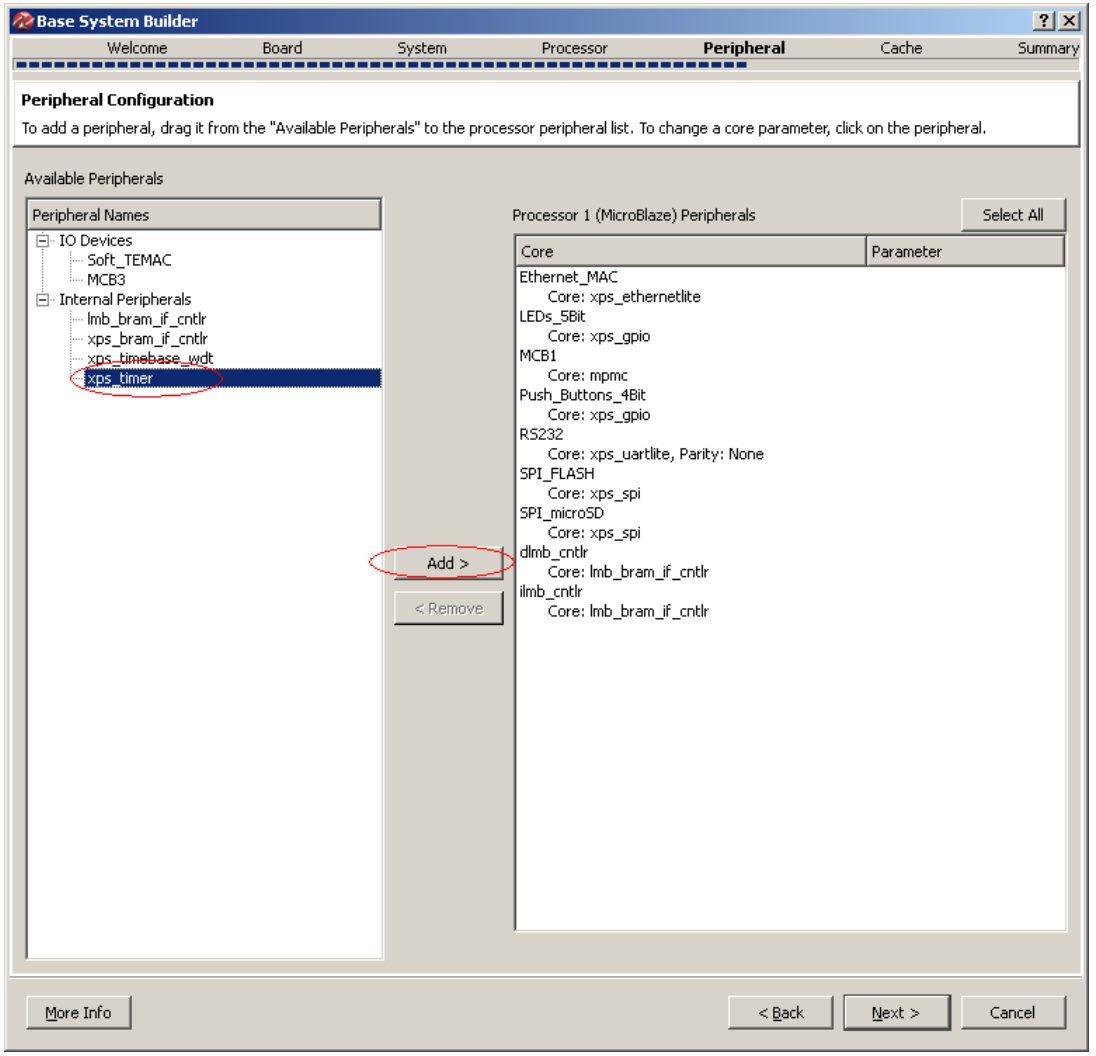
choose Single-Processor System then click Next



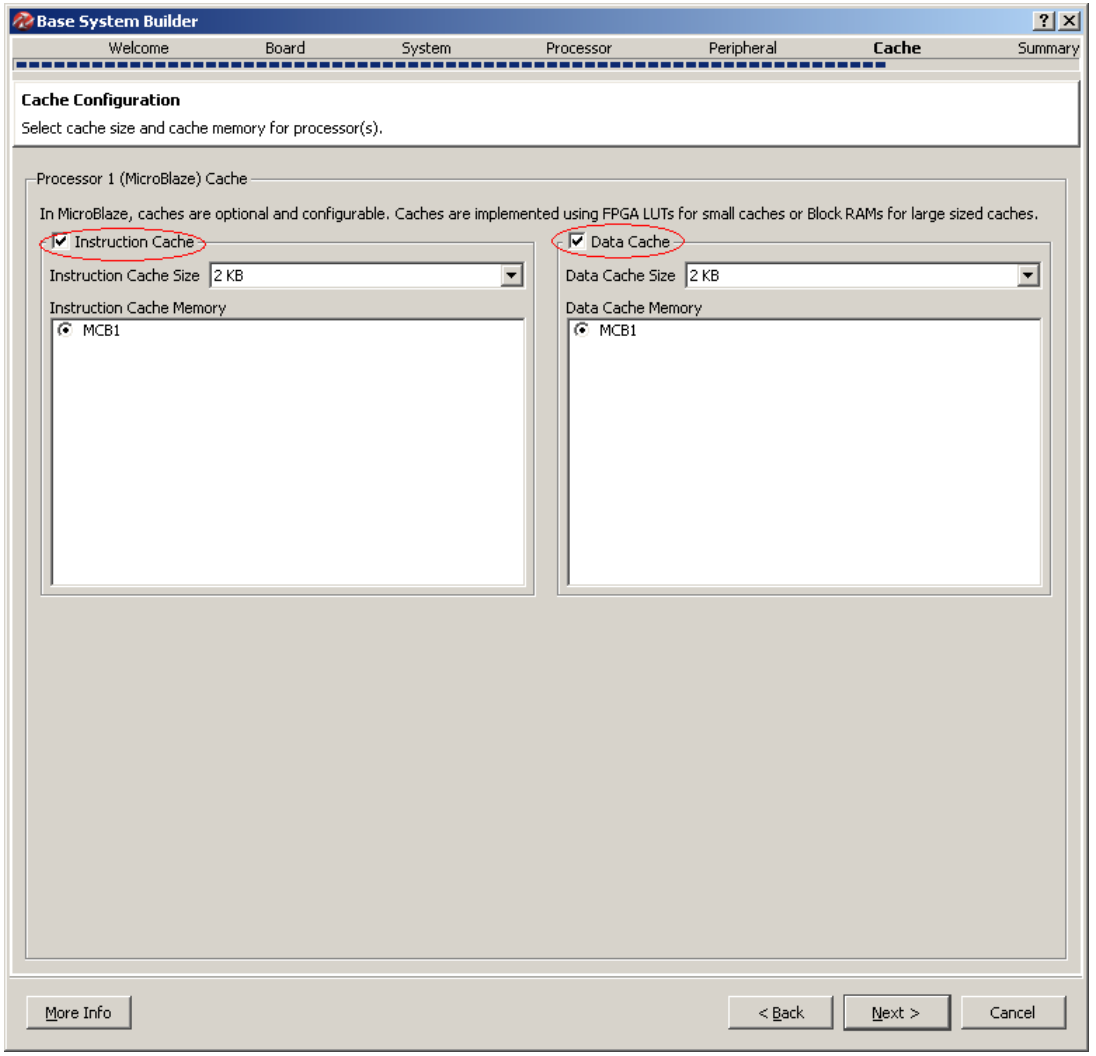
choose default Processor Type, System Clock Frequency (half of the reference) and Local Memory size (32 Kb)
then click Next



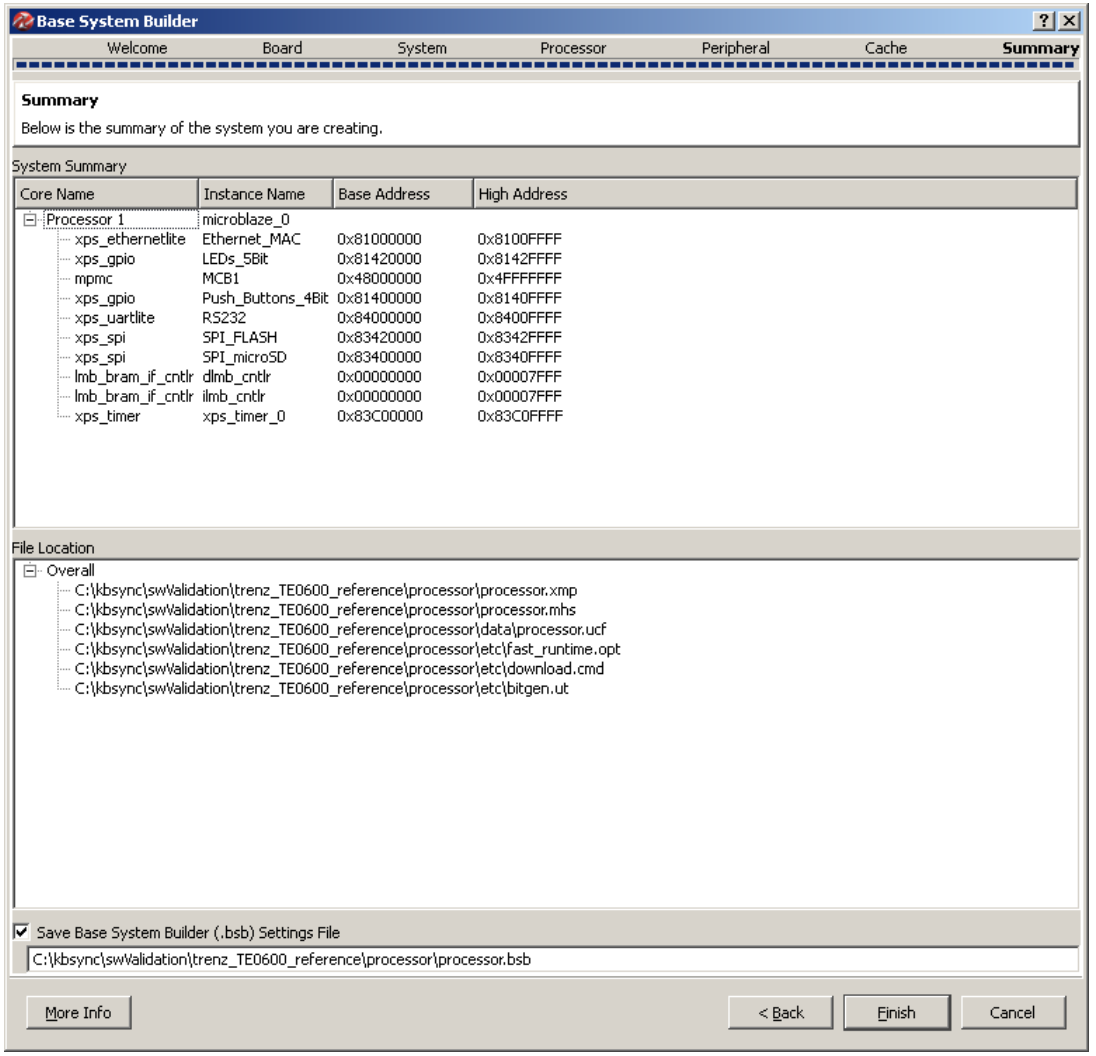
add xps_timer (XilKernel required), then click Next



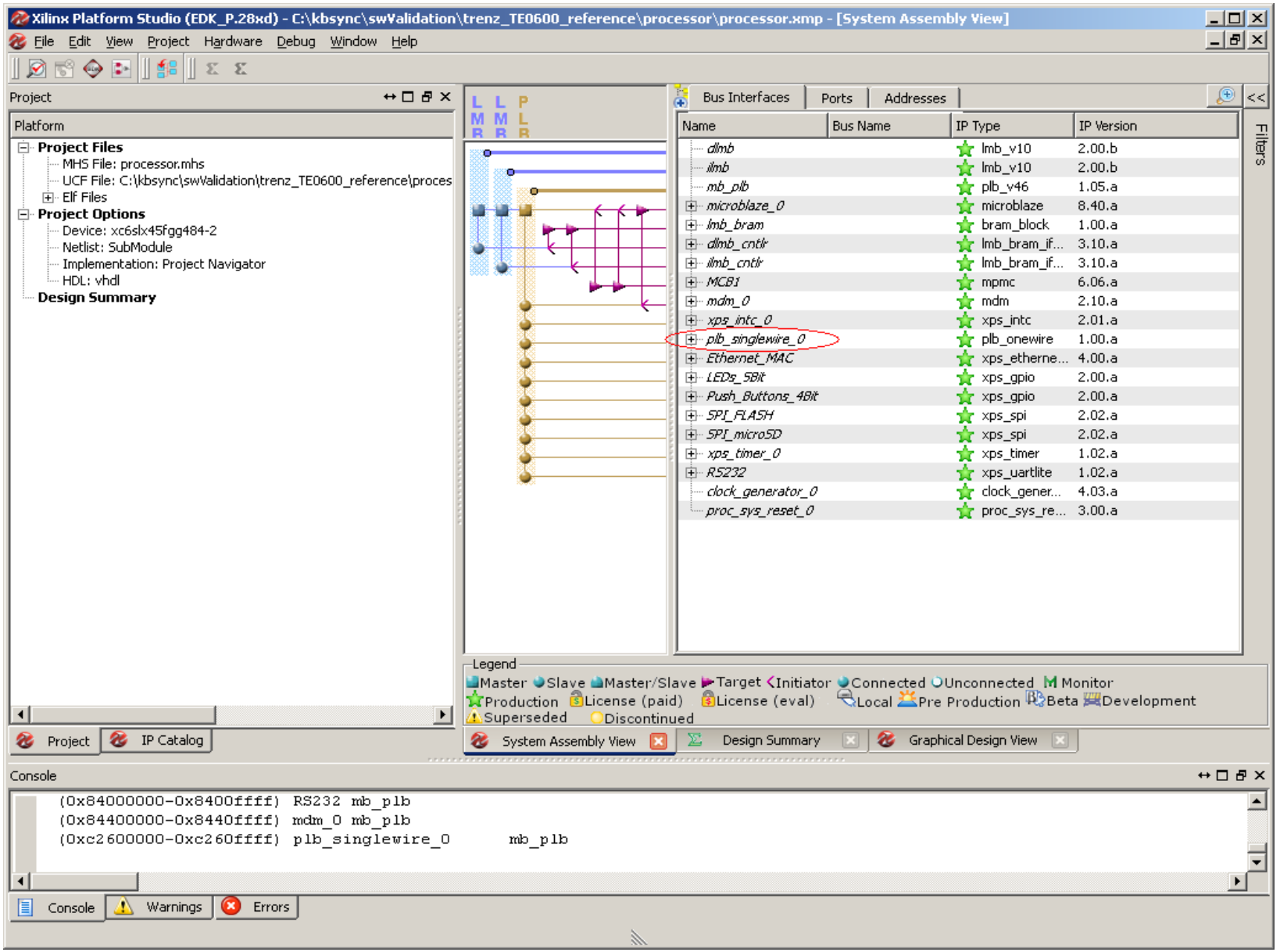
enable Instruction and Data Caches then click Next



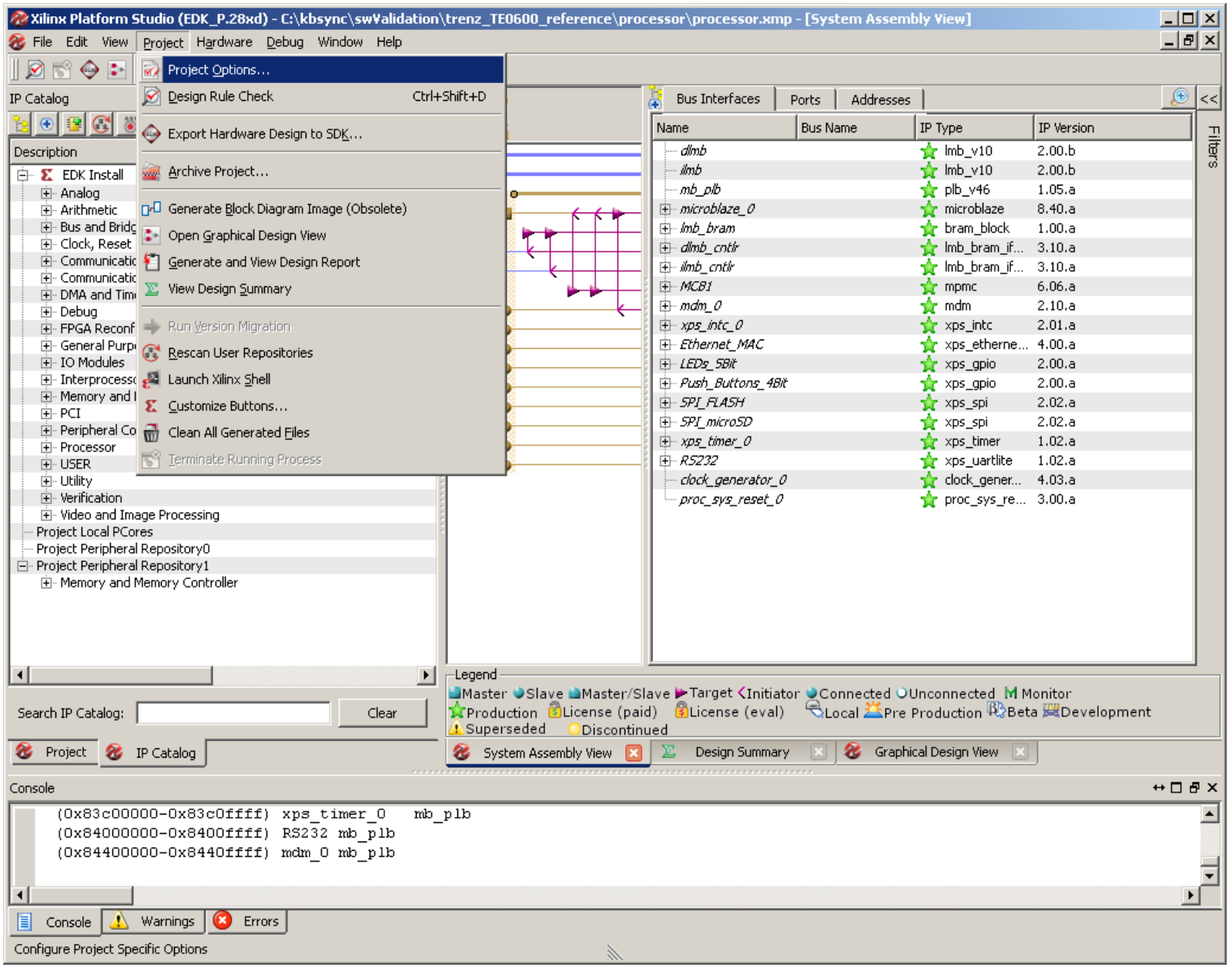
verify created configuration then click Finish



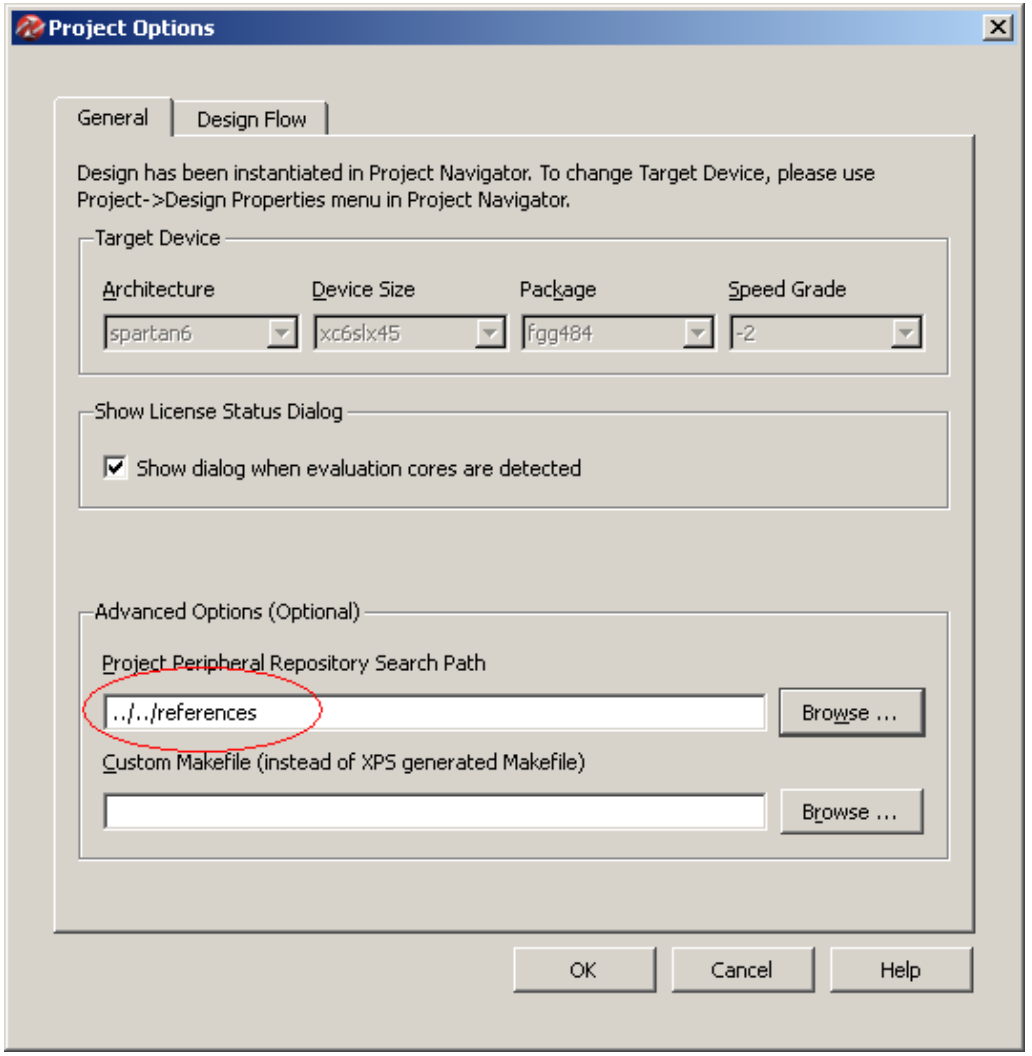
Verify singlewire pcore availability



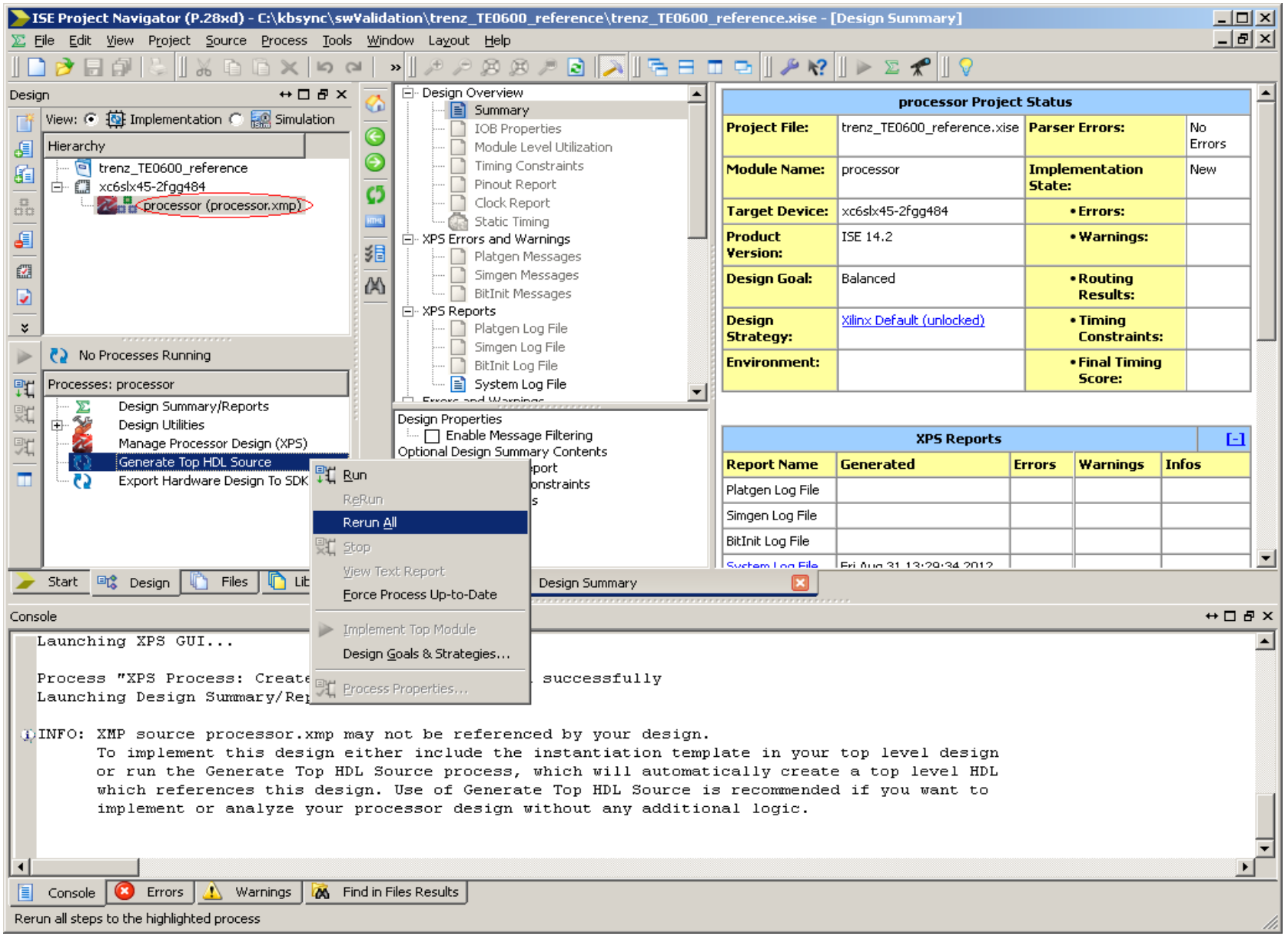
launch Project Options



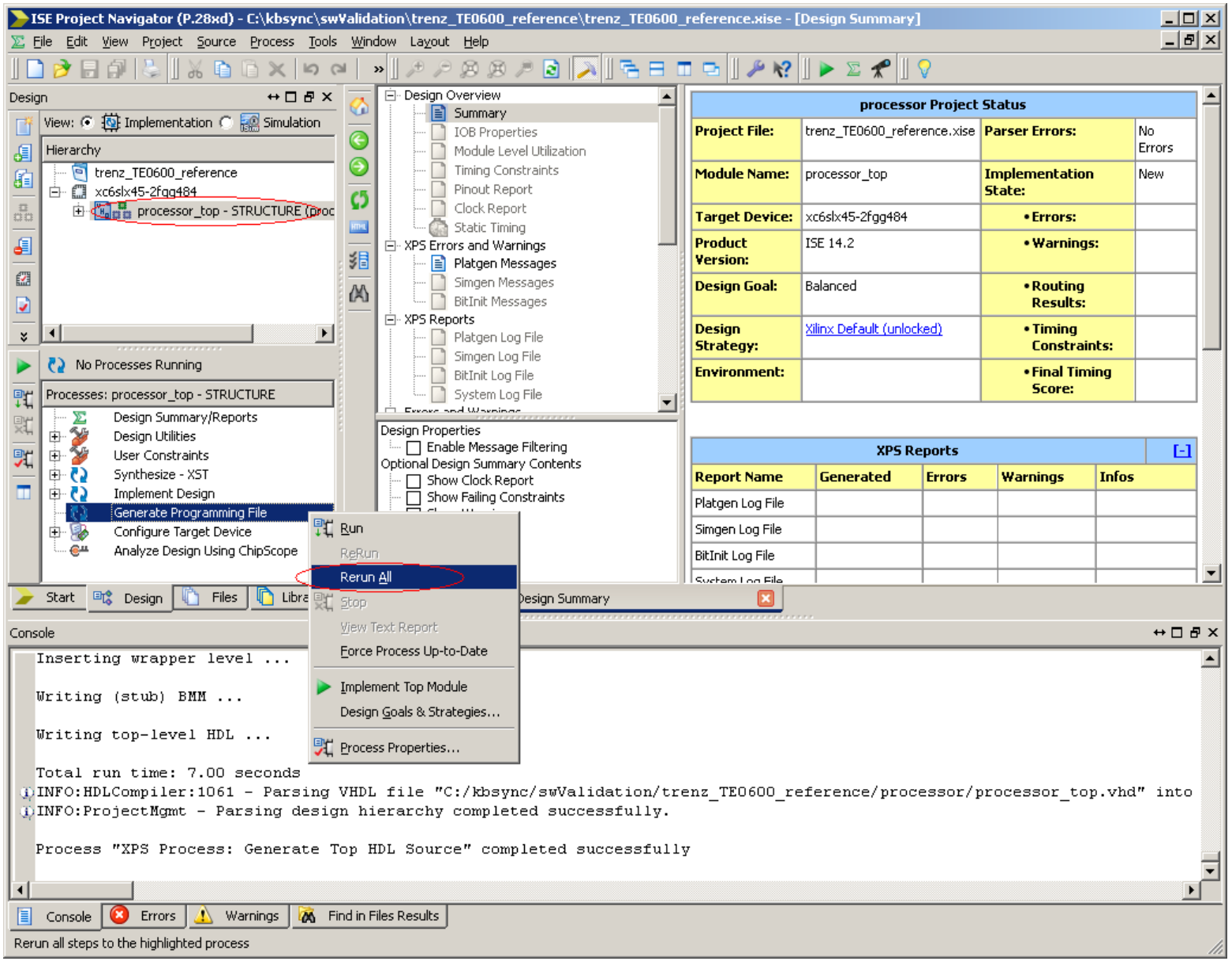
provide path to the private pcores (singlewire) then click OK



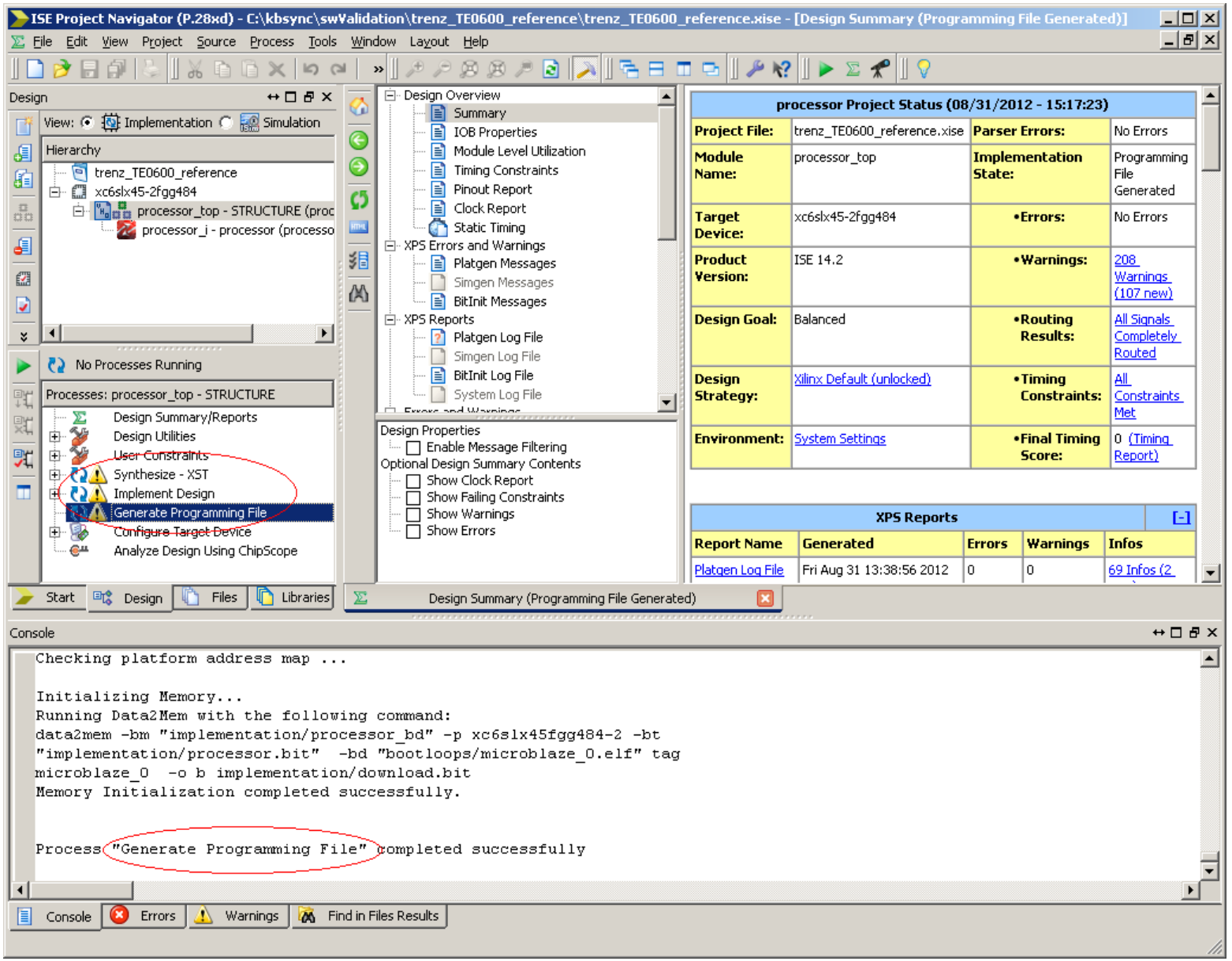
return to ISE Project Navigator, step on processor.xmp and generate TOP HDL Source



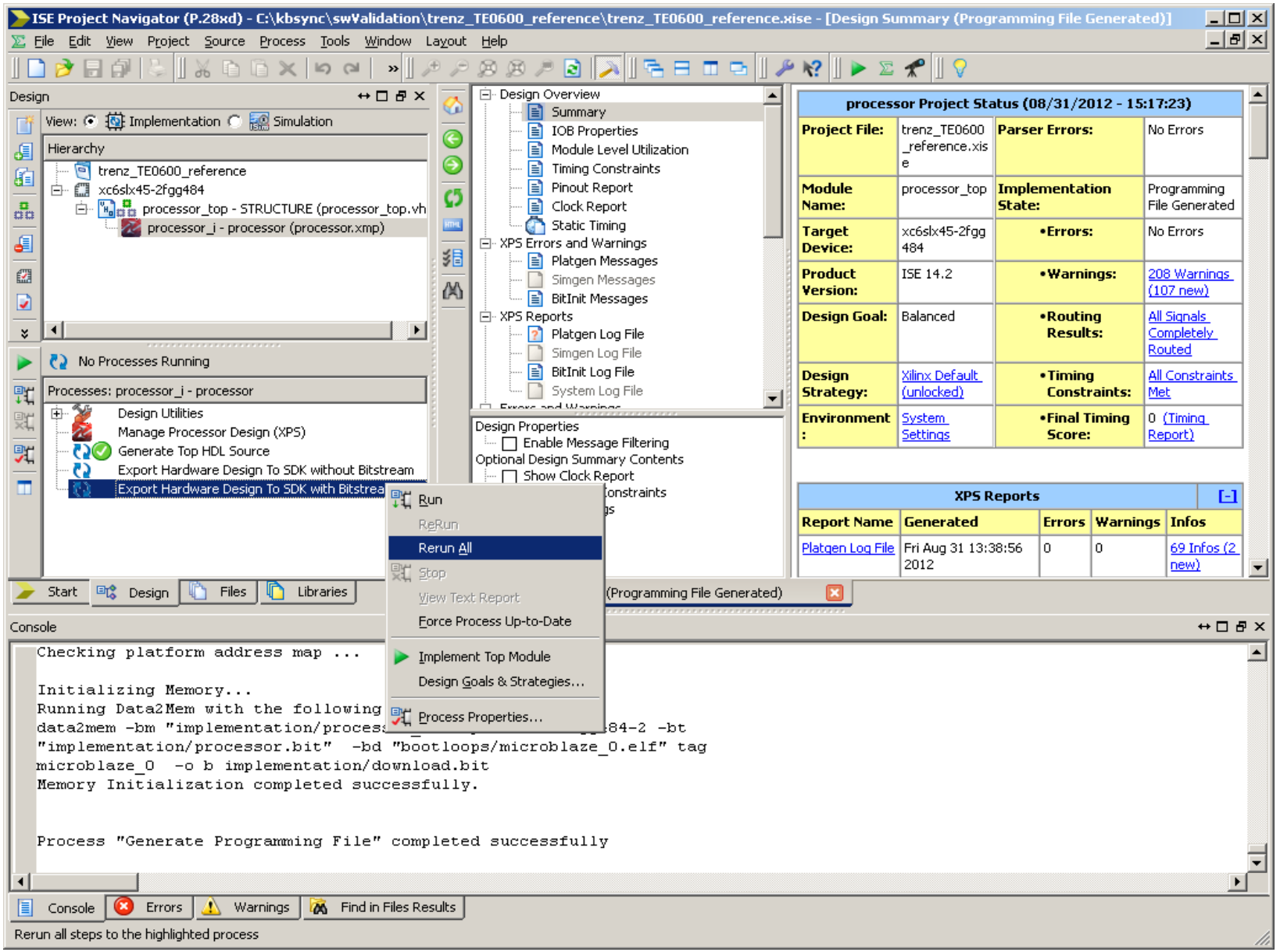
step on processor.xmp, choose Generate Programming File and click Rerun All



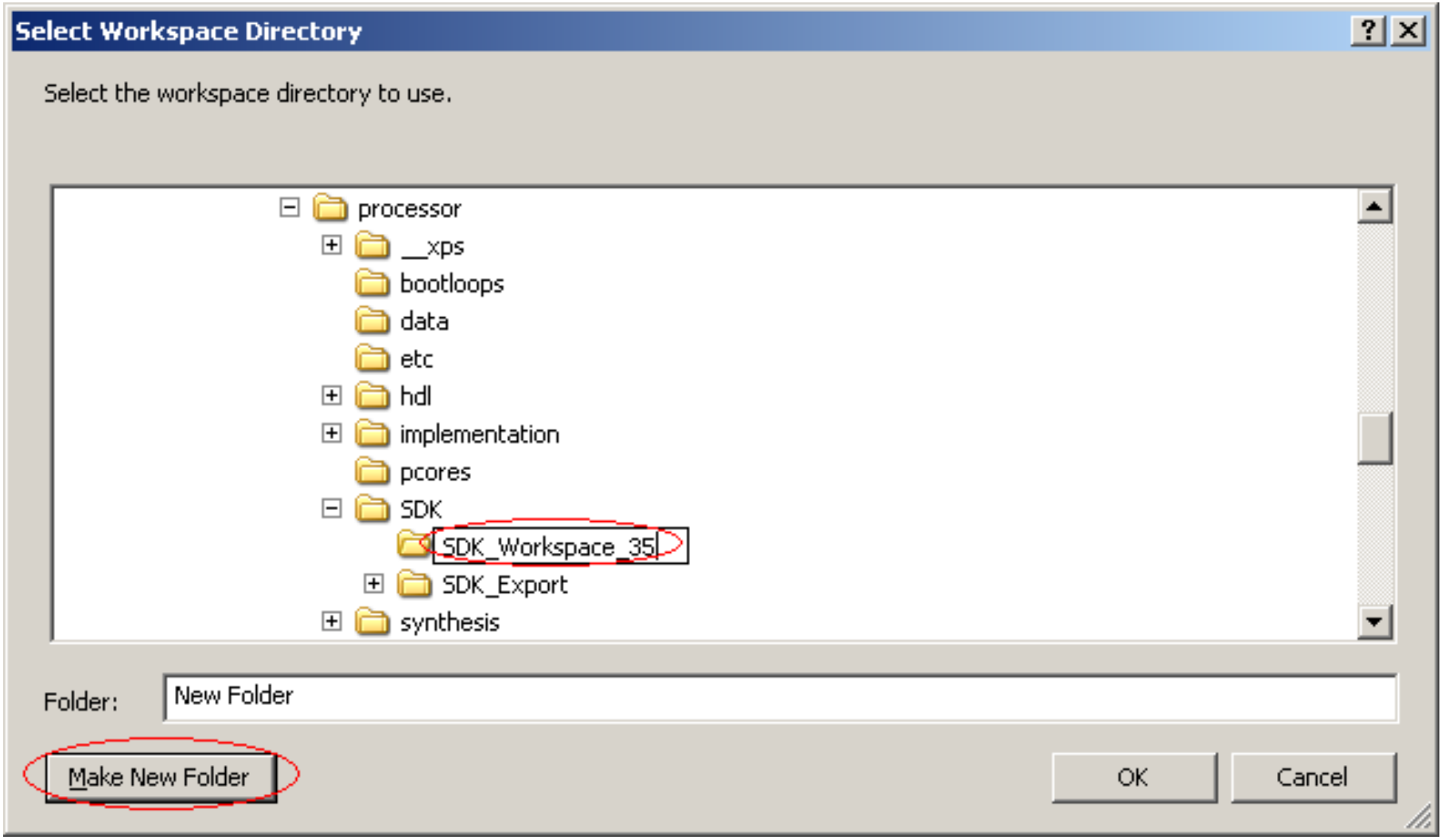
confirm generation success and return to Xilinx Platform Studio



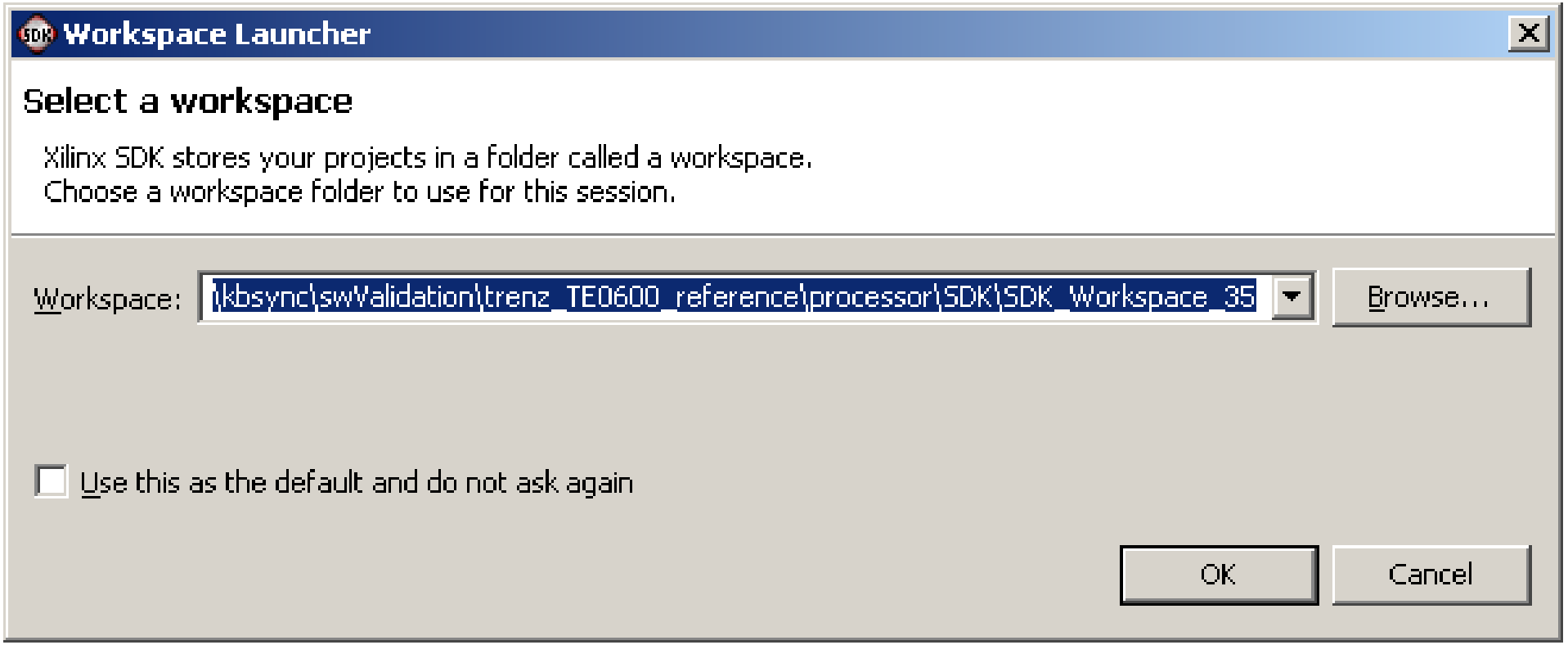
choose from menu Export Hardware Design to SDK with bitstream



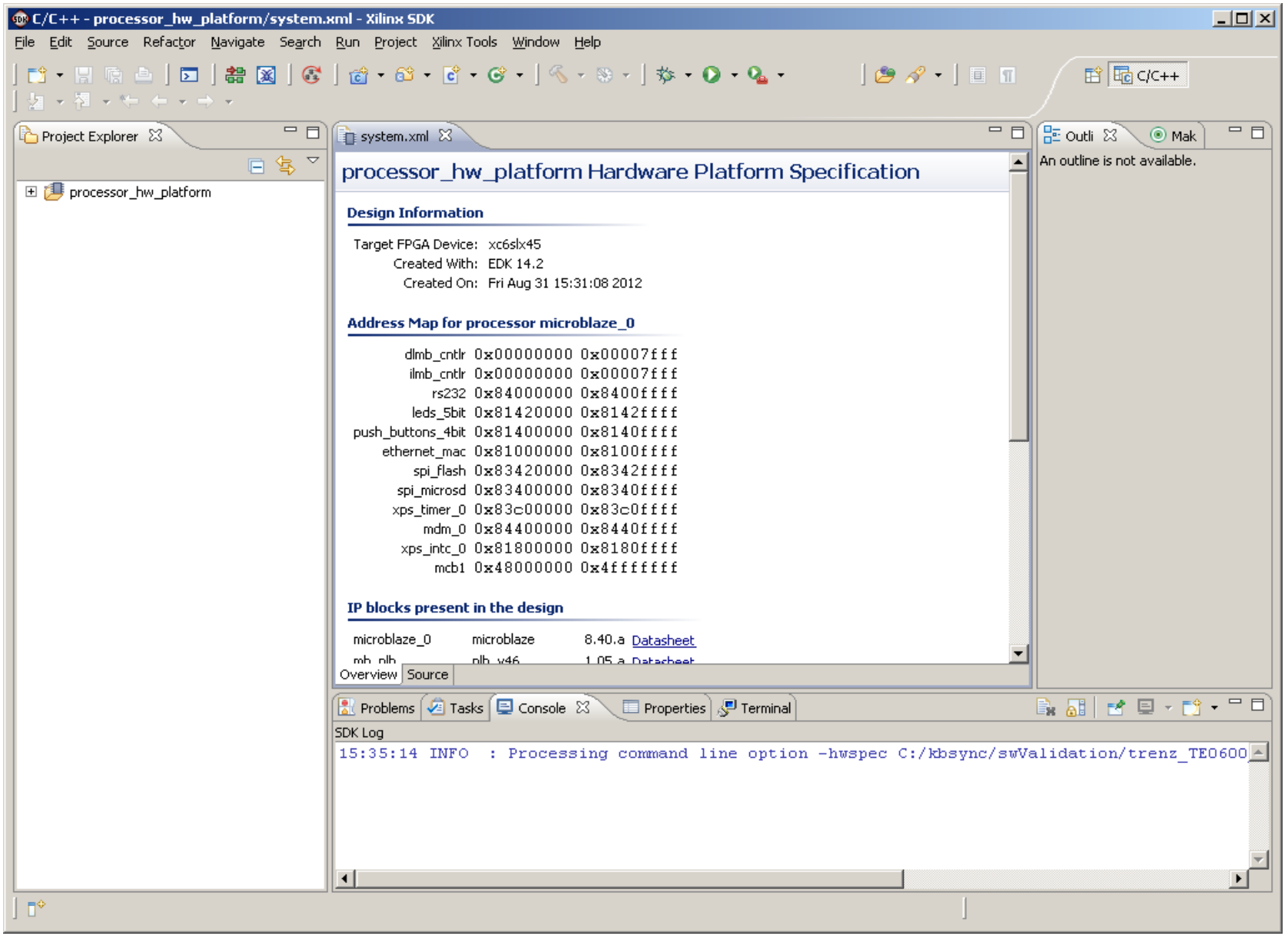
Create workspace working folder



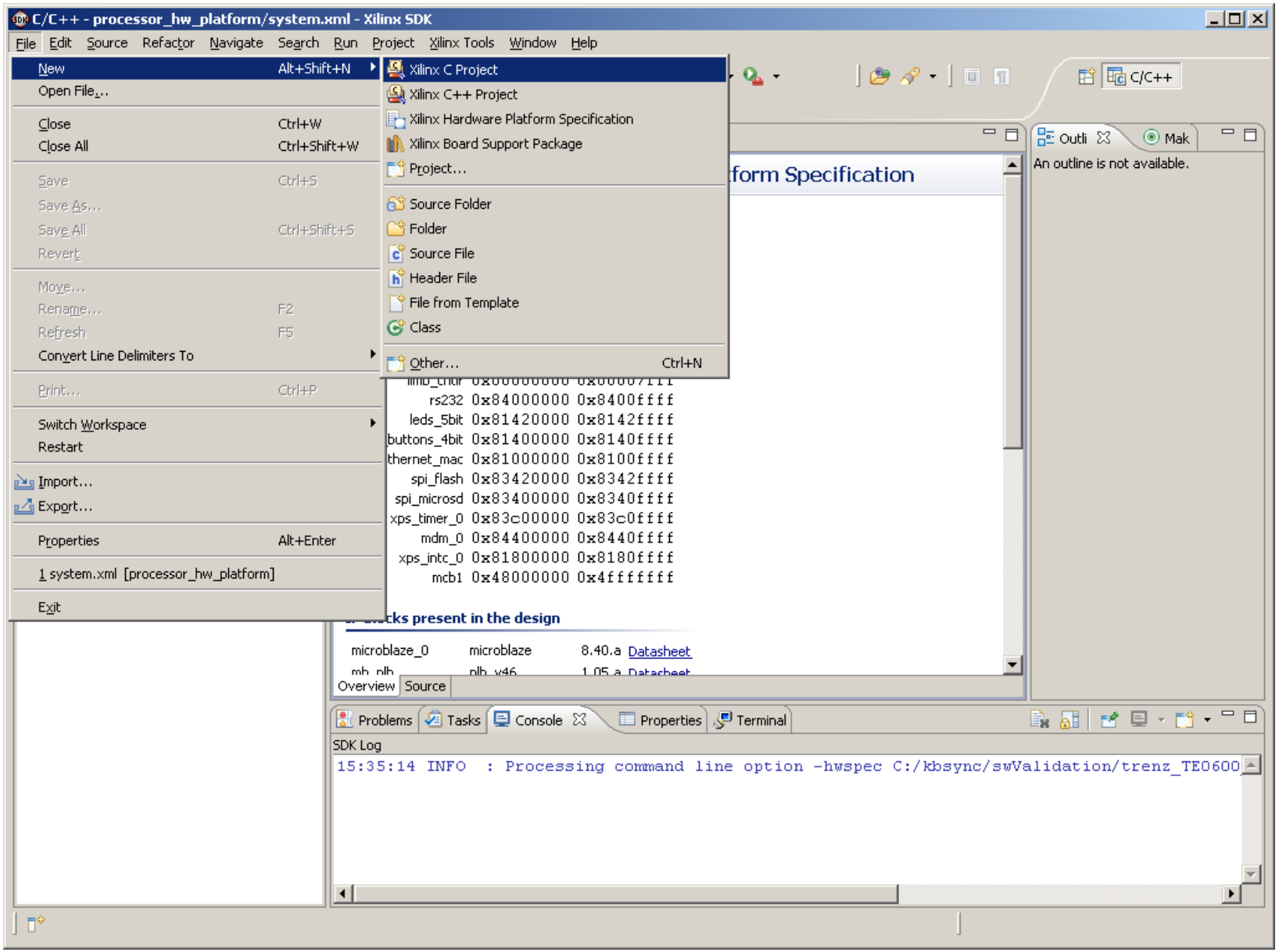
Confirm worspace location



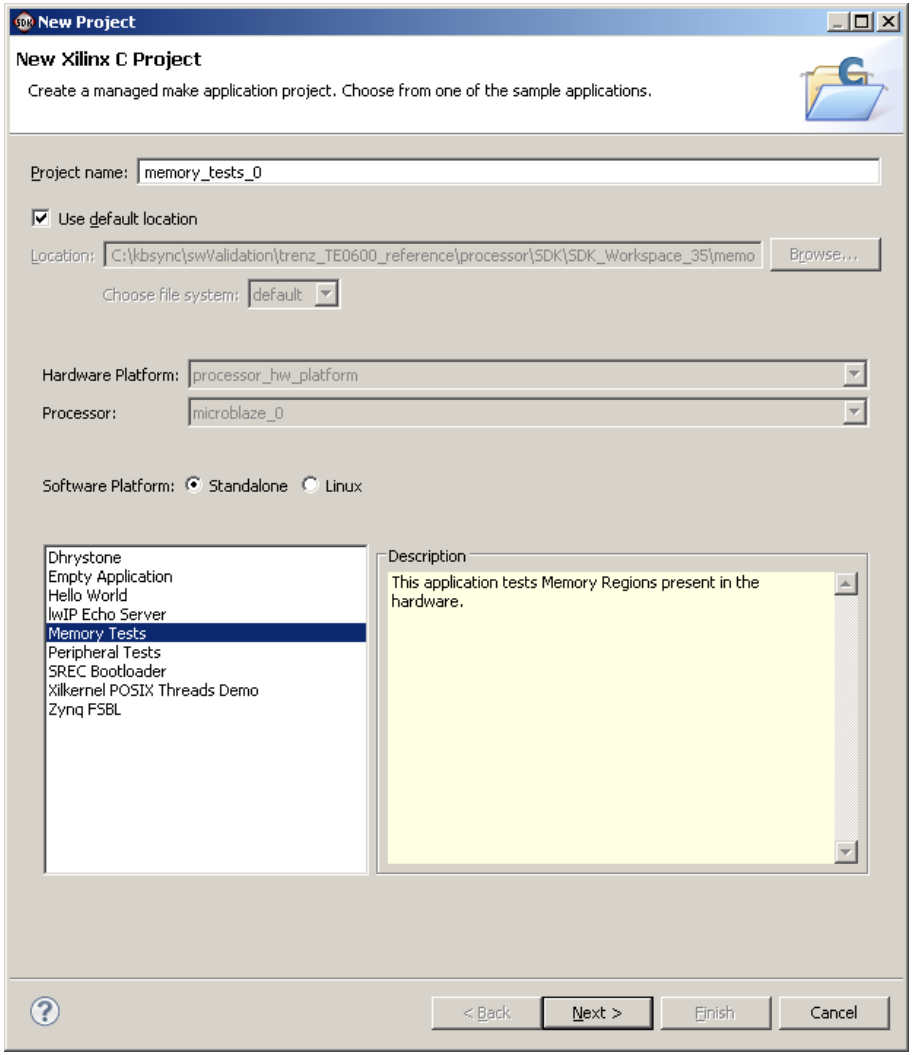
Obtain empty SDK configuration



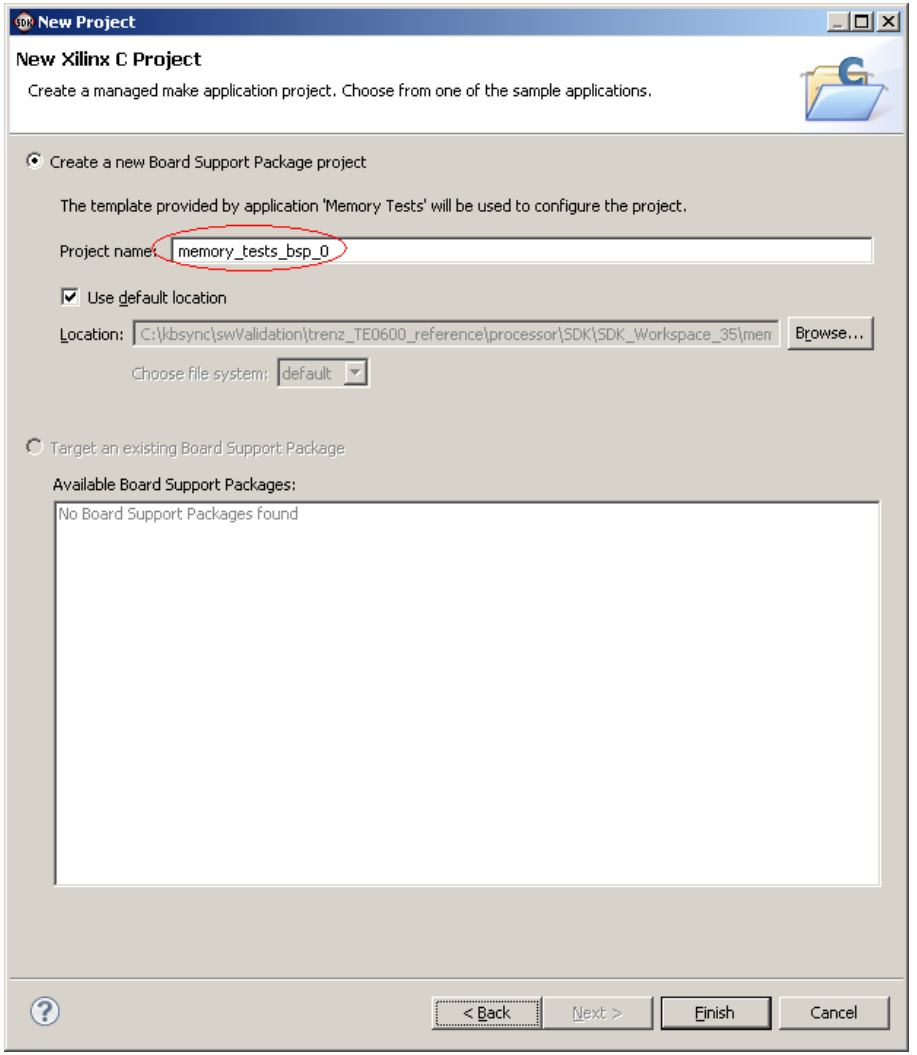
from SDK menu choose to create New Xilinx C Project



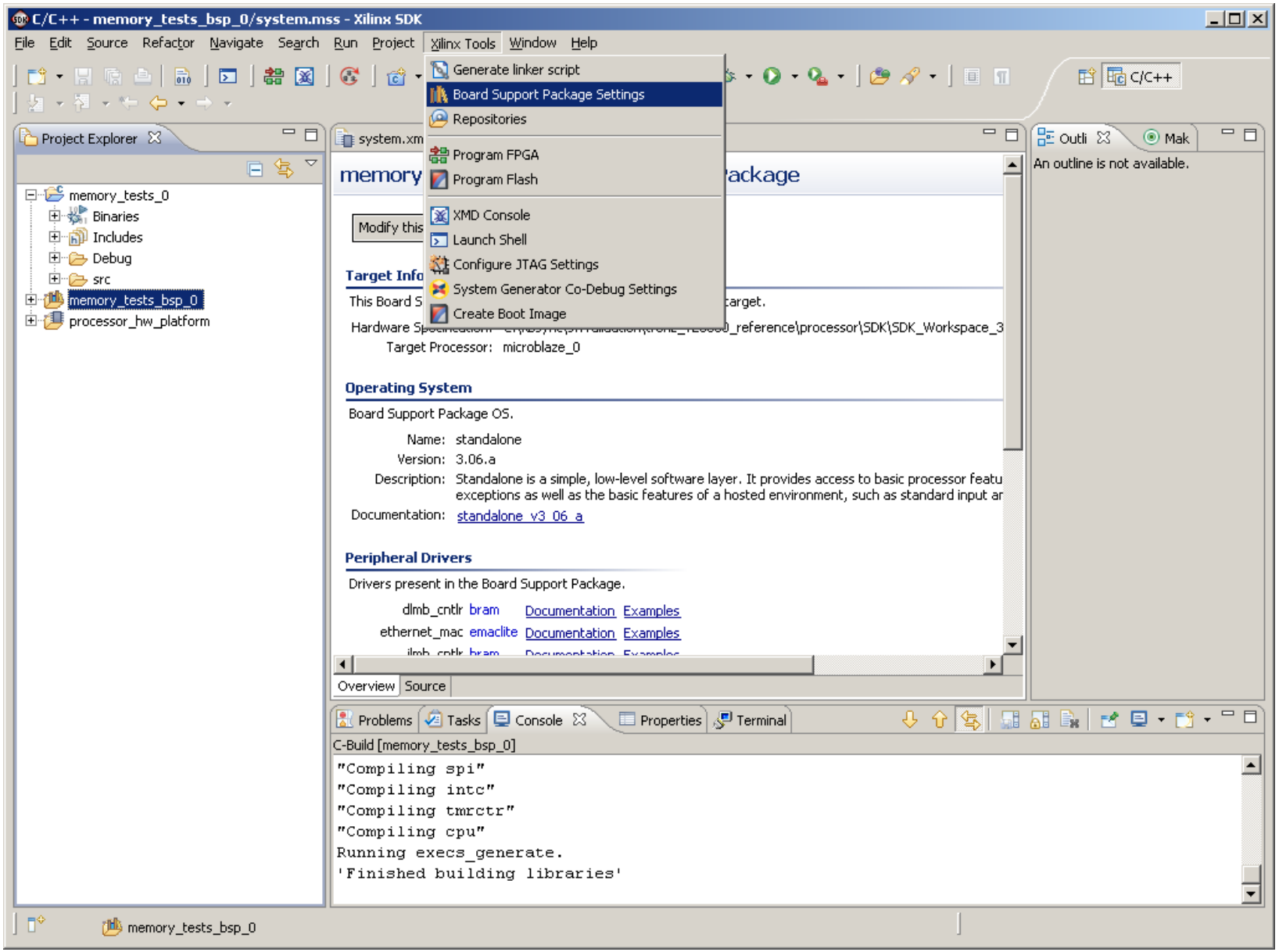
choose Memory Tests template and click Next



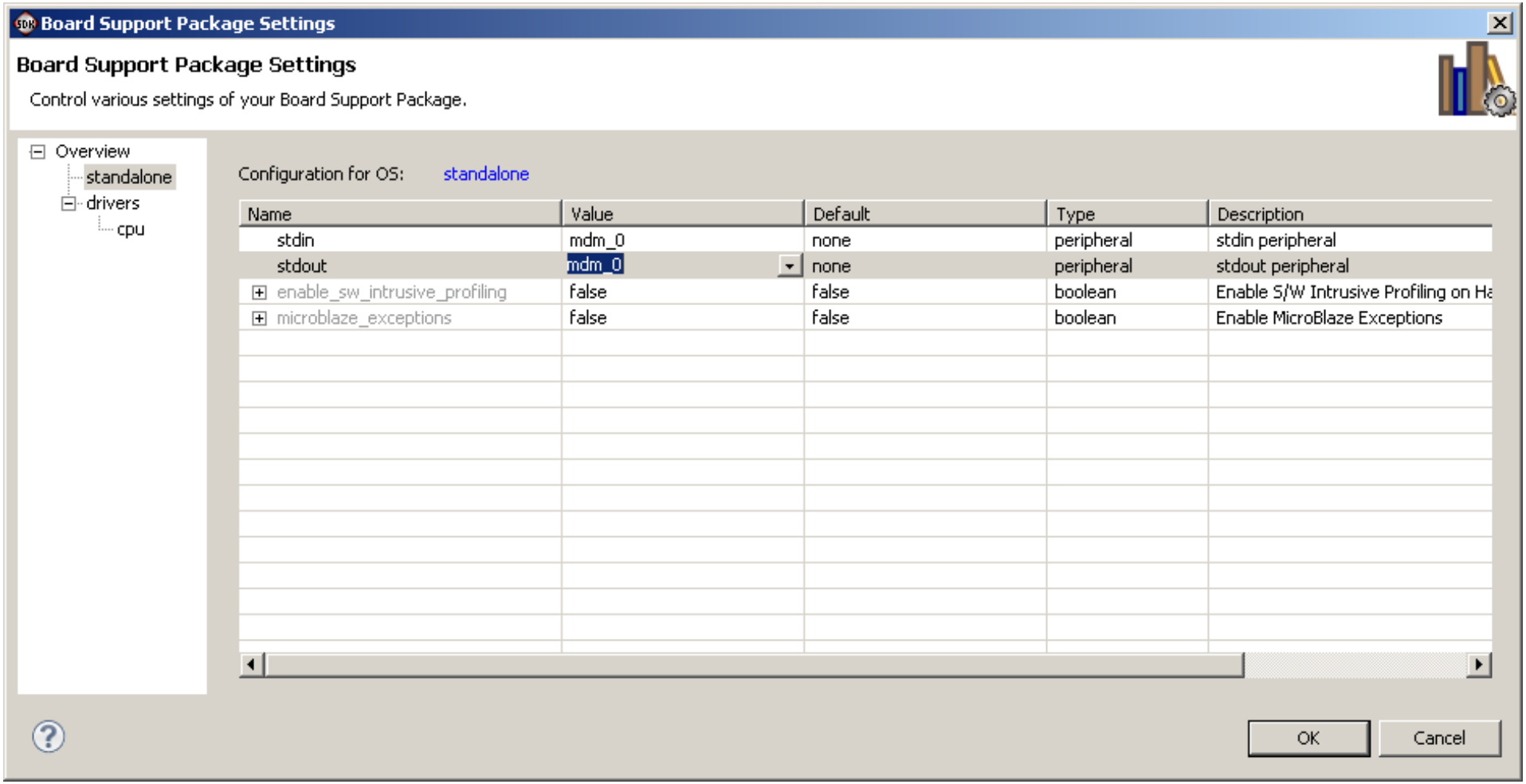
keep default BSP project name memory_tests_bsp_0 and click Finish



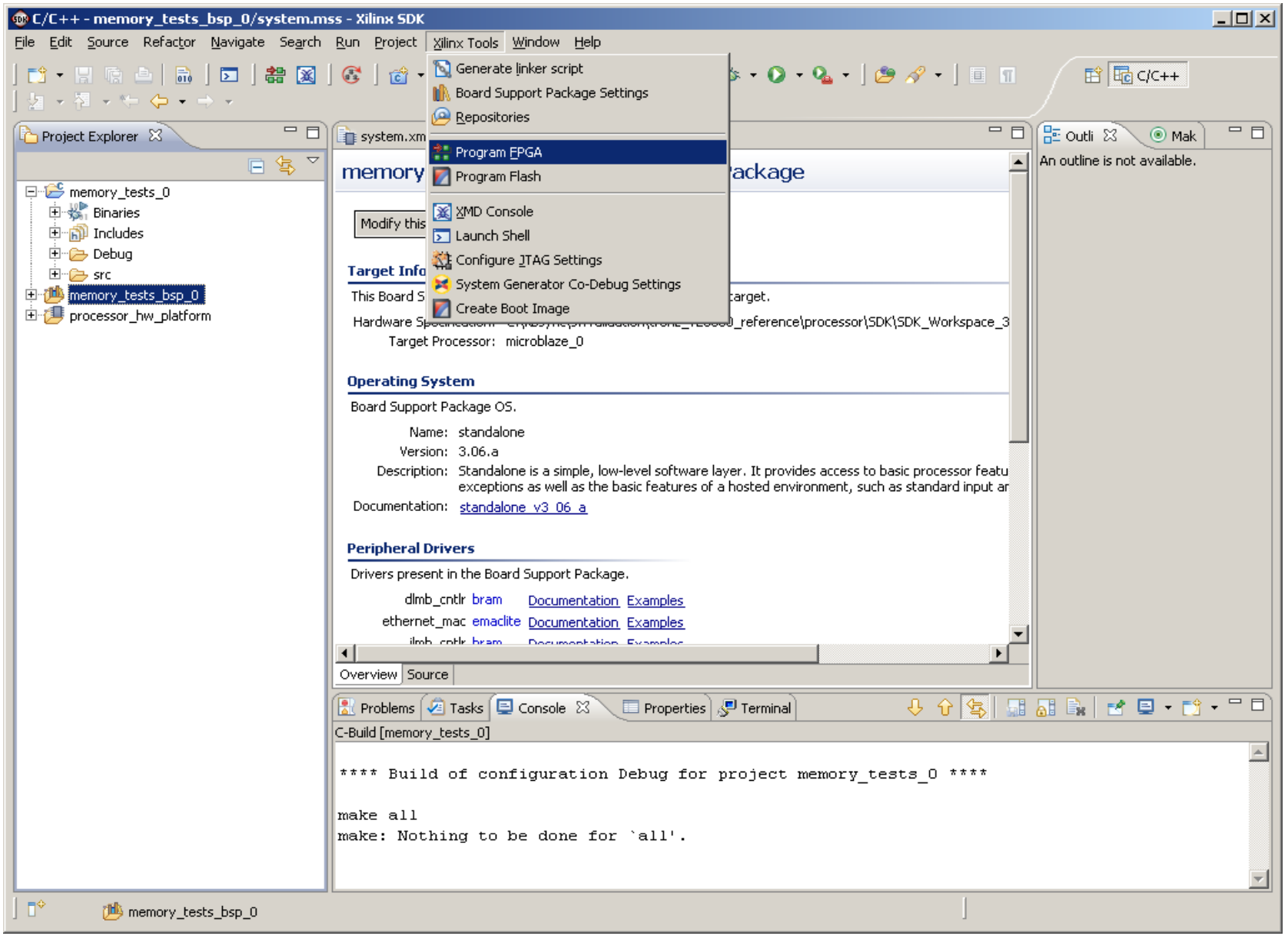
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



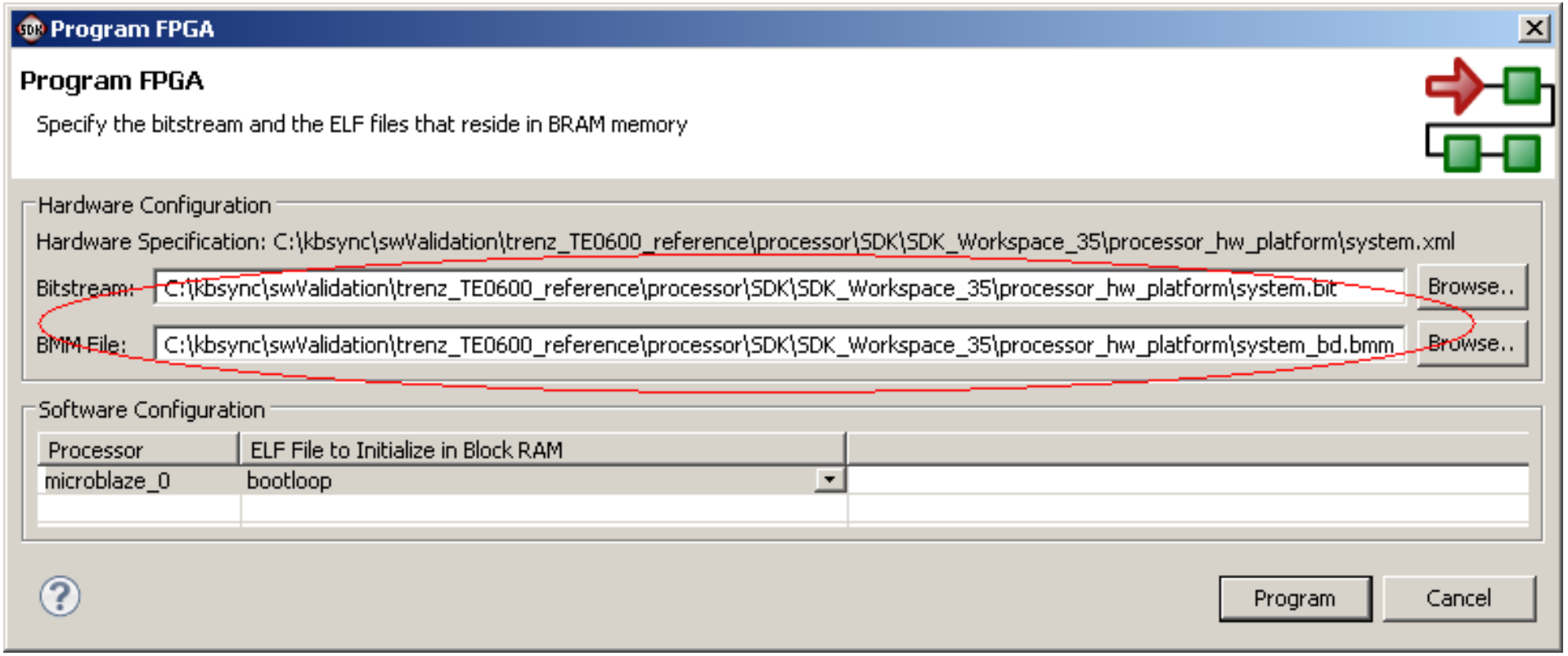
from standalone section apply mdm_0 to stdin and stdout then click OK



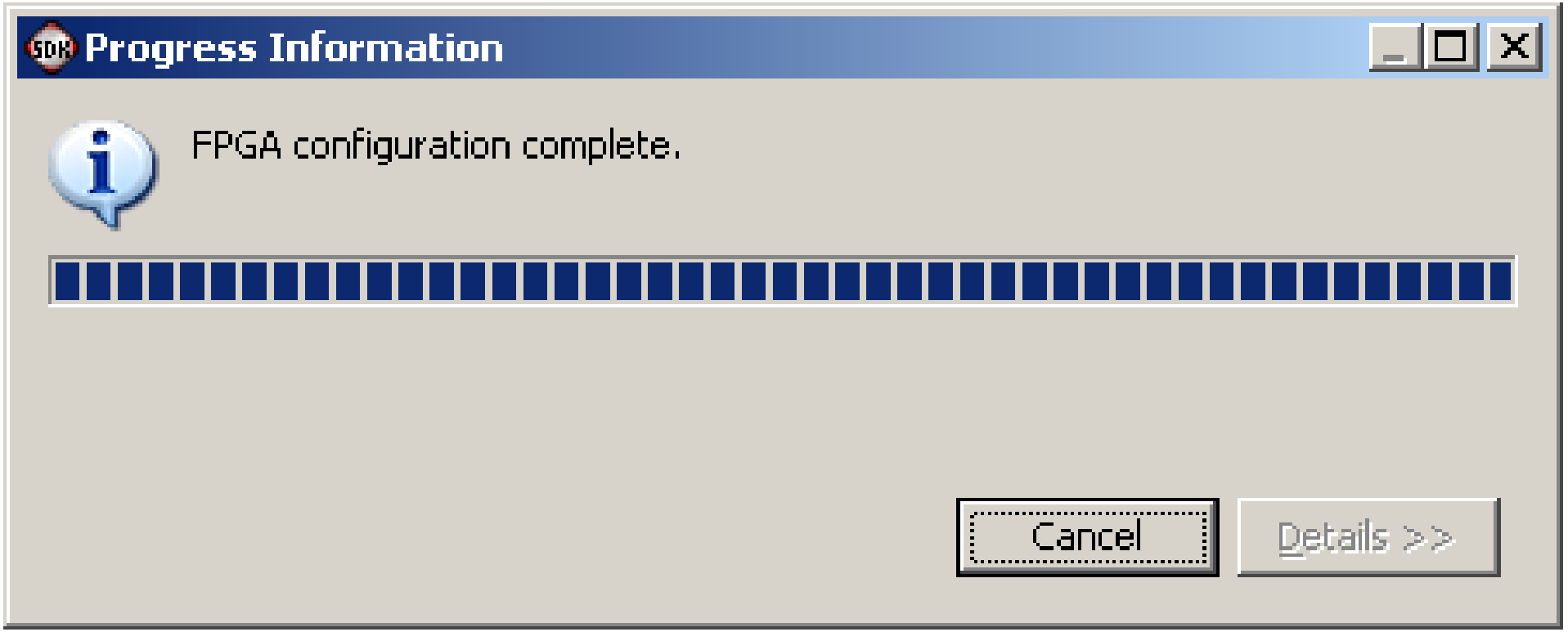
connect the prototype board TE0600 and choose Program FPGA from menu



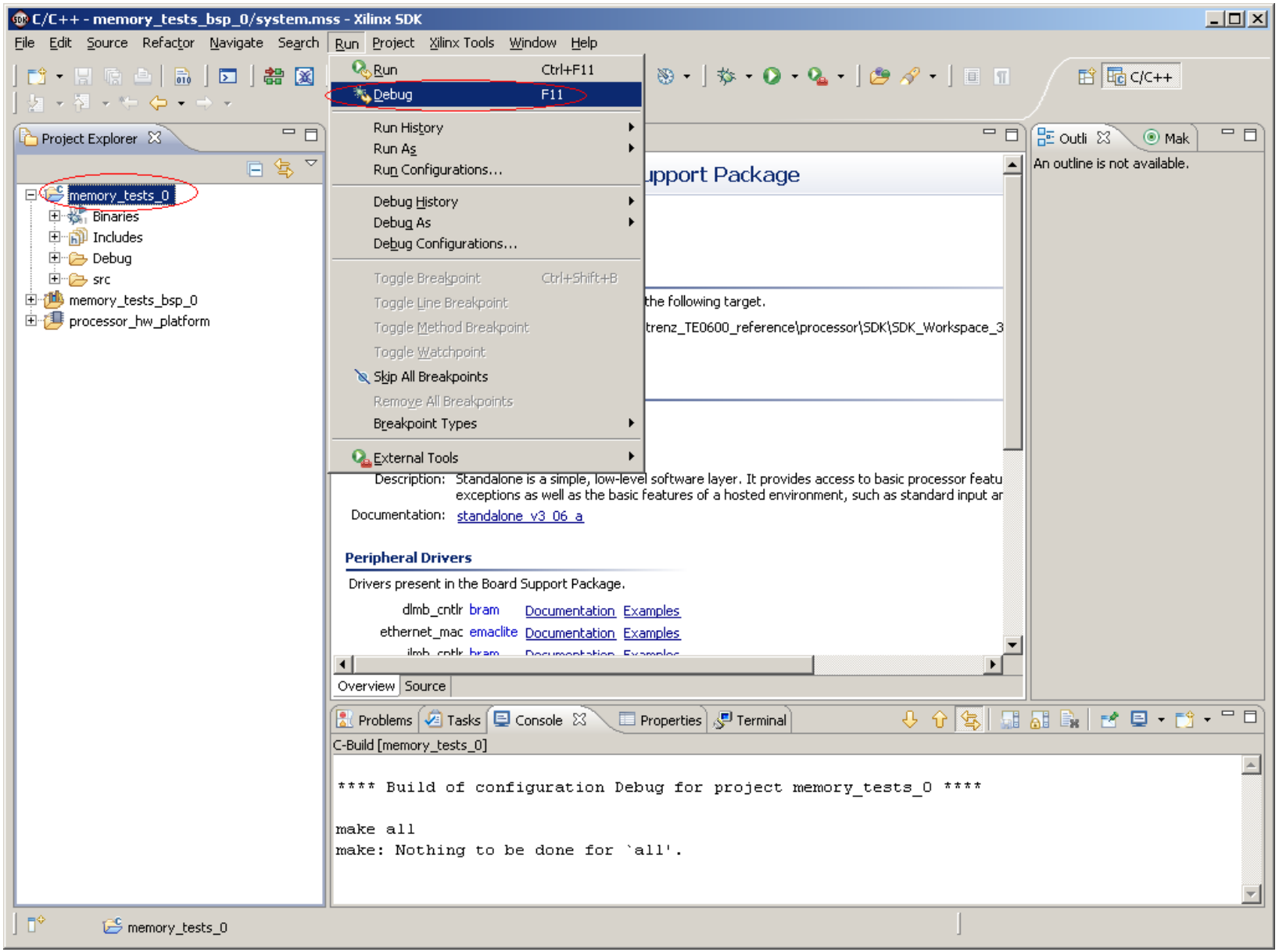
provide correct Bistream and BMM files then click Program



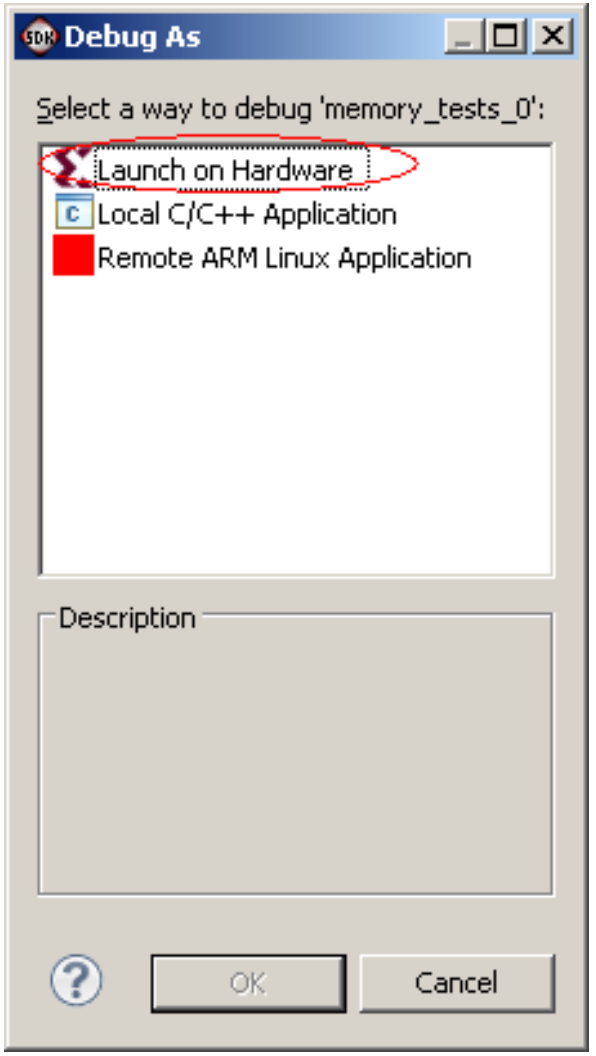
wait for FPGA programming completion



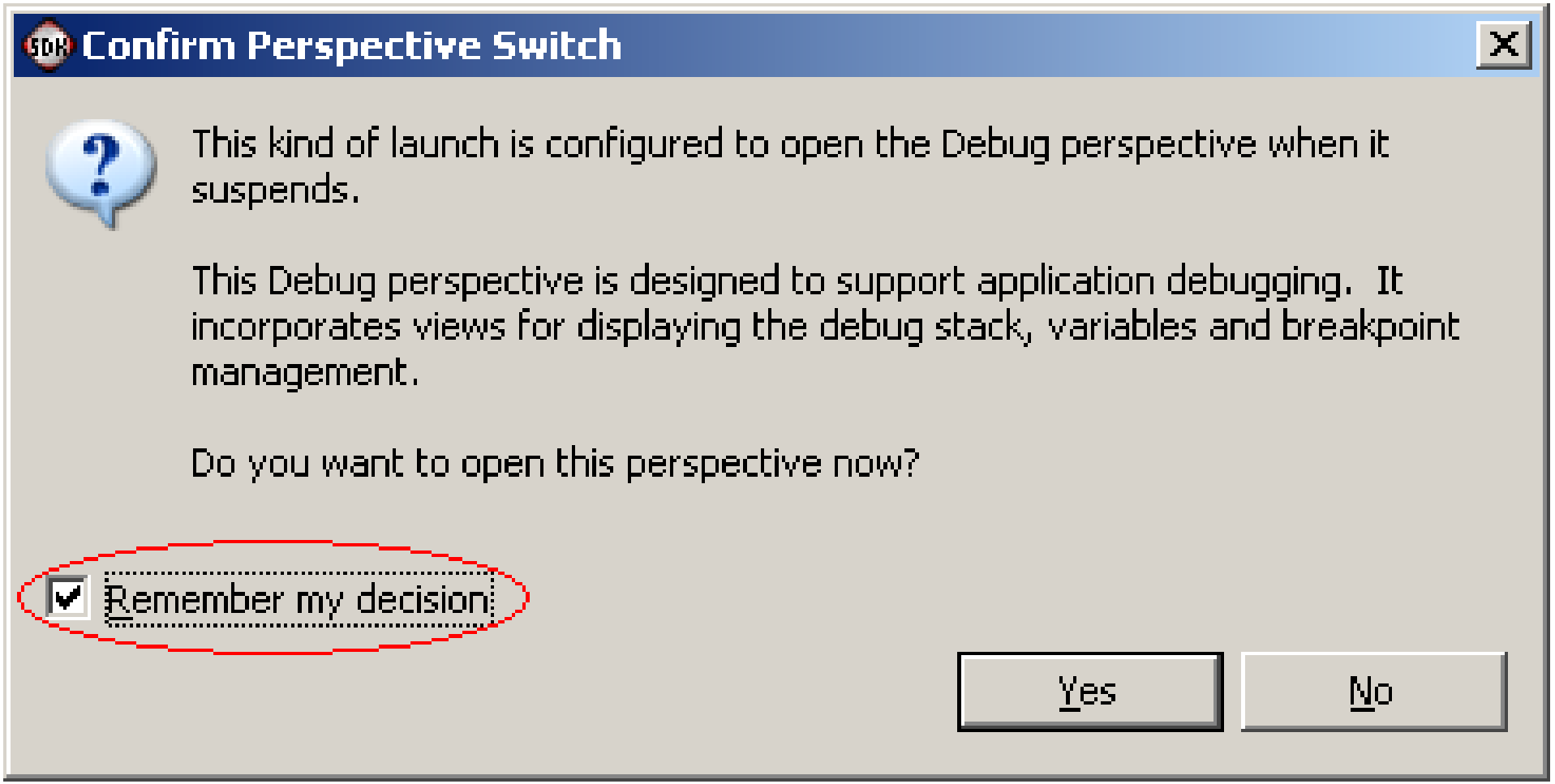
step on memory_tests_0 application and choose Debug menu



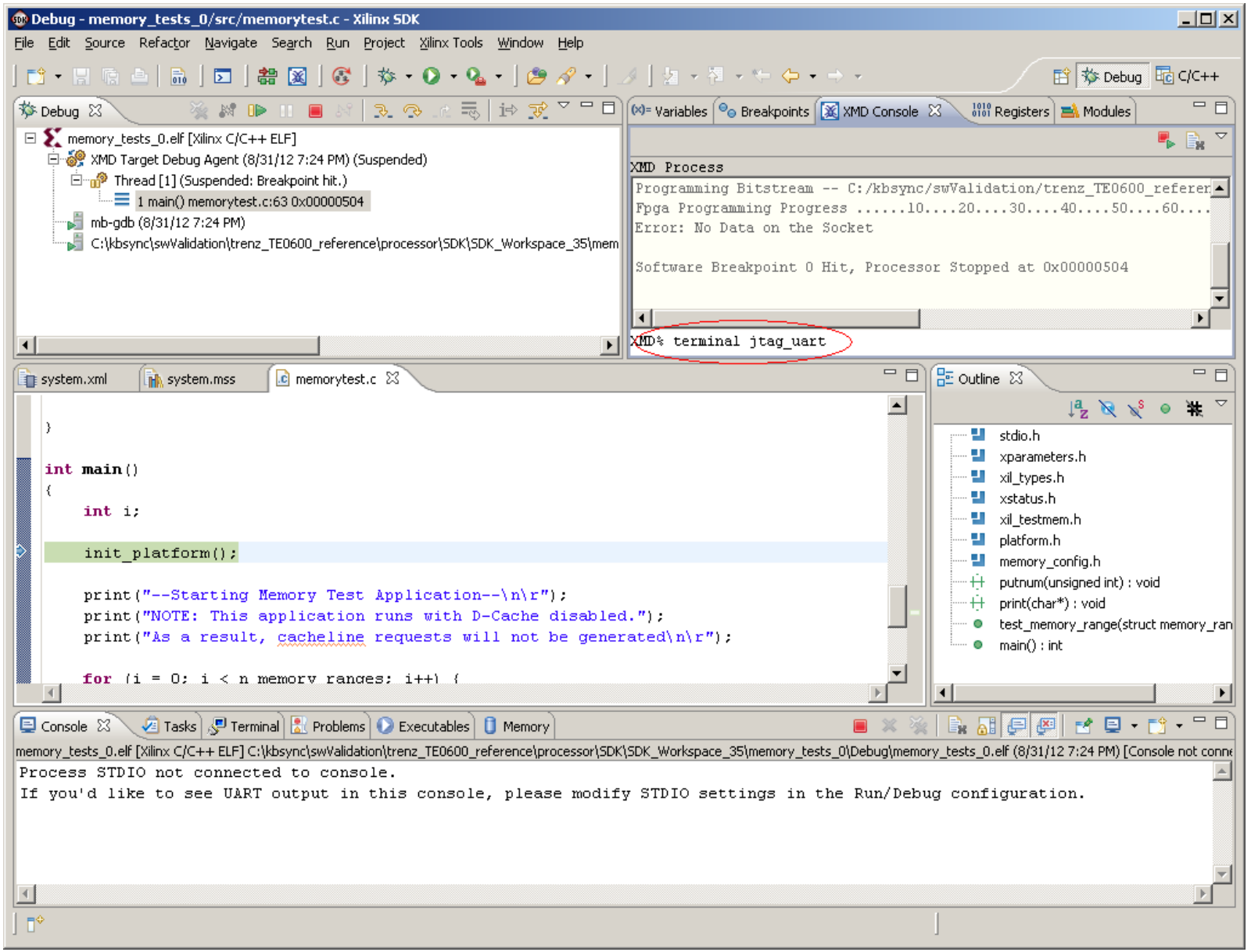
Confirm launch on a hardware



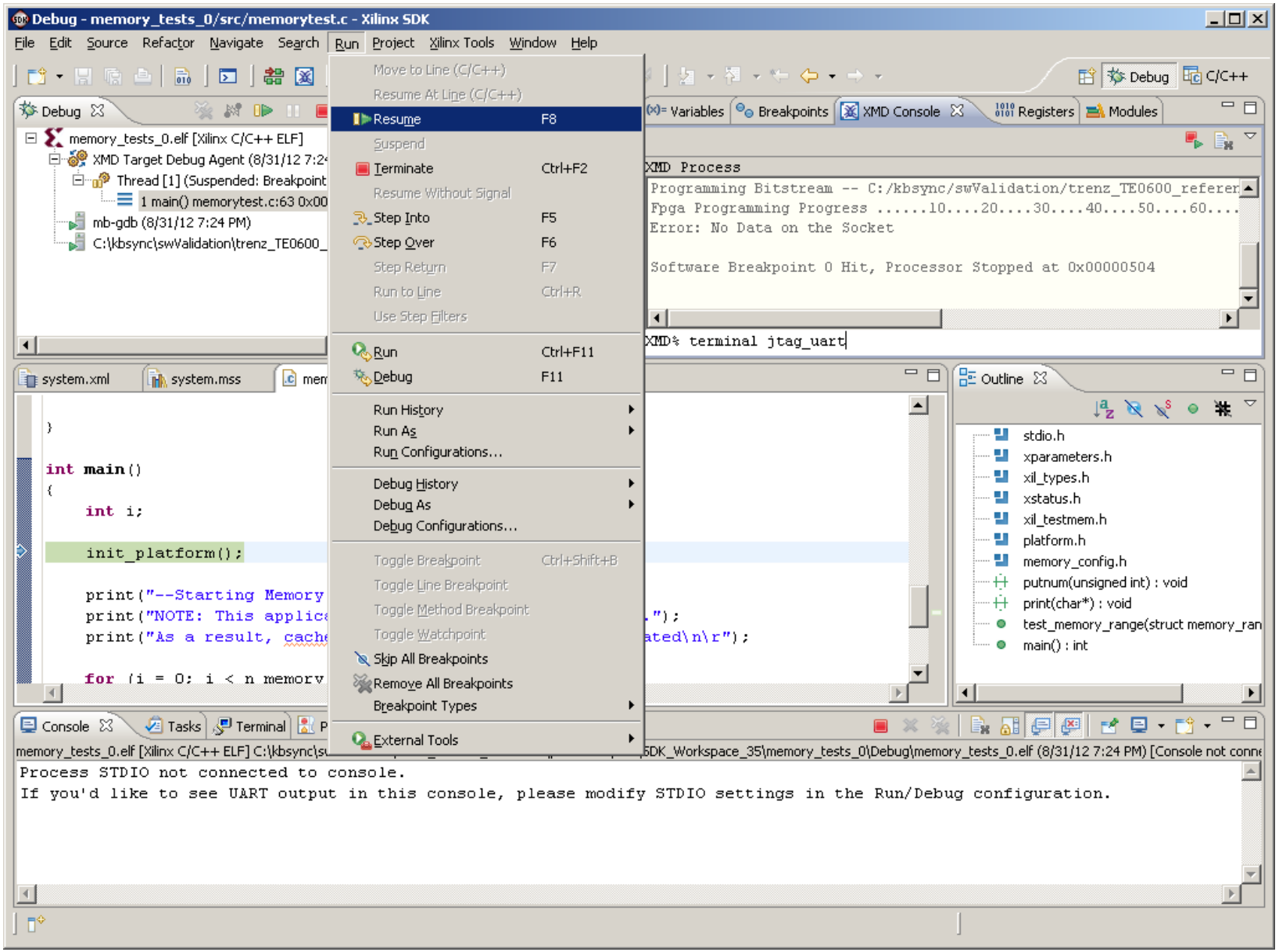
choose remember decision and confirm switching to Debug design by clicking Yes button



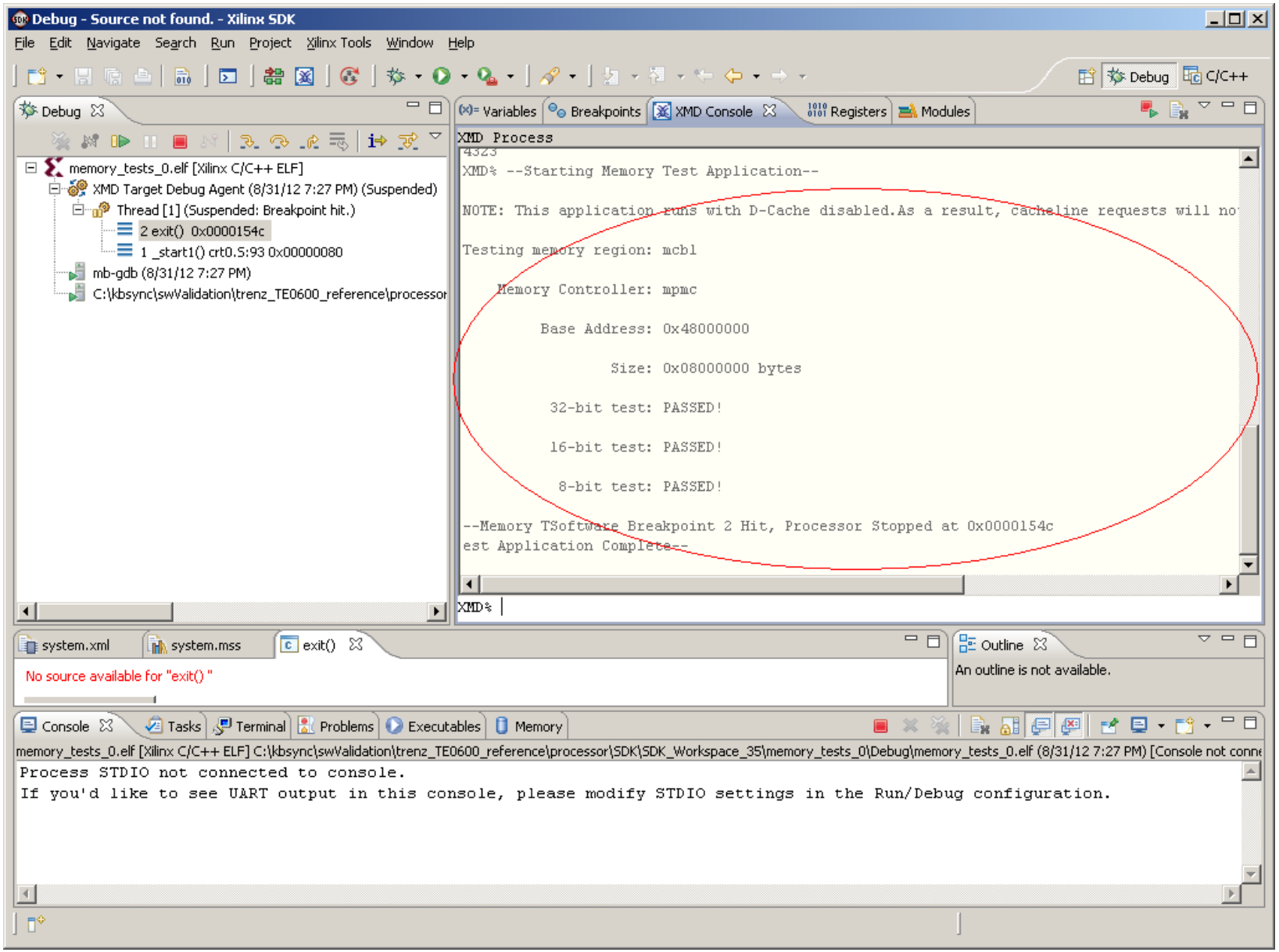
switch to XMD Console tab and type command "terminal jtag_uart



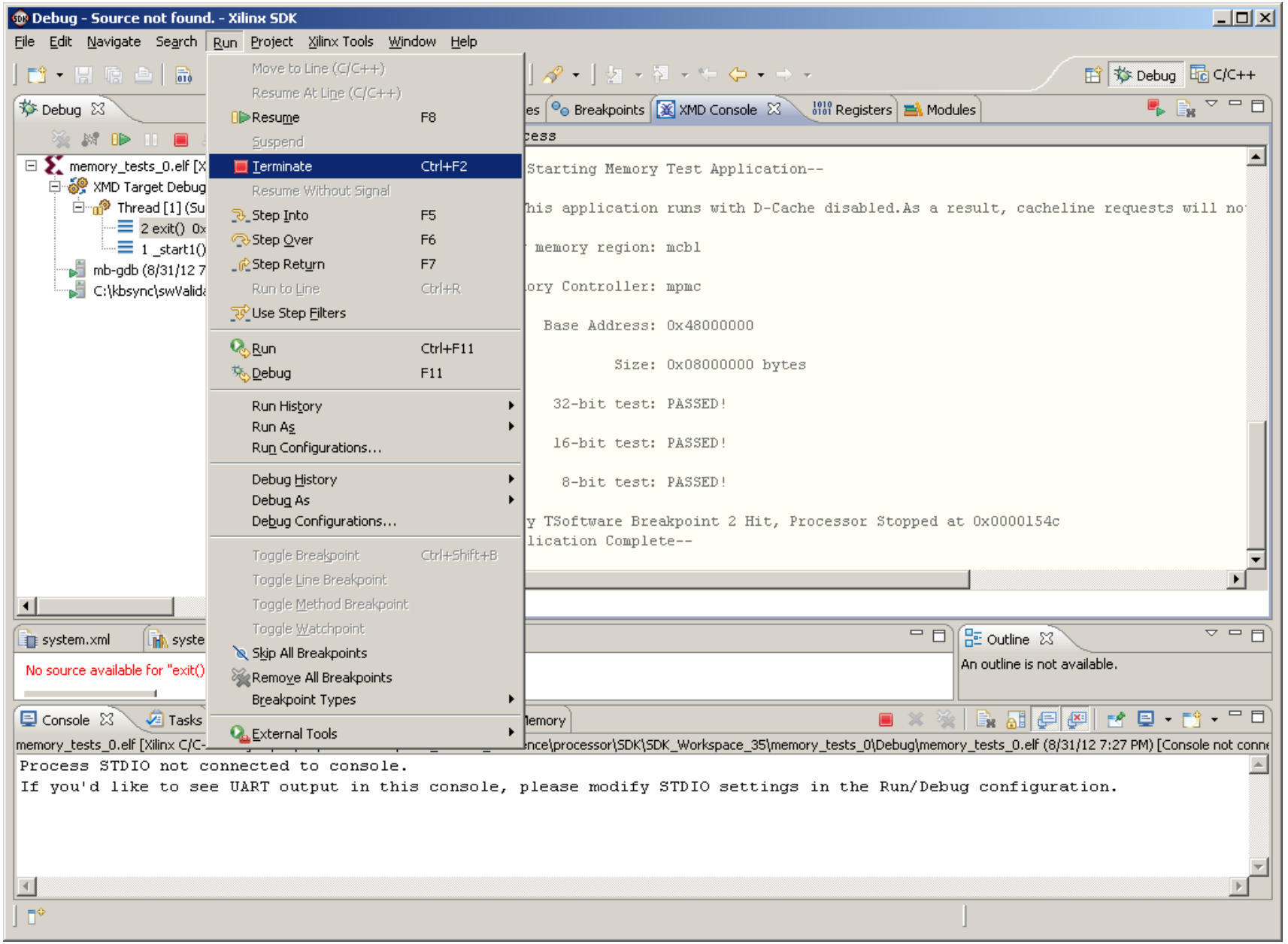
resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application



TE0600 board configuration complete

external memory configuration confirmed with test application