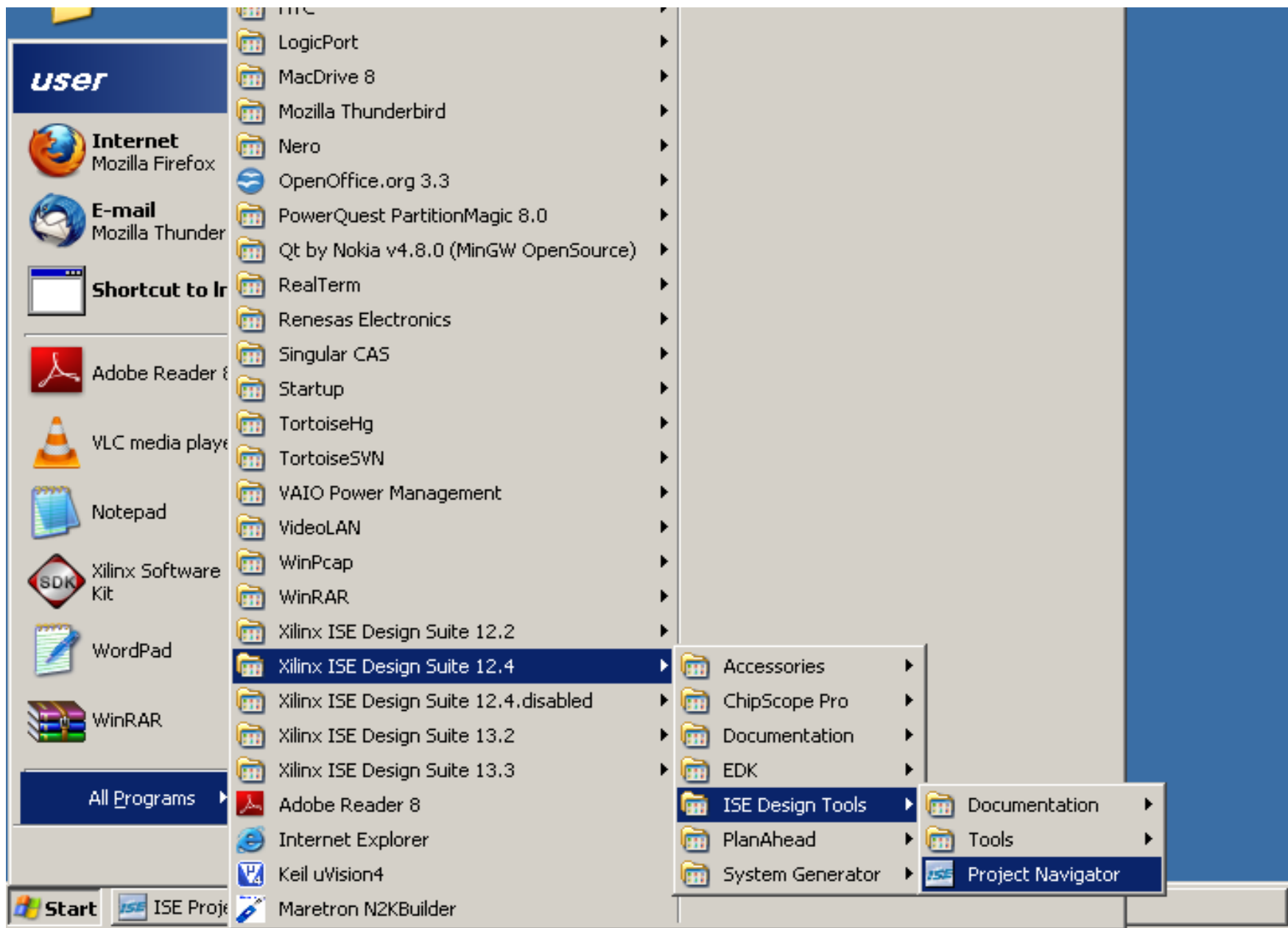
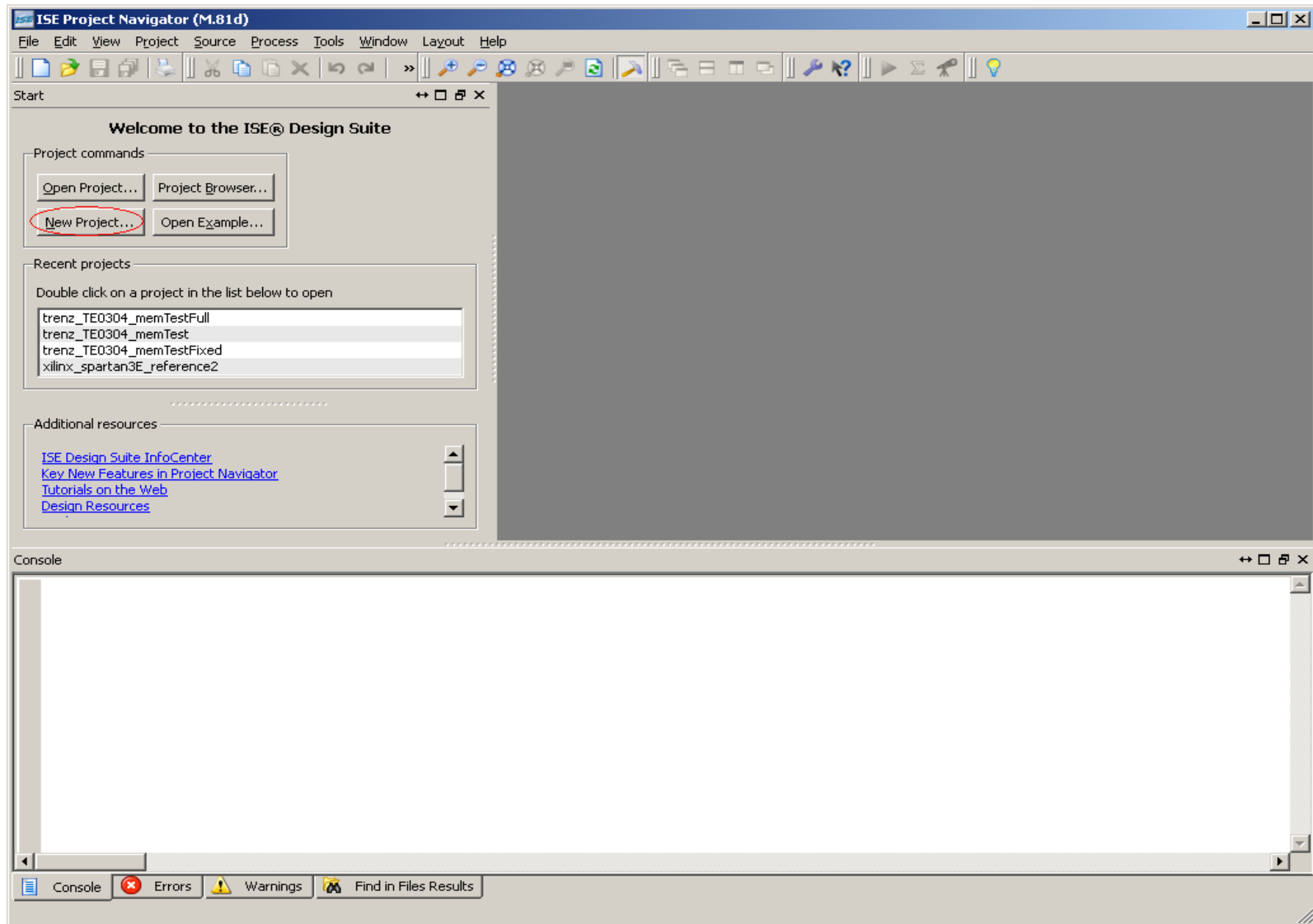


TE0320 platform

reference project creation sequence



start Xilinx ISE Project Navigator



click button to create a new project

New Project Wizard [X]

Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name: trenz_TE0320_reference

Location: C:\m2sync\trenz_TE0320_reference ...

Working Directory: C:\m2sync\trenz_TE0320_reference ...

Description:

Select the type of top-level source for the project

Top-level source type:
HDL

More Info Next > Cancel

choose project name, then click Next

New Project Wizard

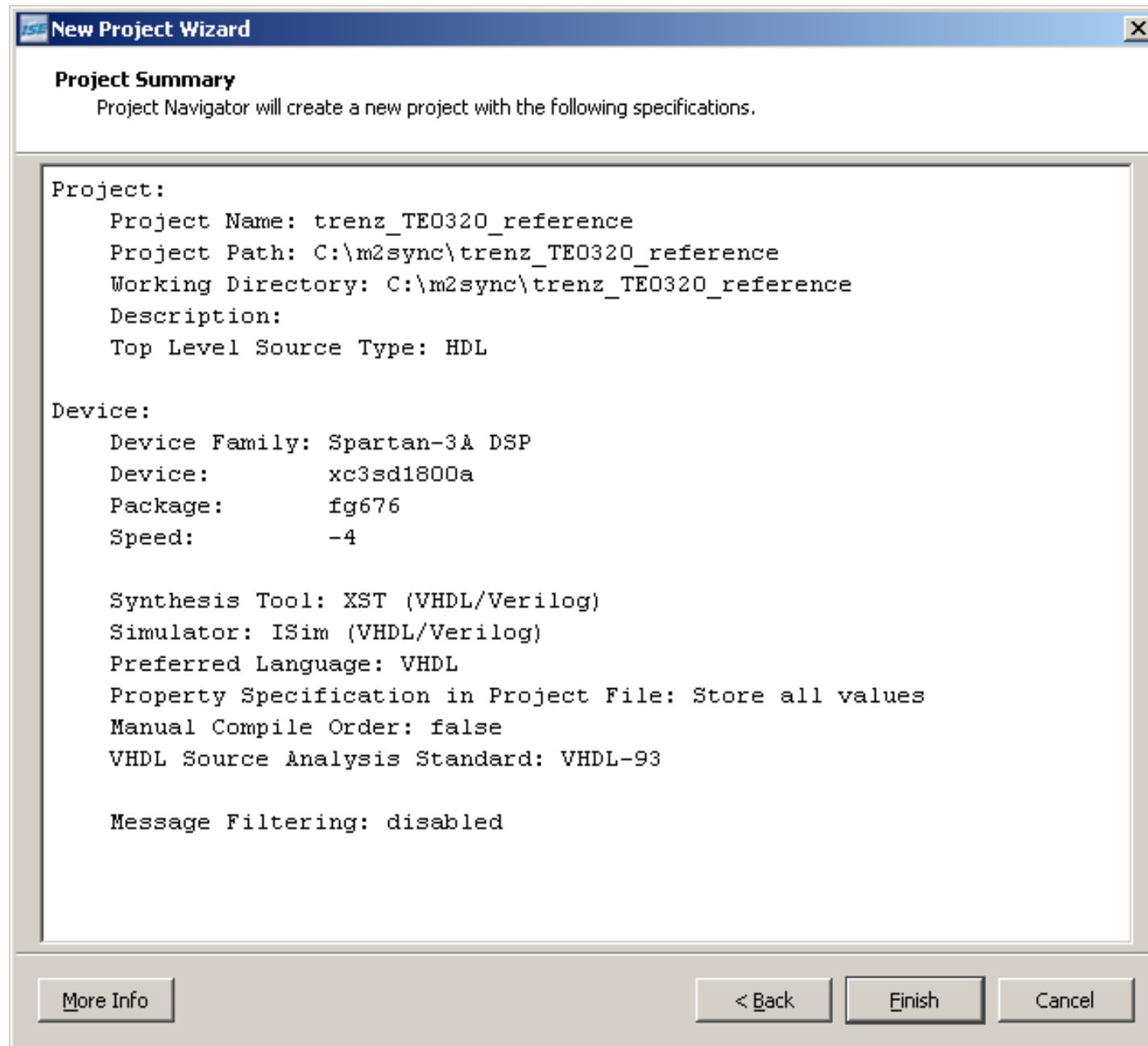
Project Settings
Specify device and project properties.

Select the device and design flow for the project

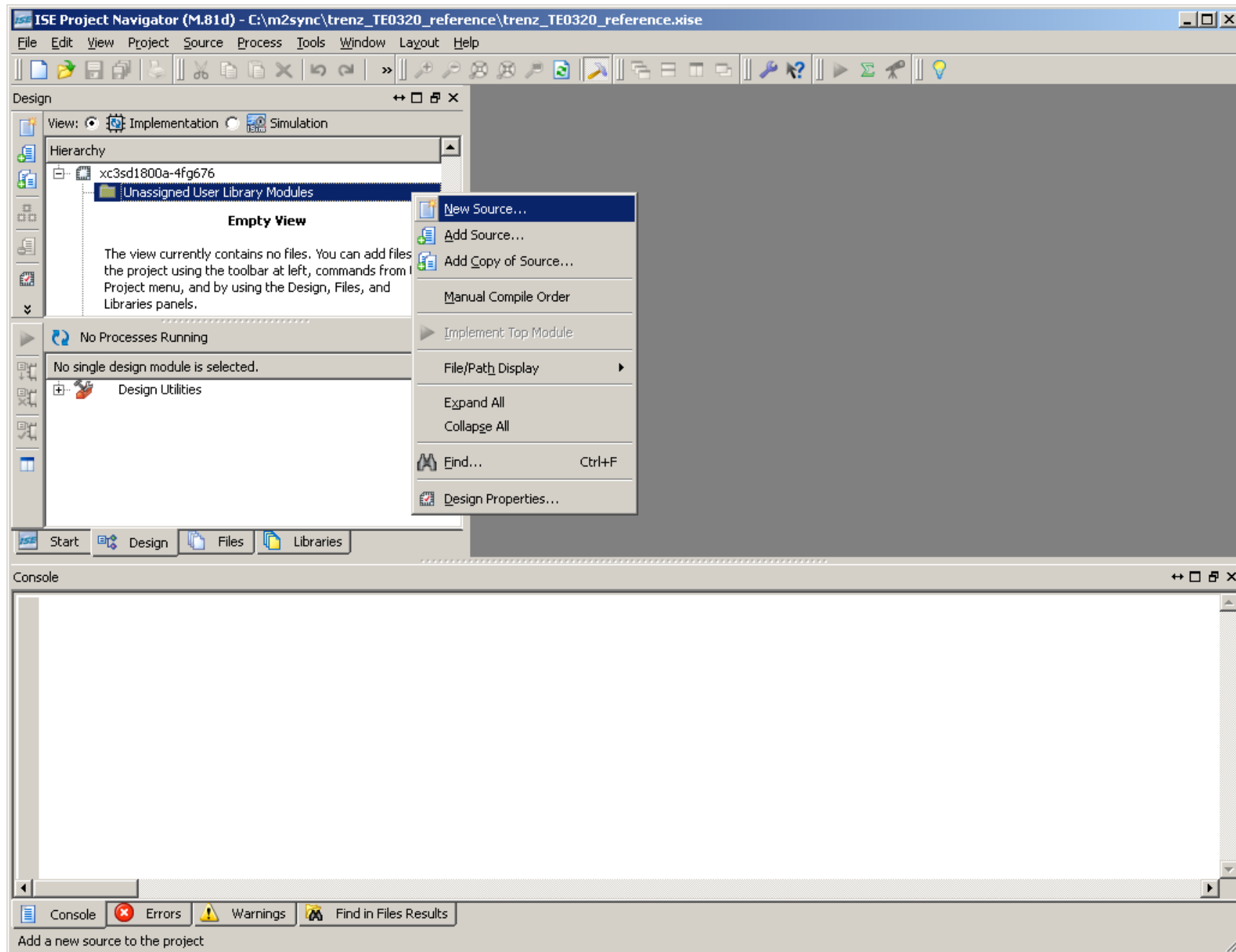
Property Name	Value
Product Category	All
Family	Spartan-3A DSP
Device	XC3SD1800A
Package	FG676
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

[More Info](#) [< Back](#) [Next >](#) [Cancel](#)

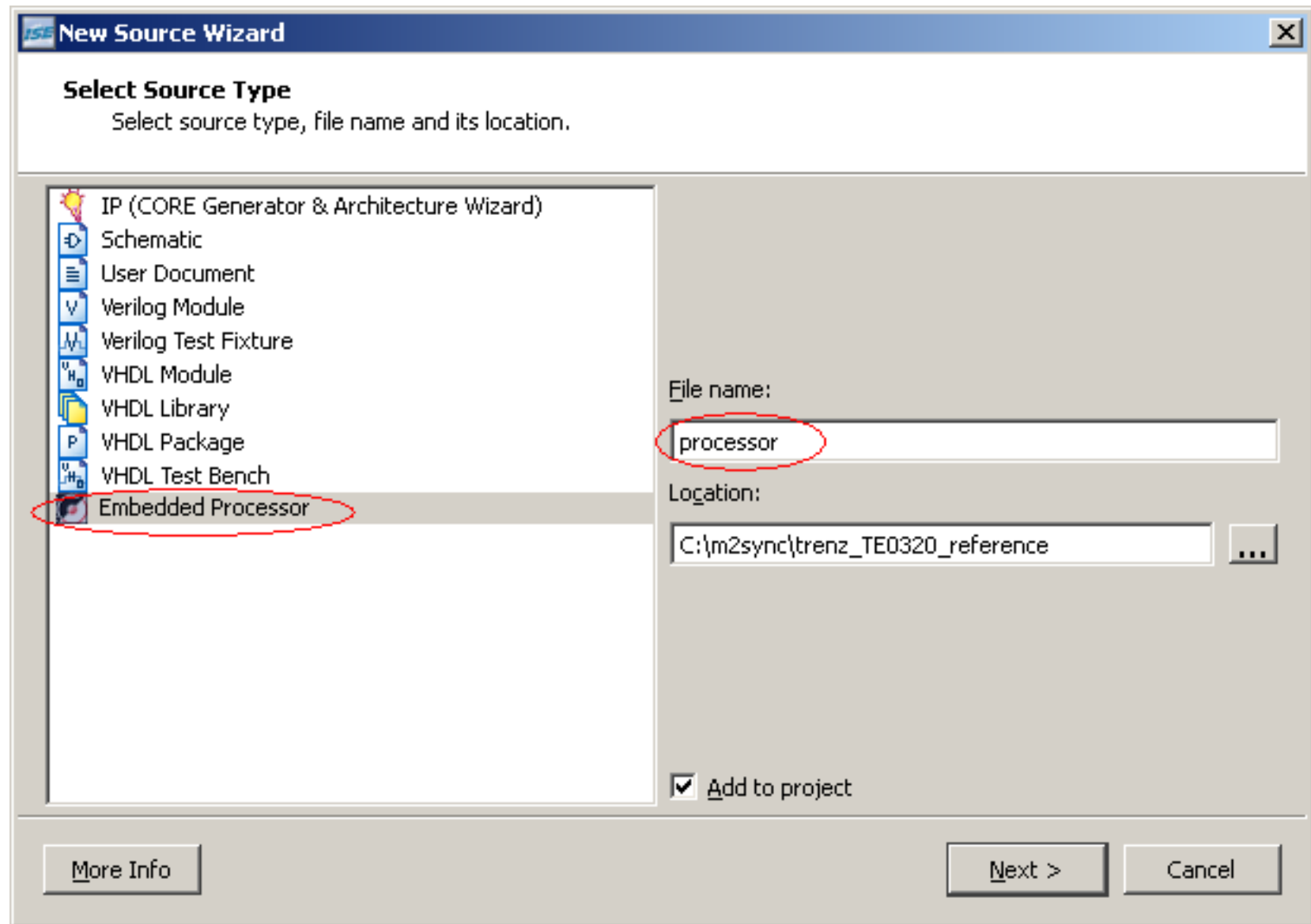
provide correct Family, Device, Package and Speed,
then click Next



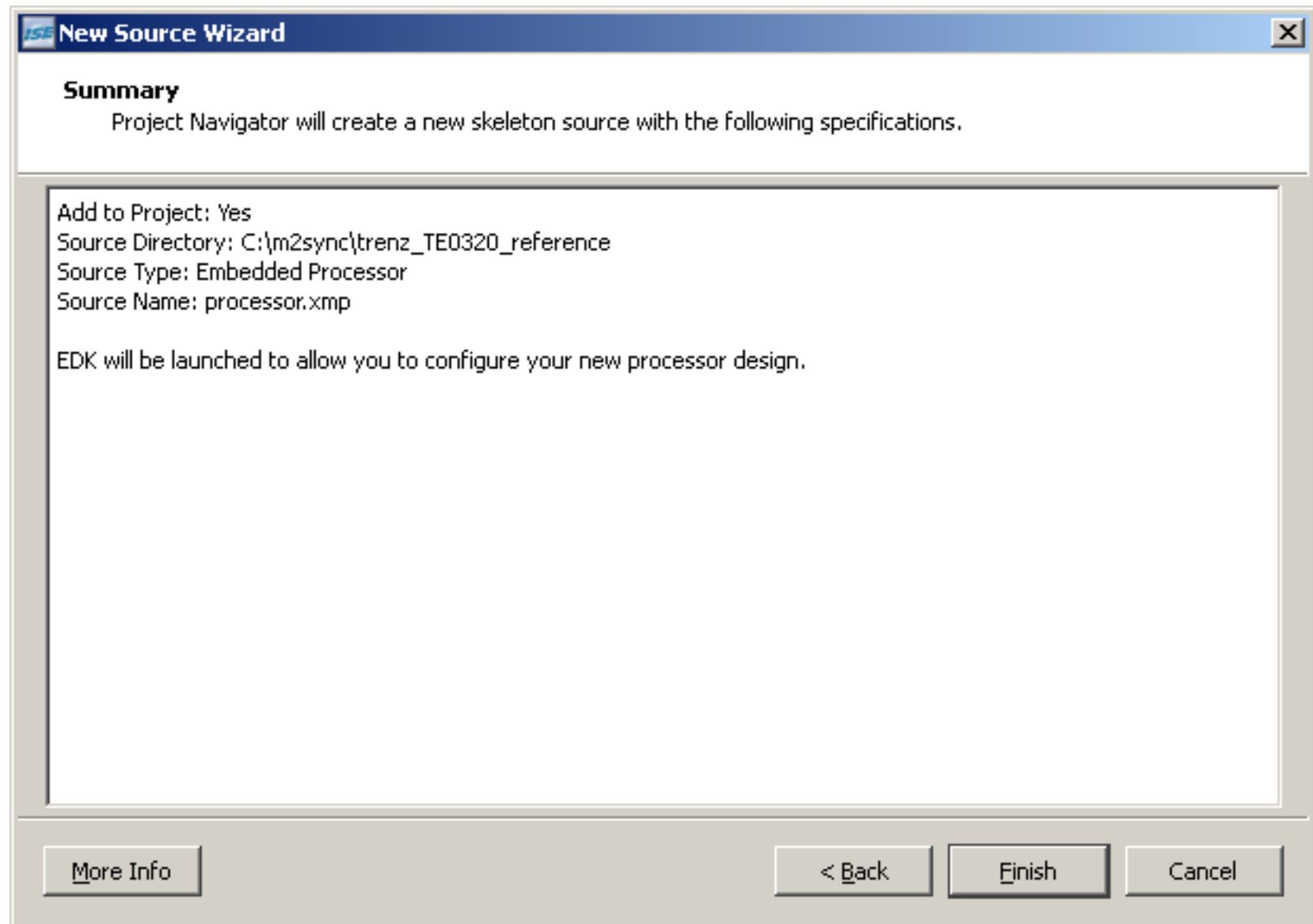
verify configuration and click Finish



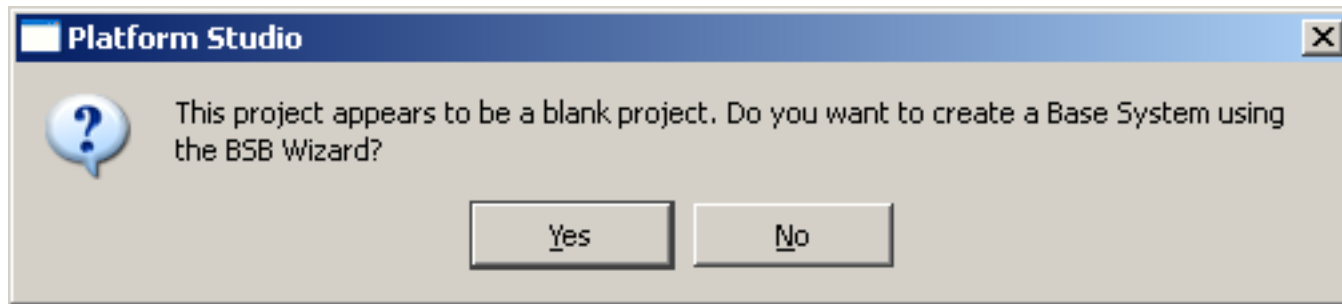
right button menu to add New Source



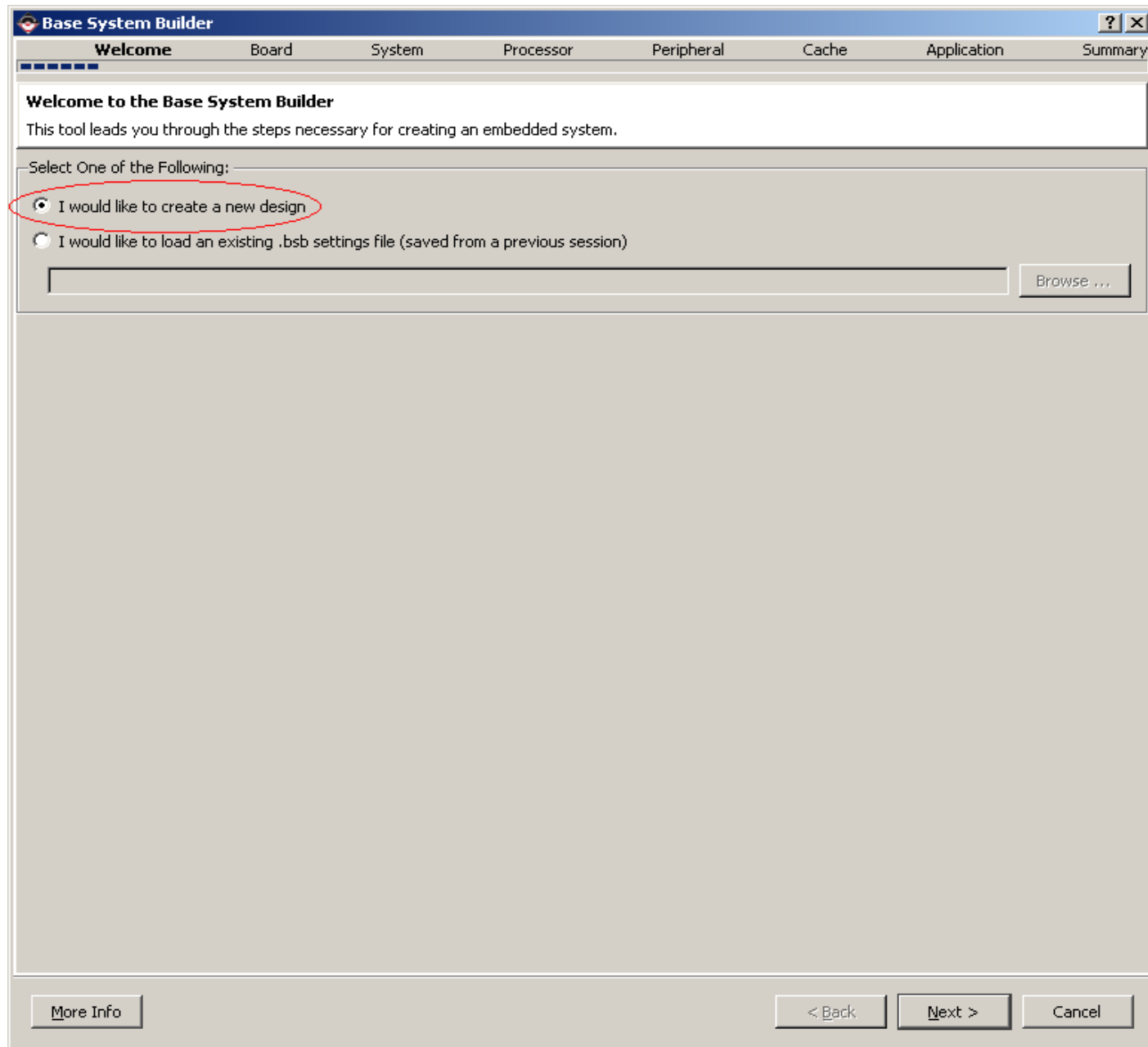
choose Embedded Processor, provide File name
then click Next



verify configuration then click Finish



confirm Yes to launch BSB Wizard



choose create new design then click Next

Base System Builder [?] [X]

Welcome **Board** System Processor Peripheral Cache Application Summary

Board Selection

Select a target development board.

Board

☒ I would like to create a system for the following development board

Board Vendor:

Board Name:

Board Revision:

☐ I would like to create a system for a custom board

Board Information

Architecture	Device	Package	Speed Grade
<input type="text" value="spartan3adsp"/>	<input type="text" value="xc3sd1800a"/>	<input type="text" value="fg676"/>	<input type="text" value="-4"/>

☐ Use Stepping

Reset Polarity:

Related Information

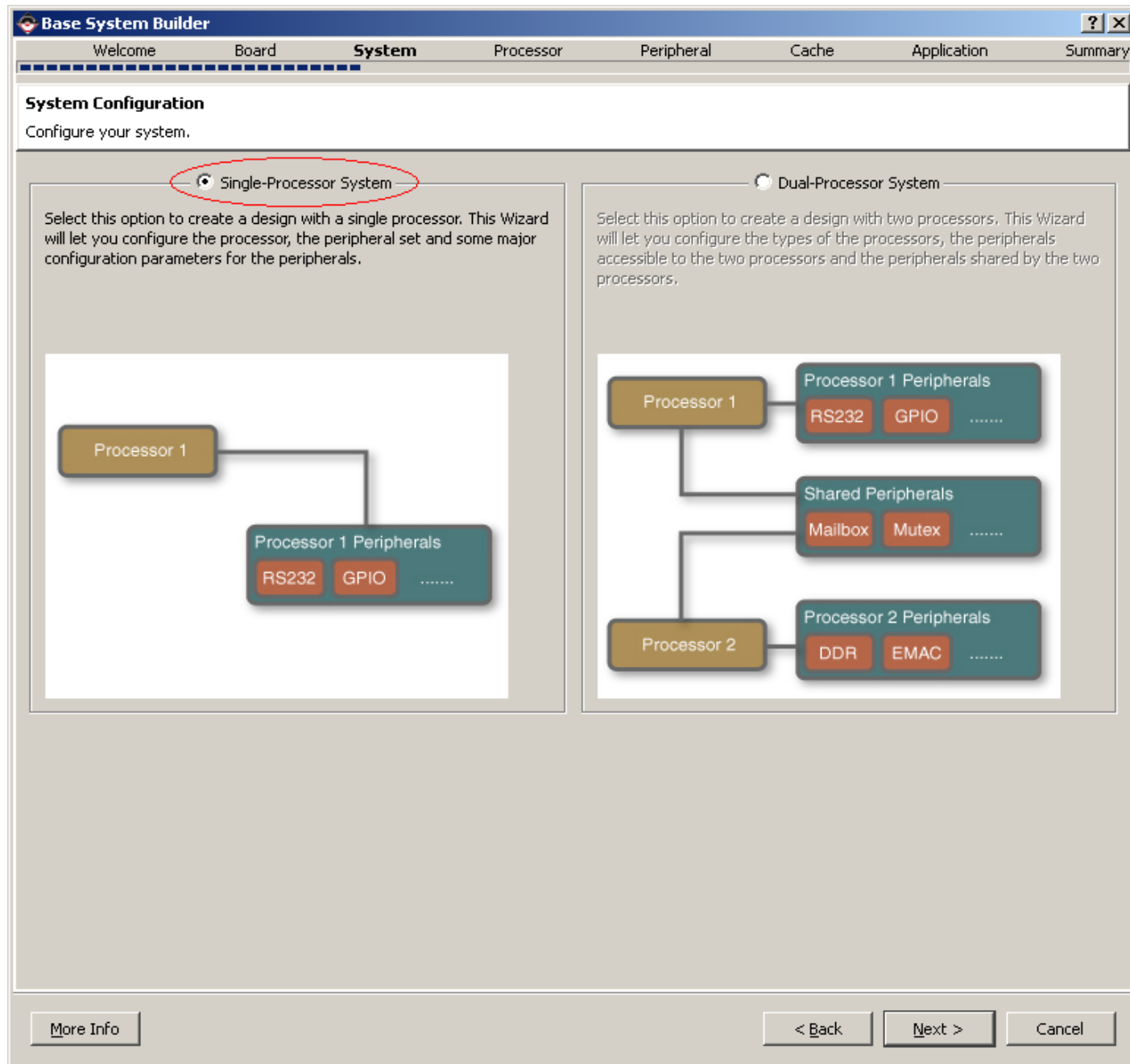
[Vendor's Website](#)

[Vendor's Contact Information](#)

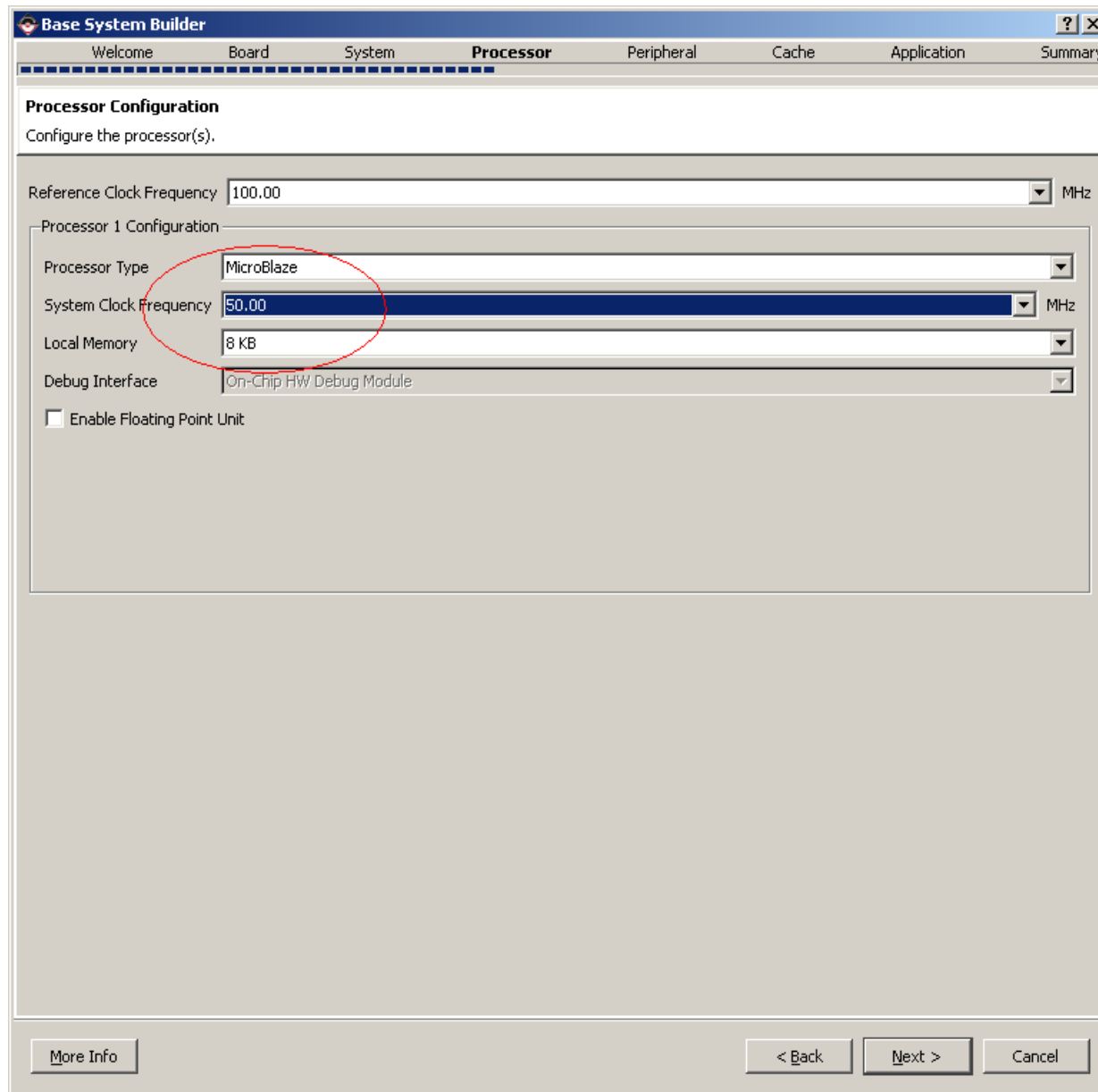
[Third Party Board Definition Files Download Website](#)

The FPGA Micromodule integrates a leading-edge Spartan-3A DSP FPGA, an USB2.0 microcontroller, DDR Ram, configuration Flash and power supply on a tiny footprint. A large number of configurable I/Os are provided via standard B2B connectors.

choose correct Vendor, Name and Revision then
click Next



choose Single-Processor System then click Next



The image shows a screenshot of the 'Base System Builder' application window, specifically the 'Processor' tab. The window has a title bar with a question mark and a close button. Below the title bar is a tabbed interface with tabs for 'Welcome', 'Board', 'System', 'Processor' (selected), 'Peripheral', 'Cache', 'Application', and 'Summary'. The main content area is titled 'Processor Configuration' and contains the instruction 'Configure the processor(s)'. It features several configuration options: 'Reference Clock Frequency' set to 100.00 MHz, 'Processor 1 Configuration' section with 'Processor Type' set to 'MicroBlaze', 'System Clock Frequency' set to 50.00 MHz, 'Local Memory' set to 8 KB, and 'Debug Interface' set to 'On-Chip HW Debug Module'. There is also an unchecked checkbox for 'Enable Floating Point Unit'. At the bottom of the window are three buttons: 'More Info', '< Back', and 'Next >', along with a 'Cancel' button.

Base System Builder

Welcome Board System **Processor** Peripheral Cache Application Summary

Processor Configuration
Configure the processor(s).

Reference Clock Frequency 100.00 MHz

Processor 1 Configuration

Processor Type MicroBlaze

System Clock Frequency 50.00 MHz

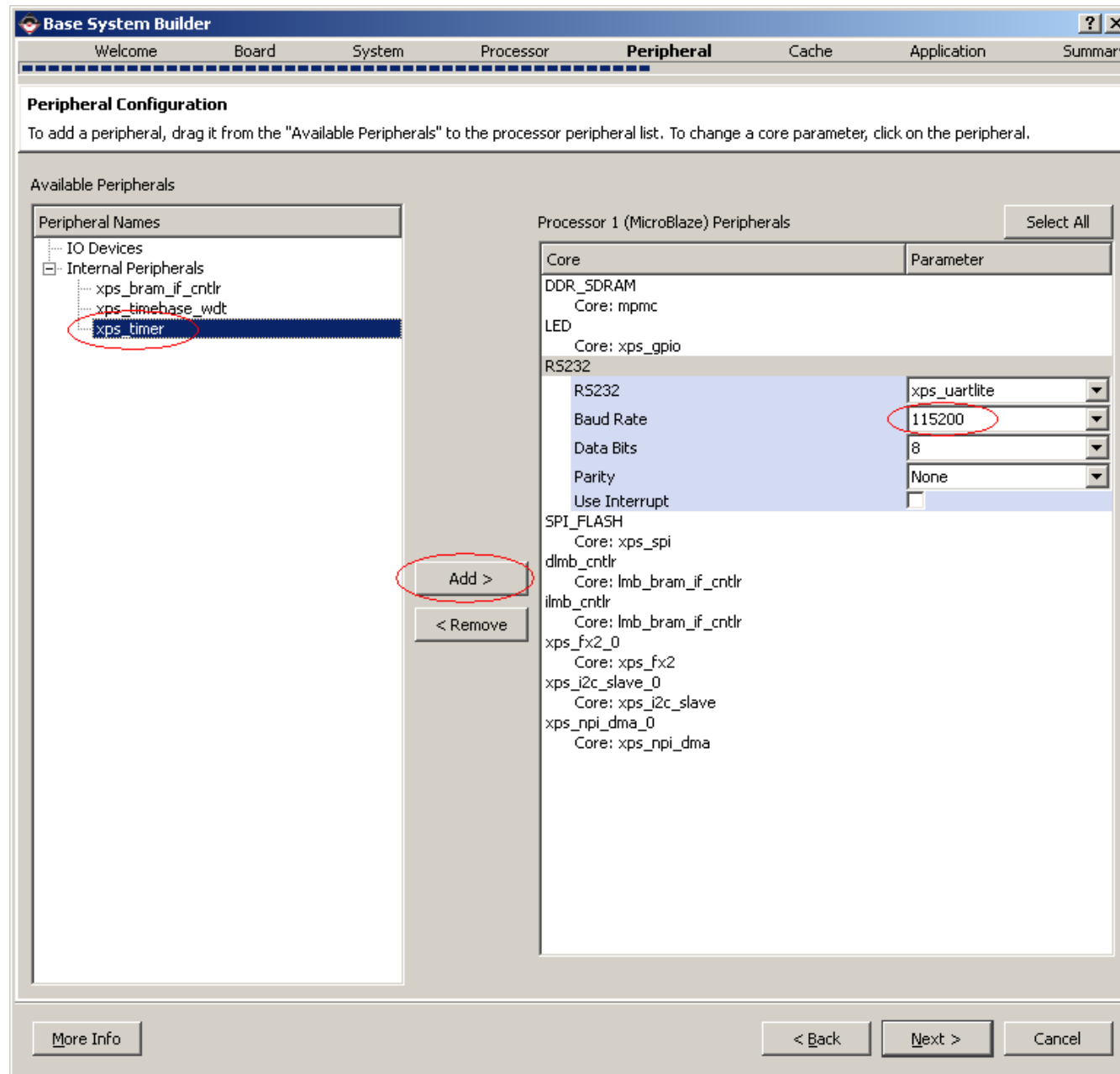
Local Memory 8 KB

Debug Interface On-Chip HW Debug Module

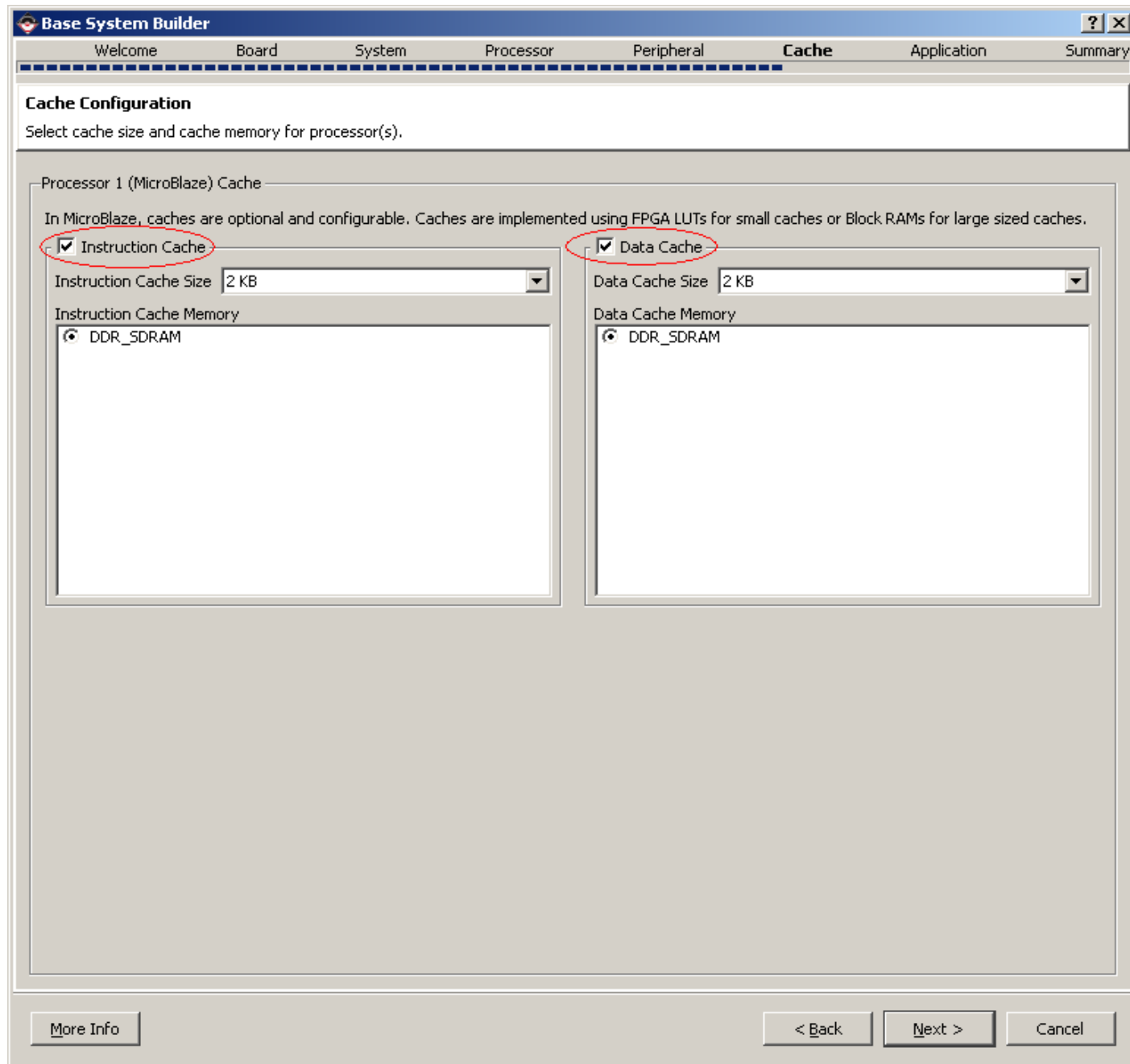
☐ Enable Floating Point Unit

More Info < Back Next > Cancel

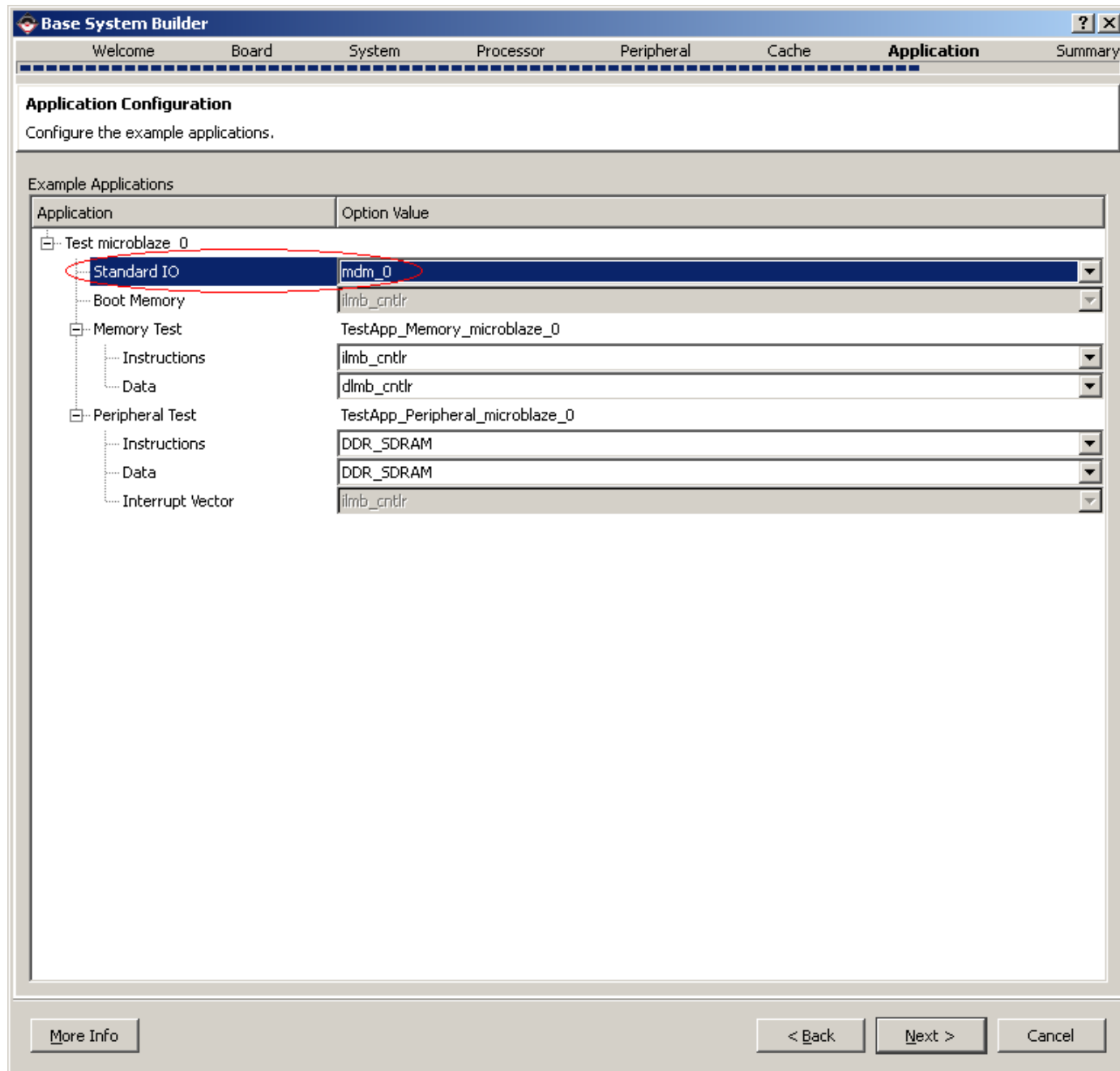
choose default Processor Type, System Clock Frequency (it should be 1/2 of the reference clock) and Local Memory size then click Next



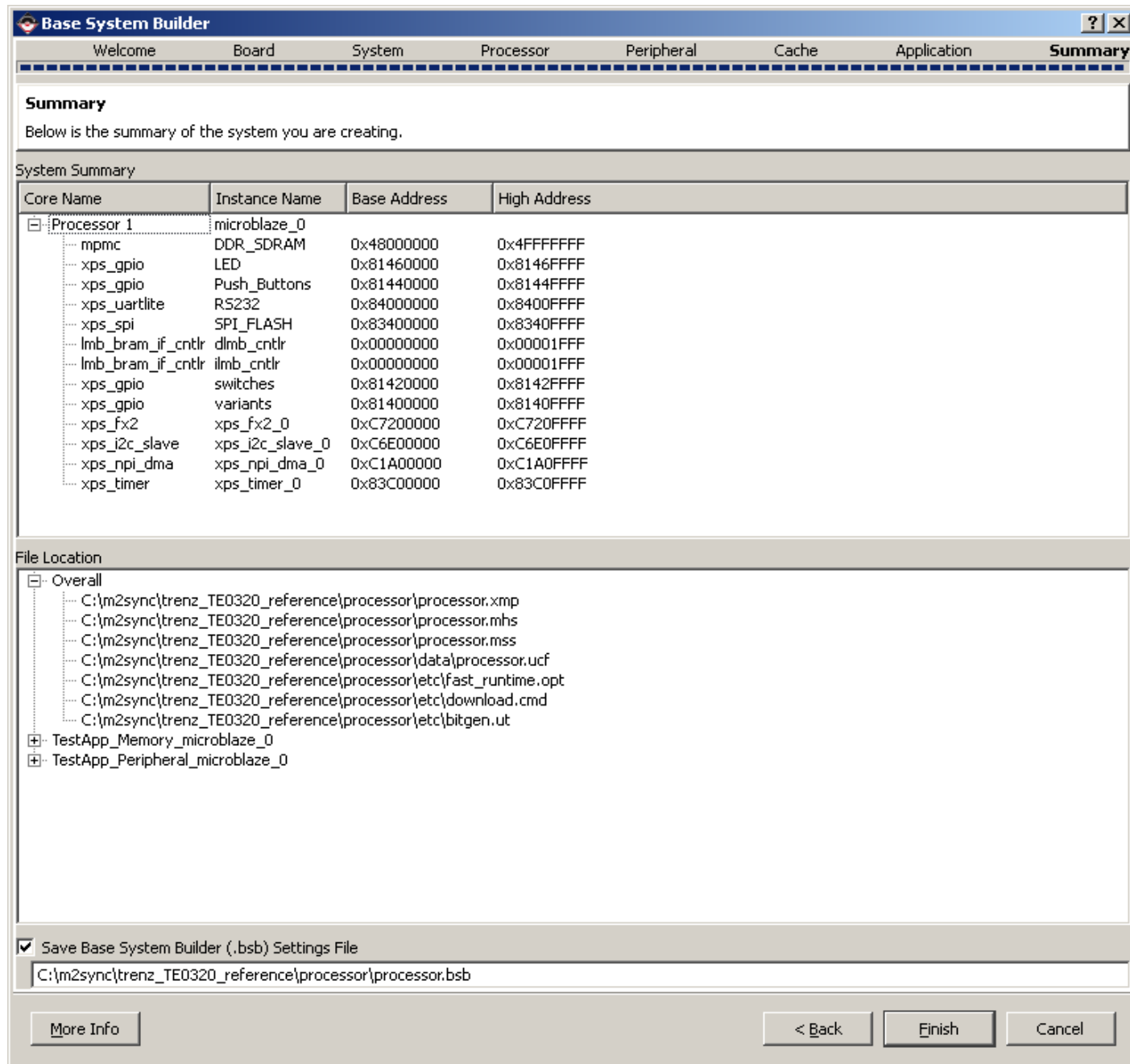
add xps_timer (XilKernel required), correct default
UART speed then click Next



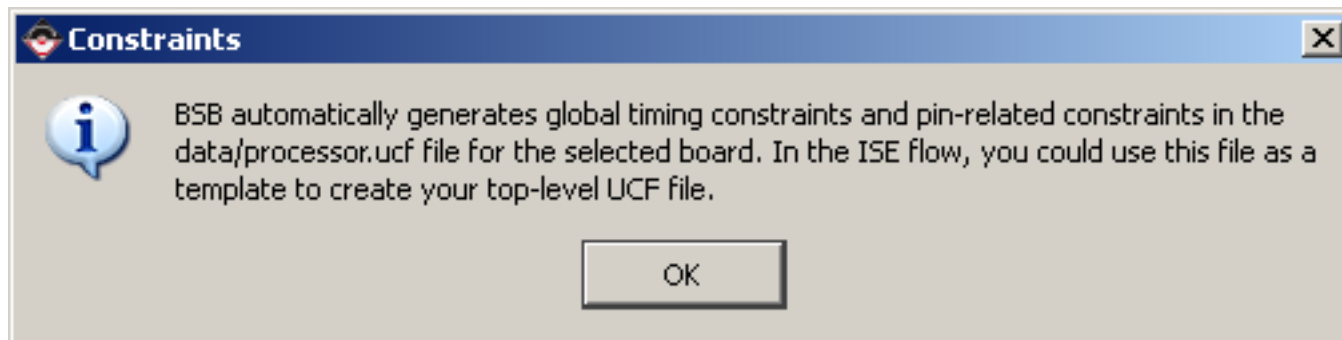
enable Instruction and Data Caches then click Next



choose mdm_0 as Standard IO then click Next



verify created configuration then click Finish



confirm UCF file creation

Xilinx Platform Studio - C:\m2sync\trenz_TE0320_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project Platform

Project Files

- MHS File: processor.mhs
- MSS File: processor.mss
- UCF File: data/processor.ucf
- IMPACT Command File: etc/do
- Implementation Options File: e
- Bitgen Options File: etc/bitgen

Project Options

- Device: xc3sd1800afg676-4
- Netlist: SubModule
- Implementation: Project Navig
- HDL: vhdl
- Sim Model: BEHAVIORAL

Design Summary

Legend

- Master Slave Master/Slave Target Initiator
- Connected Unconnected Monitor
- Production License (paid) License (eval) Local Pre Production Beta Development
- Superseded Discontinued

Bus Interfaces Ports Addresses

Name	Bus Name	IP Type
dmb		lmb_v10
ilmb		lmb_v10
mb_plb		plb_v46
microblaze_0		microblaze
lmb_bram		bram_block
dmb_cntlr		lmb_bram_if..
ilmb_cntlr		lmb_bram_if..
DDR_SDRAM		mpmc
mdm_0		mdm
xps_fx2_0		xps_fx2
SPLB	mb_plb	
FIFO_IN	xps_npi_dma_0_DMA_OUT	
FIFO_OUT	xps_fx2_0_FIFO_OUT	
LED		xps_gpio
Push_Buttons		xps_gpio
switches		xps_gpio
variants		xps_gpio
xps_i2c_slave_0		xps_i2c_slav
xps_npi_dma_0		xps_npi_dma
SPLB	mb_plb	
DMA_IN	xps_fx2_0_FIFO_OUT	
DMA_OUT	xps_npi_dma_0_DMA_OUT	

Bus Interface Filters

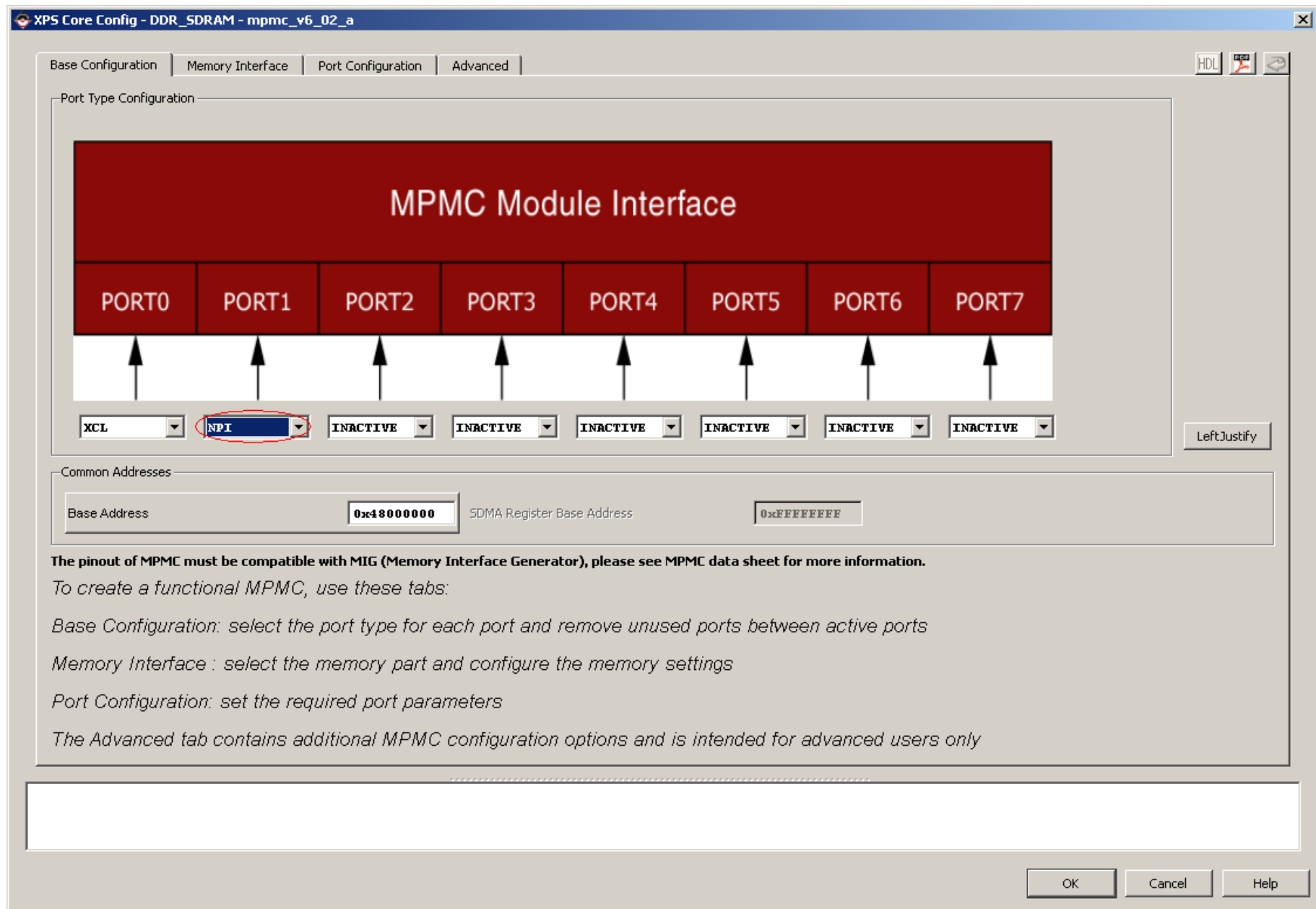
- By Connection
 - Connected
 - Unconnected
- By Bus Standard
 - LMB
 - PLBV46
- Xilinx Point To Point
 - XIL_BRAM
 - XIL_BSCAN
 - XIL_MBDEBUG3
 - XIL_MBTRACE2
 - XIL_MEMORY_C...
 - XIL_NPI
- User Defined
- By Interface Type
 - Slaves
 - Masters
 - Master Slaves
 - Monitors
 - Targets
 - Initiators

Console

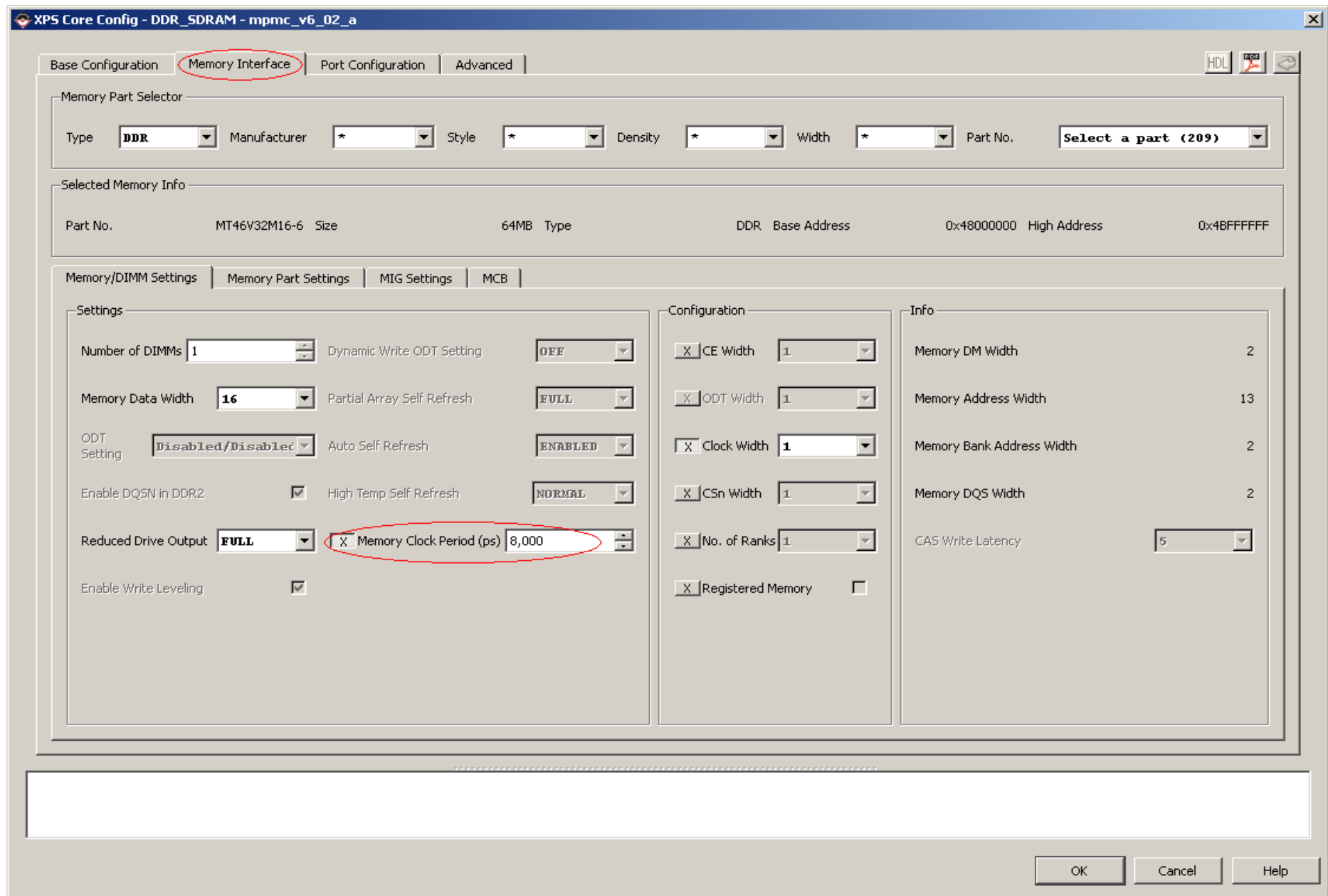
```
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
```

Console Warnings Errors

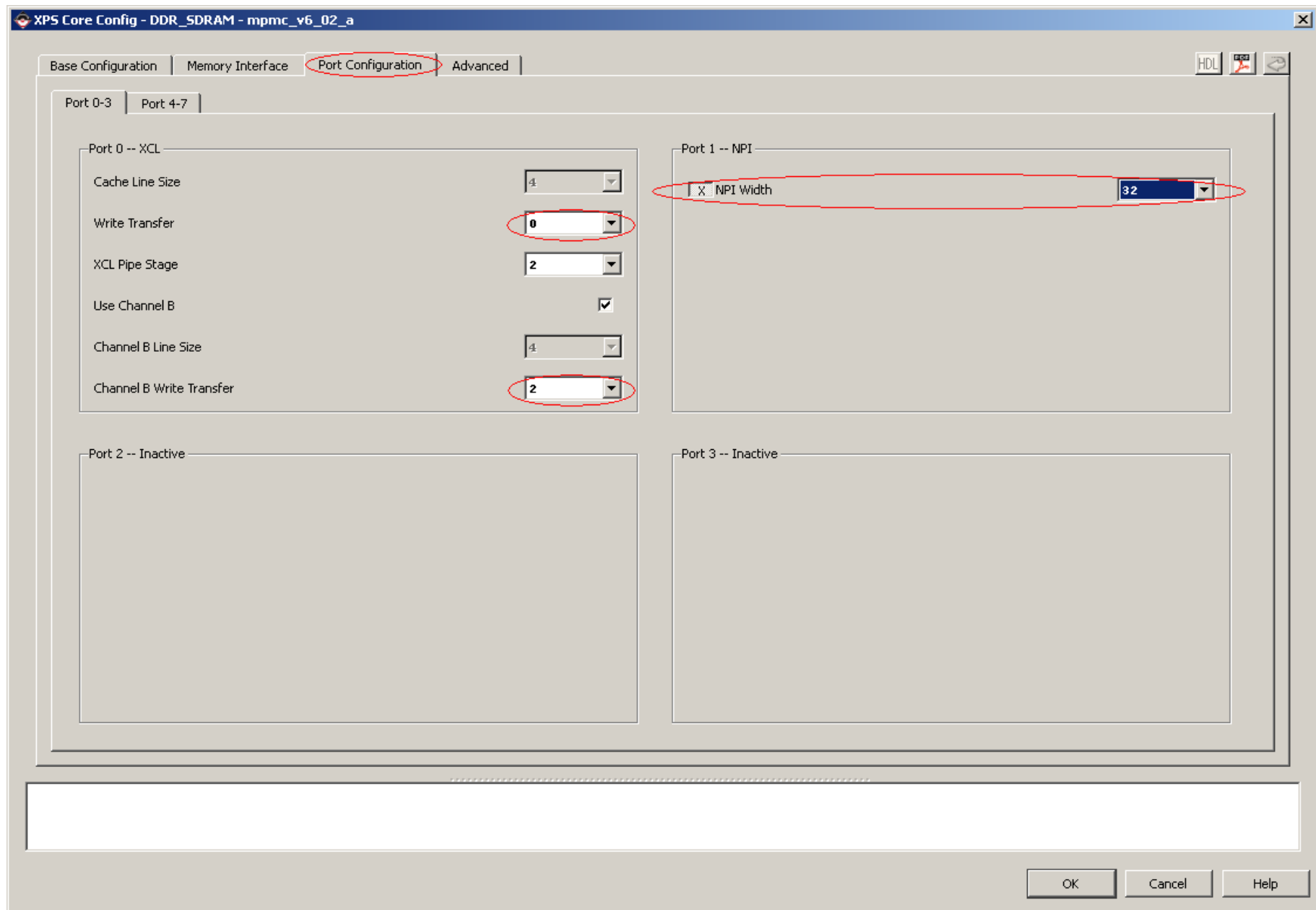
connect np_i_dma and fx2 pcores to each other



double click on DDR_SDRAM pcore and configure NPI port



switch to Memory Interface tab and activate Clock Period (8000 ps for 125Mhz, 10000 ps for 100Mhz)



switch to Port Configuration tab, correct Write Transfers and NPI Width then click OK

Xilinx Platform Studio - C:\m2sync\trenz_TE0320_reference\processor\processor.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project Platform

Project Files

- MHS File: processor.mhs
- MSS File: processor.mss
- UCF File: data/processor.ucf
- IMPACT Command File: etc/do
- Implementation Options File: e
- Bitgen Options File: etc/bitger

Project Options

- Device: xc3sd1800afg676-4
- Netlist: SubModule
- Implementation: Project Navig
- HDL: vhdl
- Sim Model: BEHAVIORAL

Design Summary

Legend

- Master Slave Master/Slave Target Initiator
- Connected Unconnected Monitor
- Production License (paid) License (eval) Local Pre Production Beta Development
- Superseded Discontinued

Bus Interfaces Ports Addresses

Name	Bus Name	IP Type
dmb		lmb_v10
ilmb		lmb_v10
mb_plb		plb_v46
microblaze_0		microblaz
lmb_bram		bram_blo
dmb_cntlr		lmb_bram
ilmb_cntlr		lmb_bram
DDR_SDRAM		mpmc
XCL0	microblaze_0_IXCL	
XCL0_B	microblaze_0_DXCL	
MPMC_PIM1	xps_npi_dma_0_MPMC_PIM	
mdm_0		mdm
xps_fx2_0		xps_fx2
LED		xps_gpio
Push_Buttons		xps_gpio
switches		xps_gpio
variants		xps_gpio
xps_i2c_slave_0		xps_i2c_s
xps_npi_dma_0		xps_npi_i
SPI_FLASH		xps_spi
xps_timer_0		xps_timer
RS232		xps_uartl

Bus Interface Filters

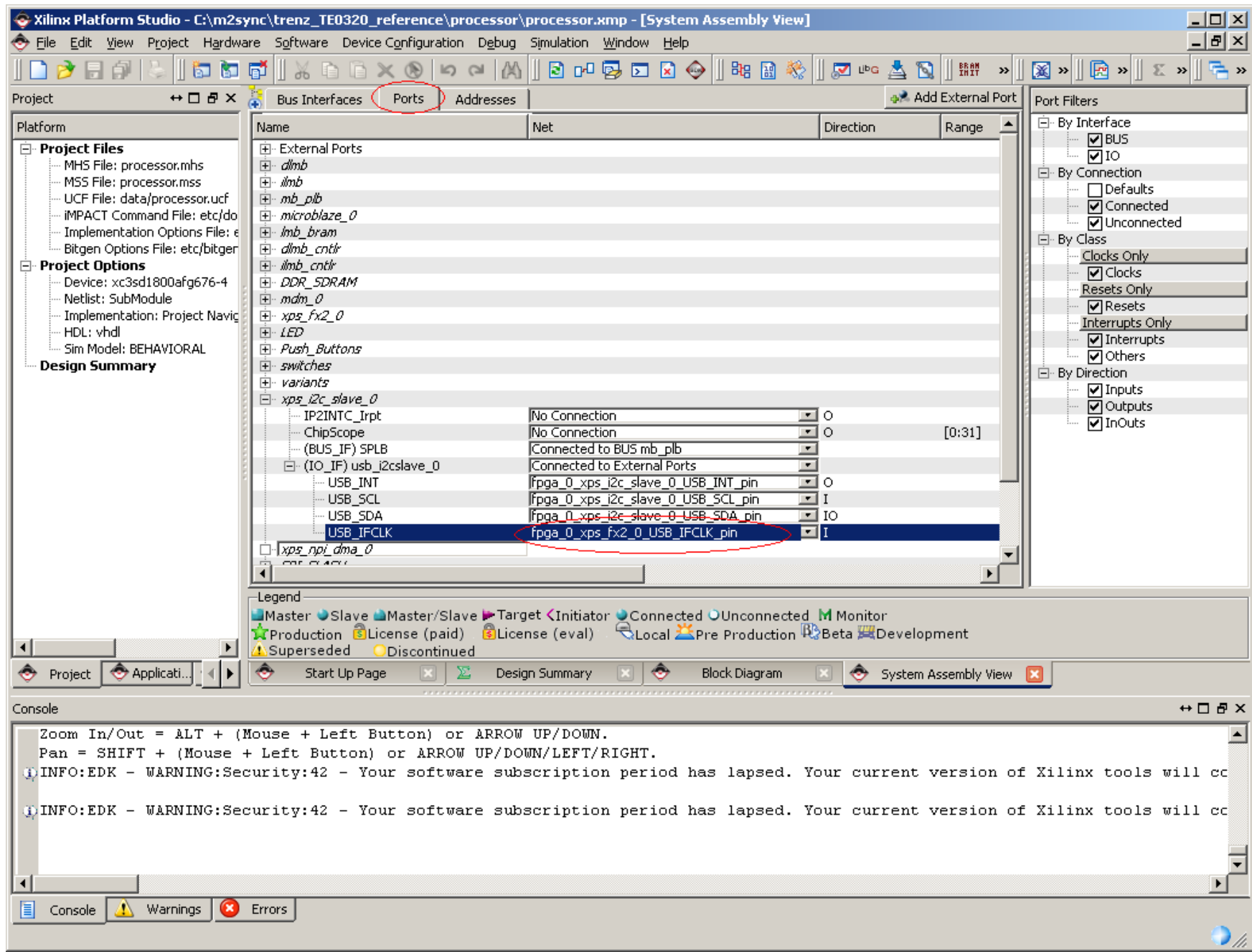
- By Connection
 - Connected
 - Unconnected
- By Bus Standard
 - LMB
 - PLBV46
- Xilinx Point To Point
 - XIL_BRAM
 - XIL_BSCAN
 - XIL_MBDEBUG3
 - XIL_MBTRACE2
 - XIL_MEMORY_C...
 - XIL_NPI
- User Defined
- By Interface Type
 - Slaves
 - Masters
 - Master Slaves
 - Monitors
 - Targets
 - Initiators

Console

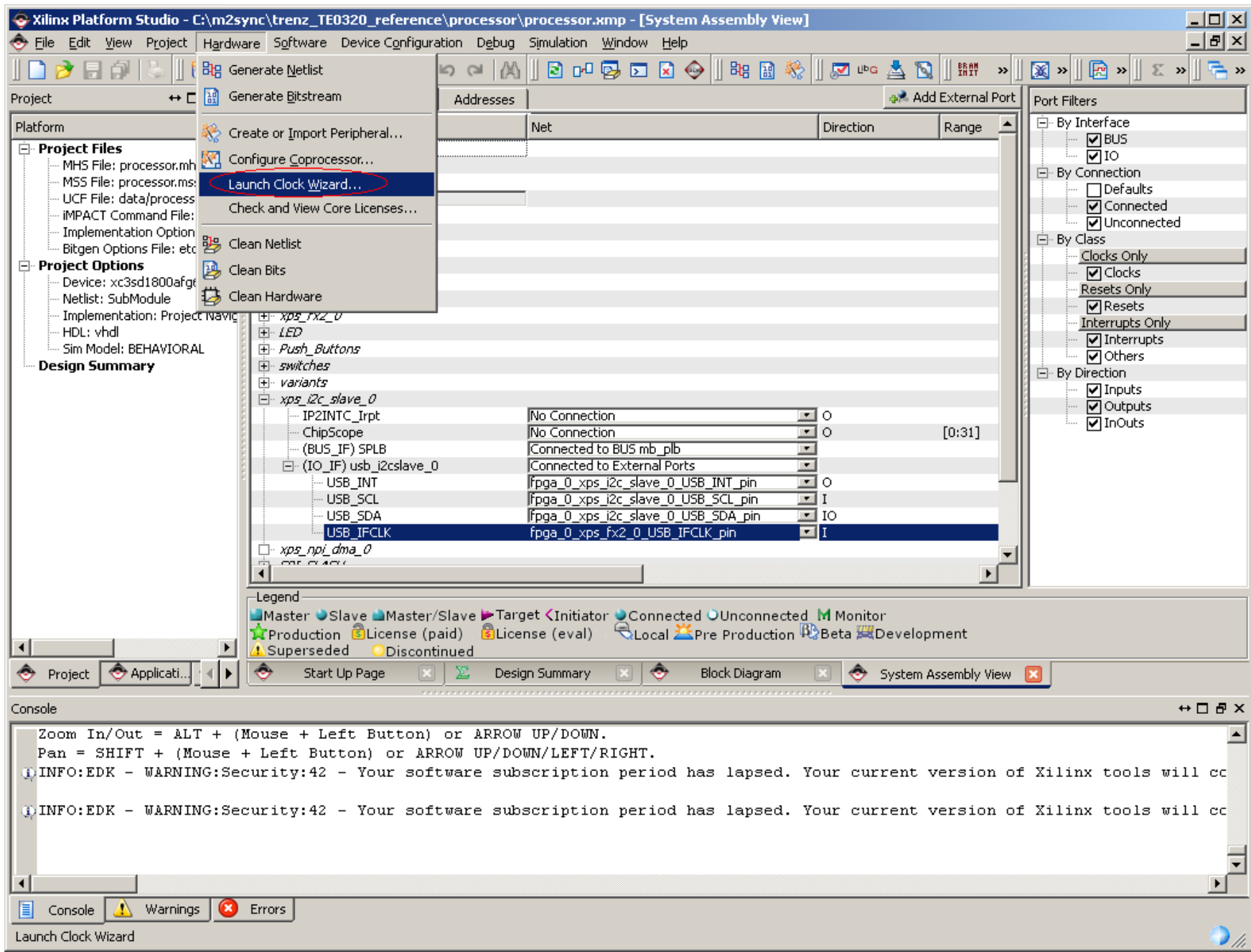
```
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
INFO:EDK - WARNING:Security:42 - Your software subscription period has lapsed. Your current version of Xilinx tools will cc
```

Console Warnings Errors

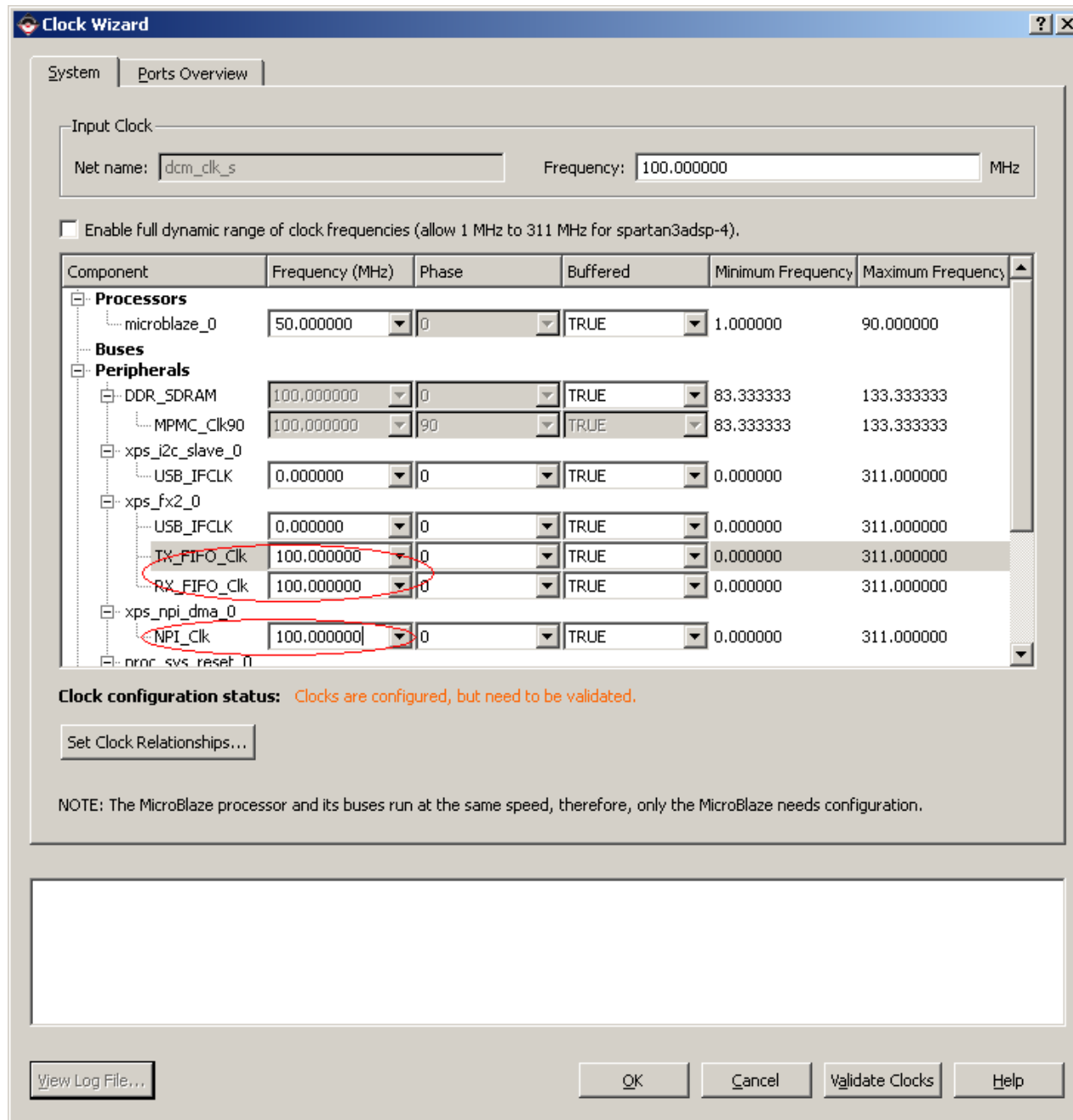
connect mpmc and npi_dma pcores



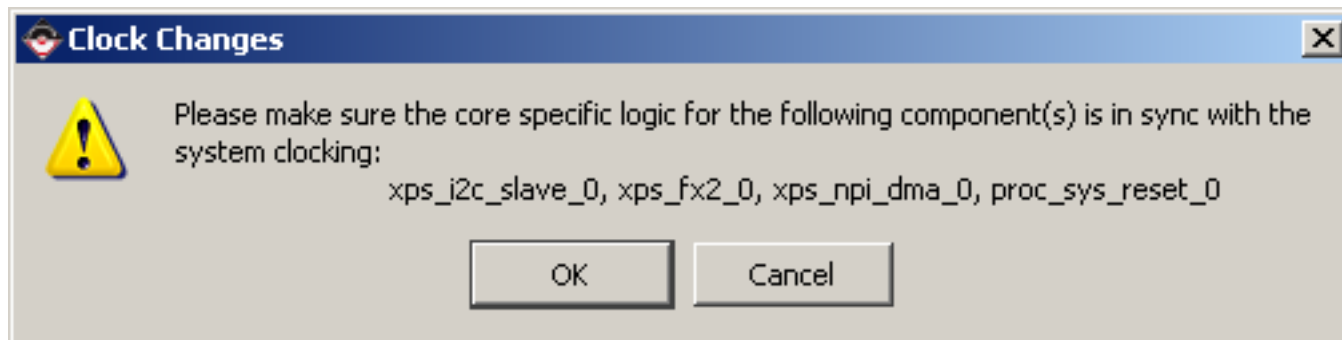
switch to Ports tab and assign xps_i2c_slave clock



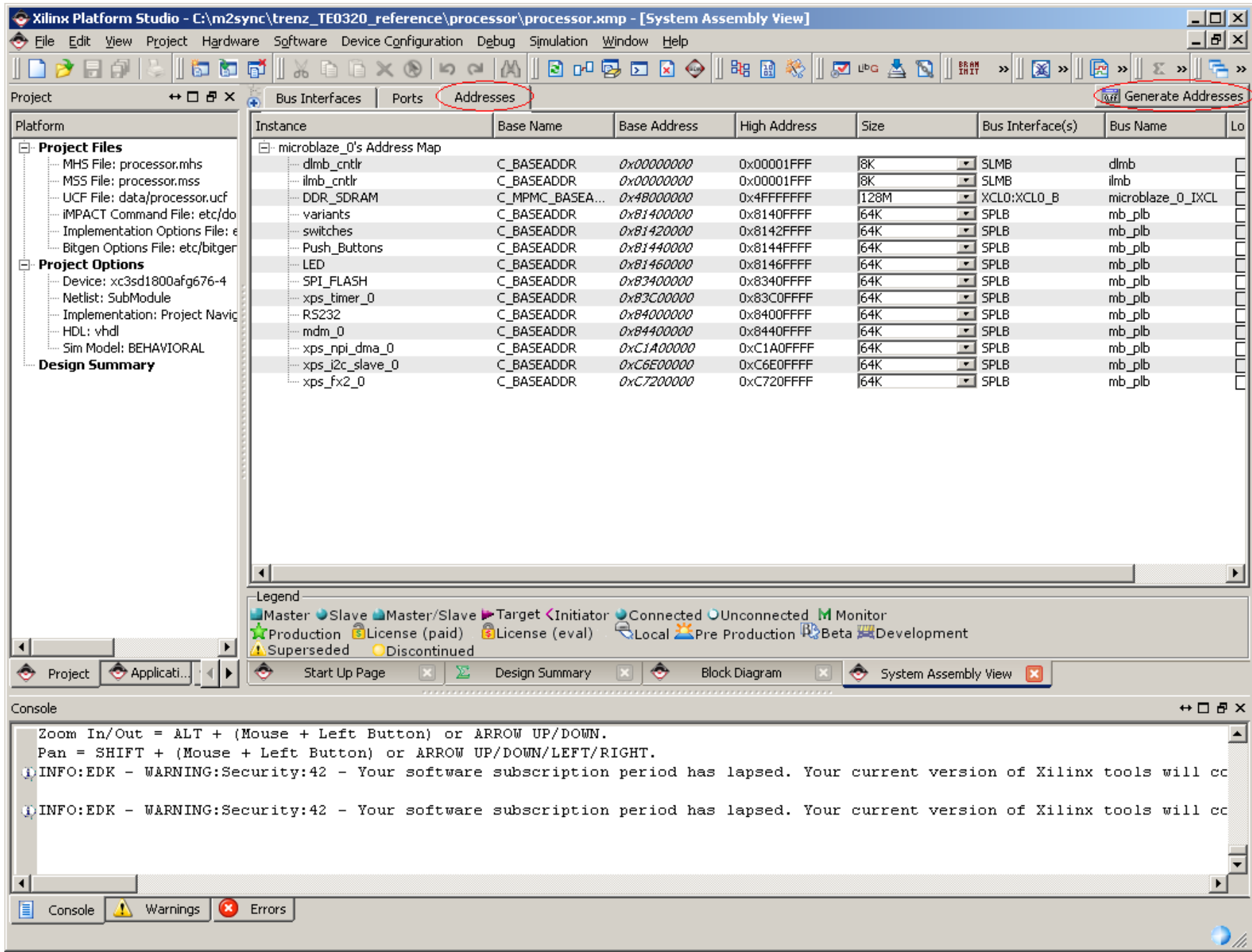
launch Clock Wizard



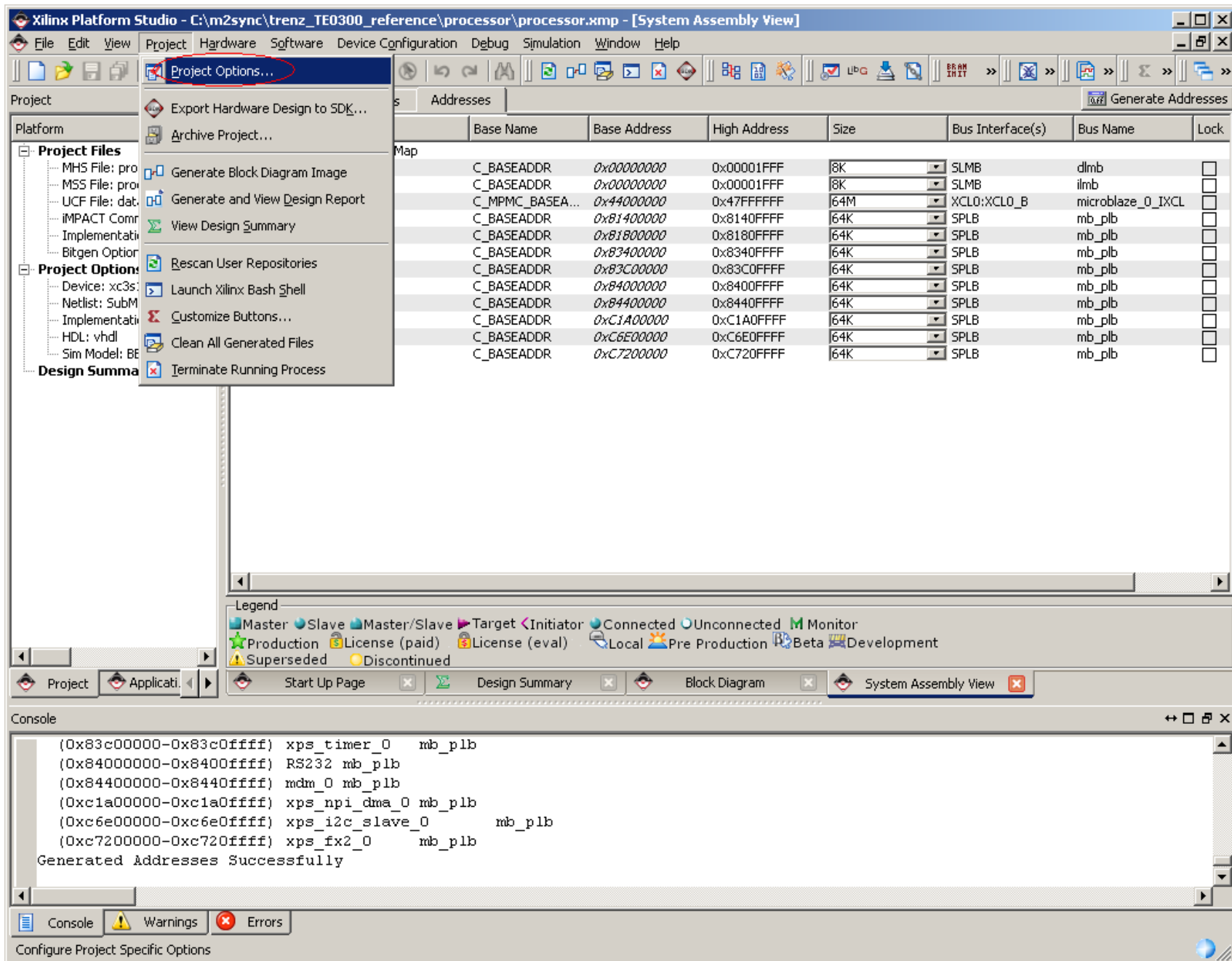
assign xps_fx2 and xps_npi clocks, re-validate then
click OK



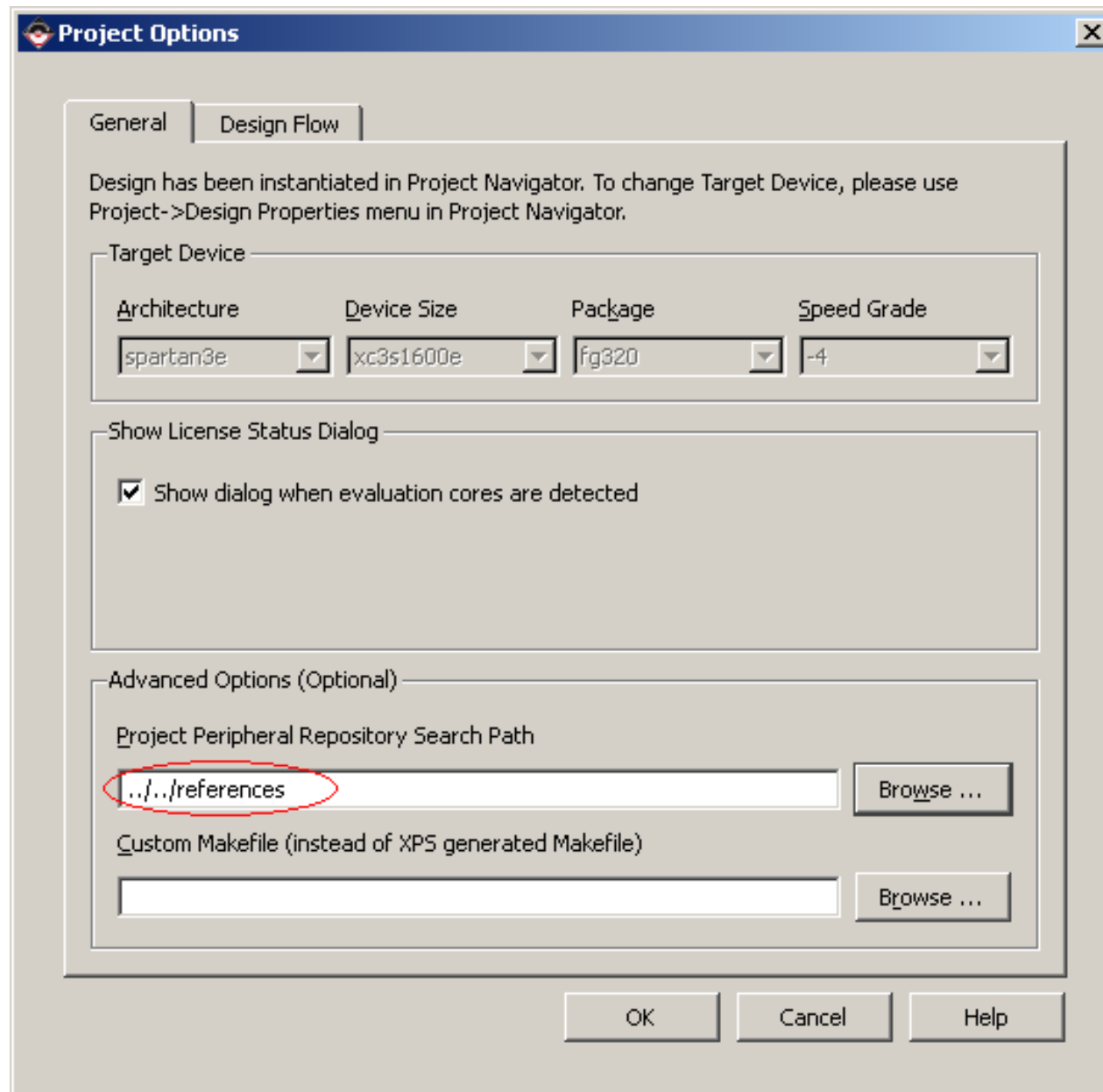
confirm Clock Changes



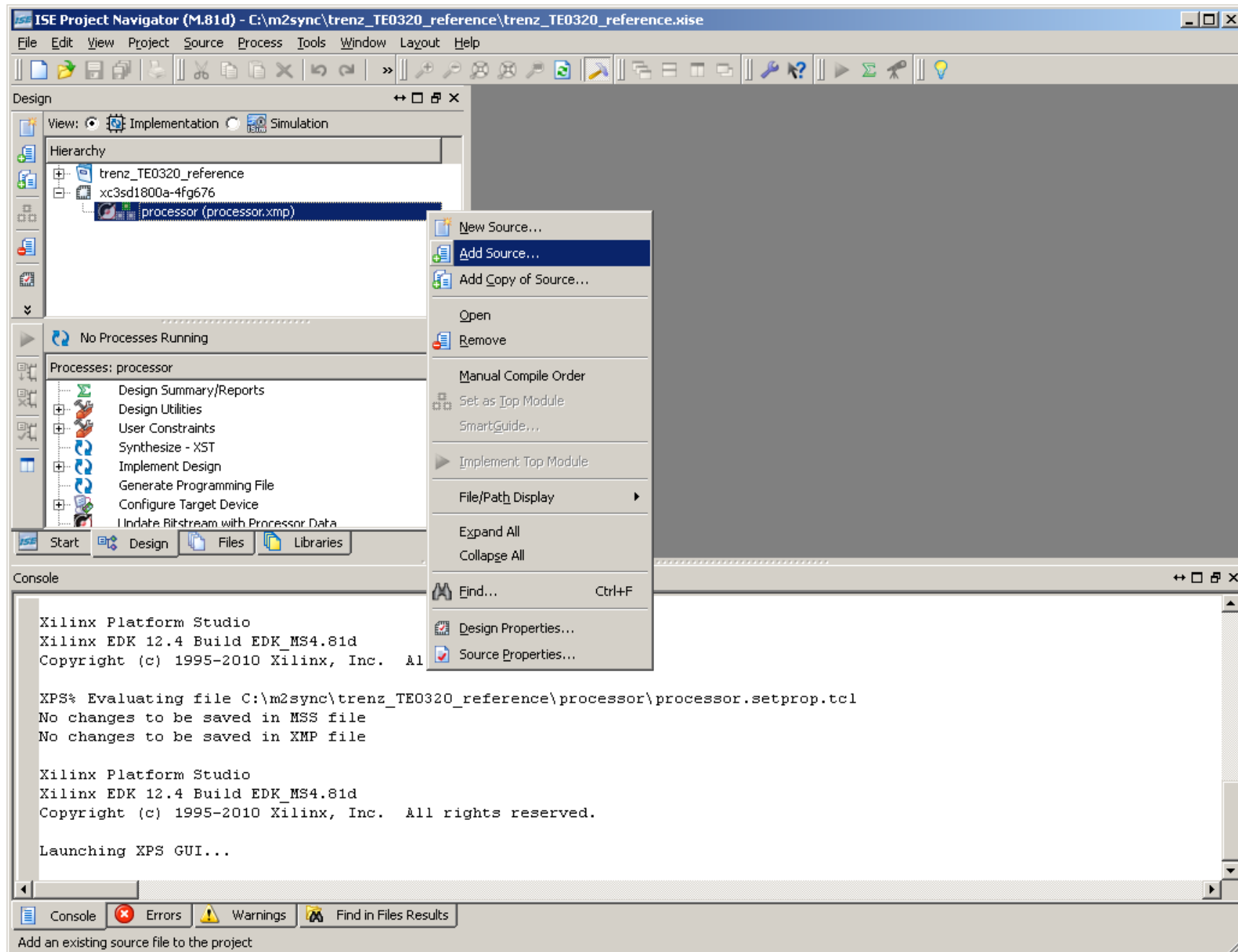
switch to Addresses tab and re-generate addresses



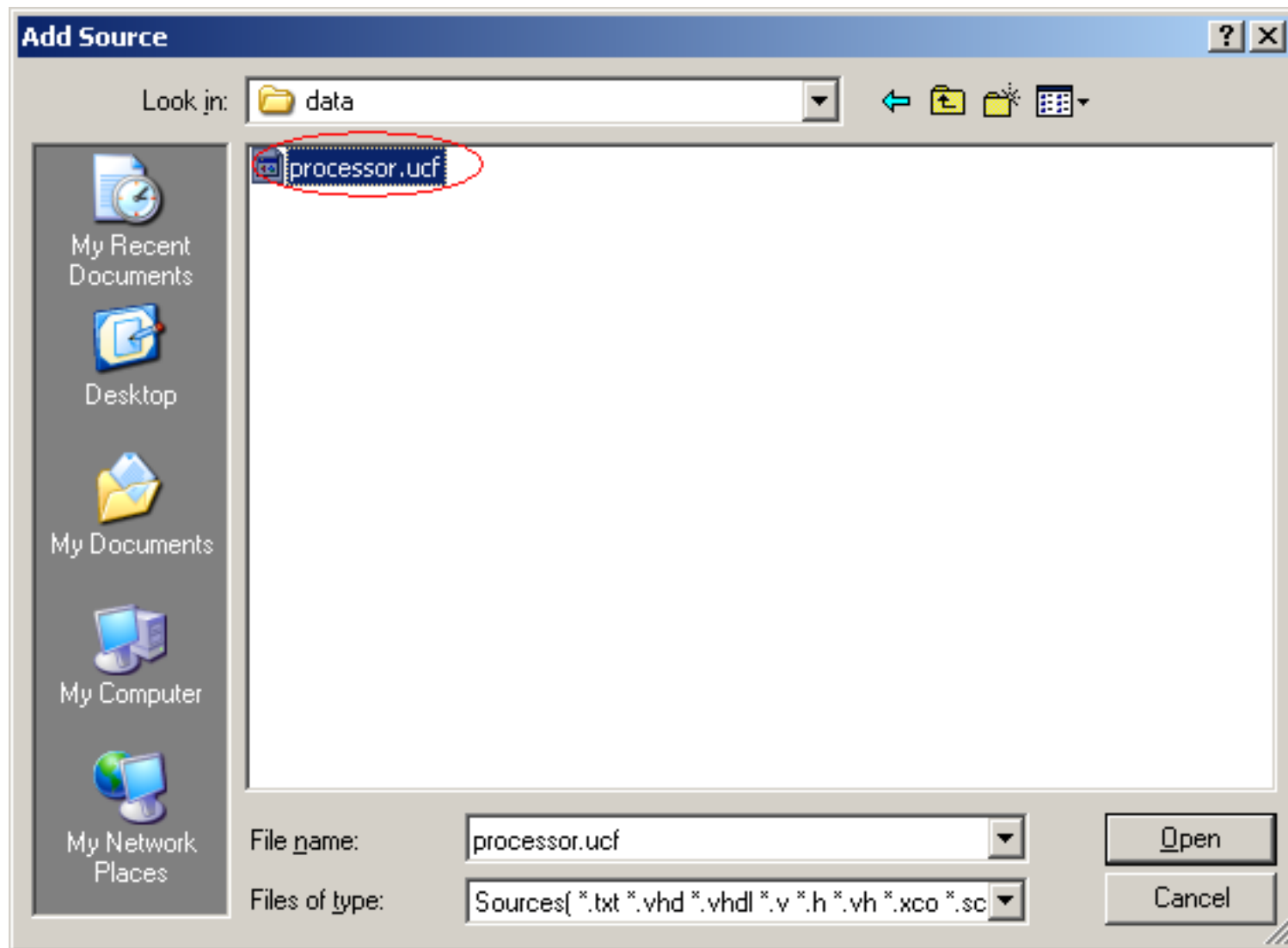
launch Project Options



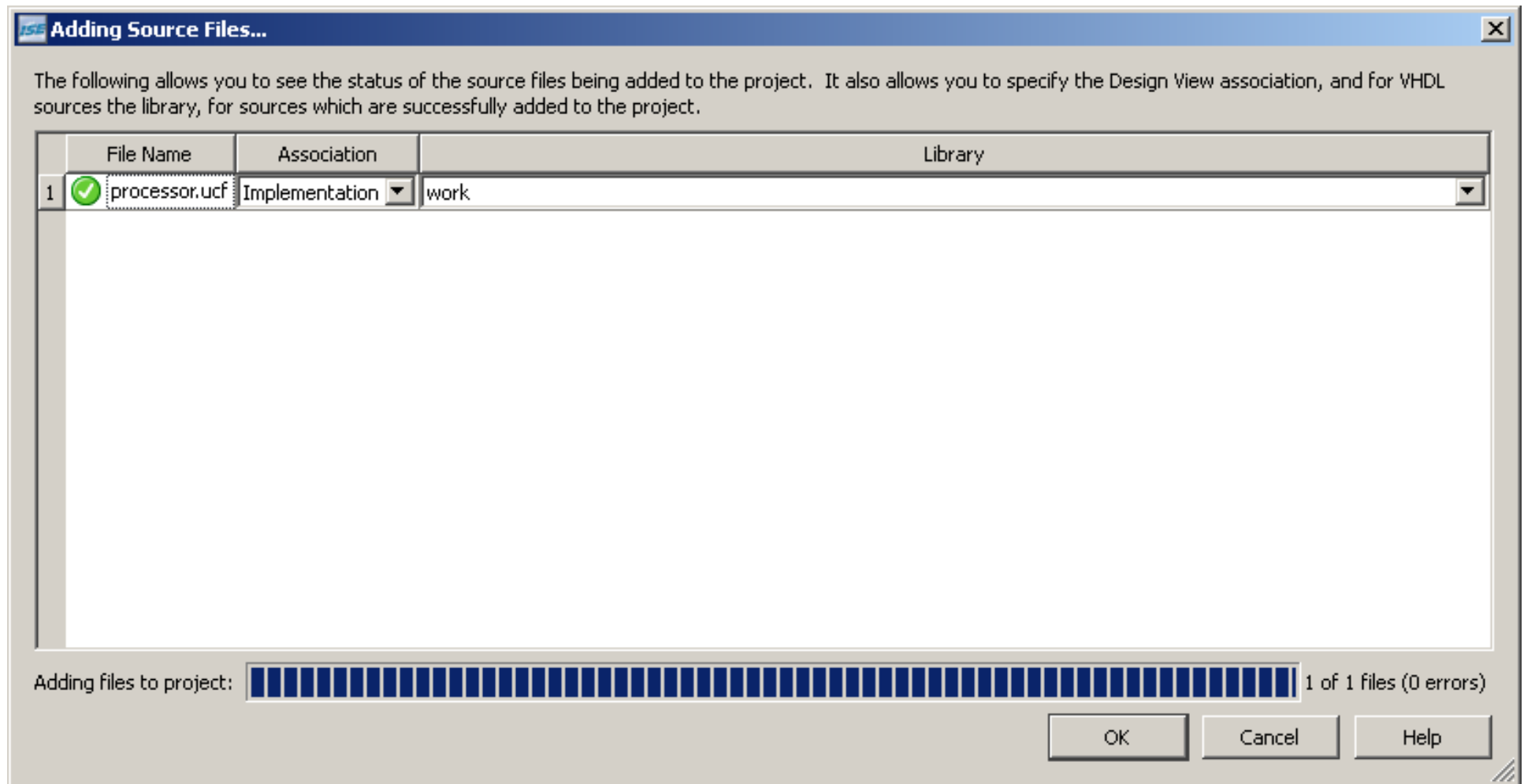
provide path to the private pcores (npi_dma, fx2, i2c_slave) then click OK



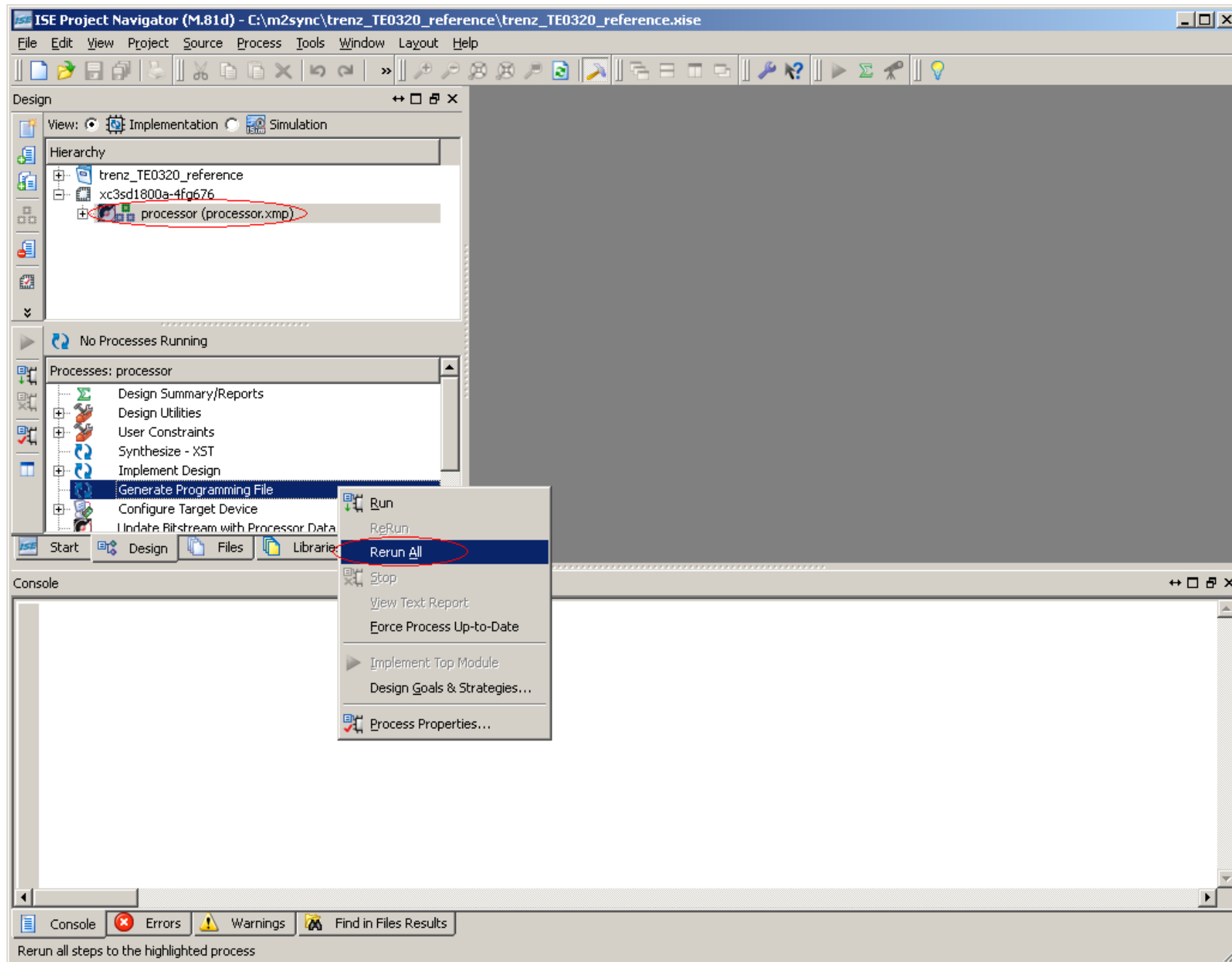
return to ISE Project Navigator and add Source



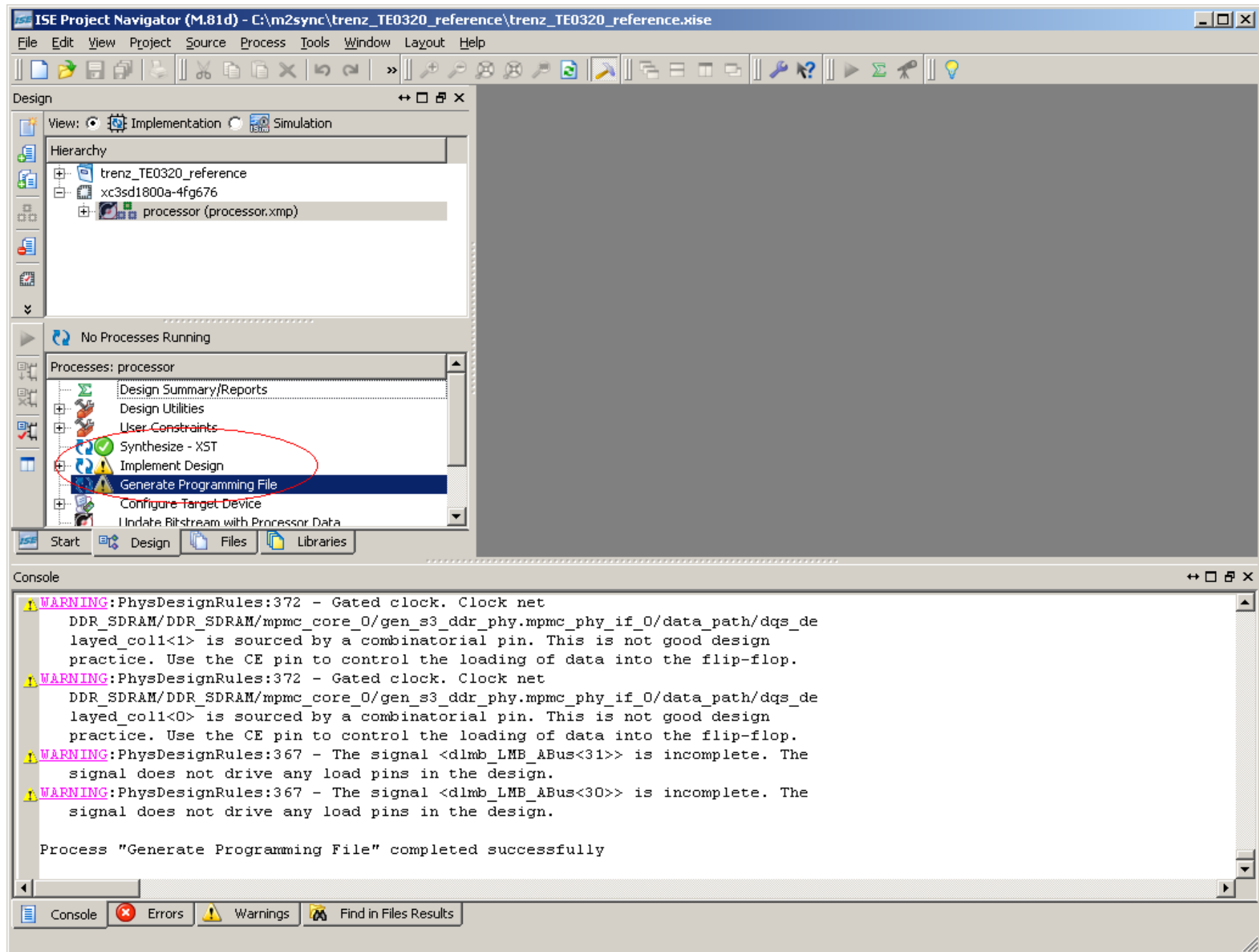
choose processor.ucf from processor/data/ subfolder
then click Open



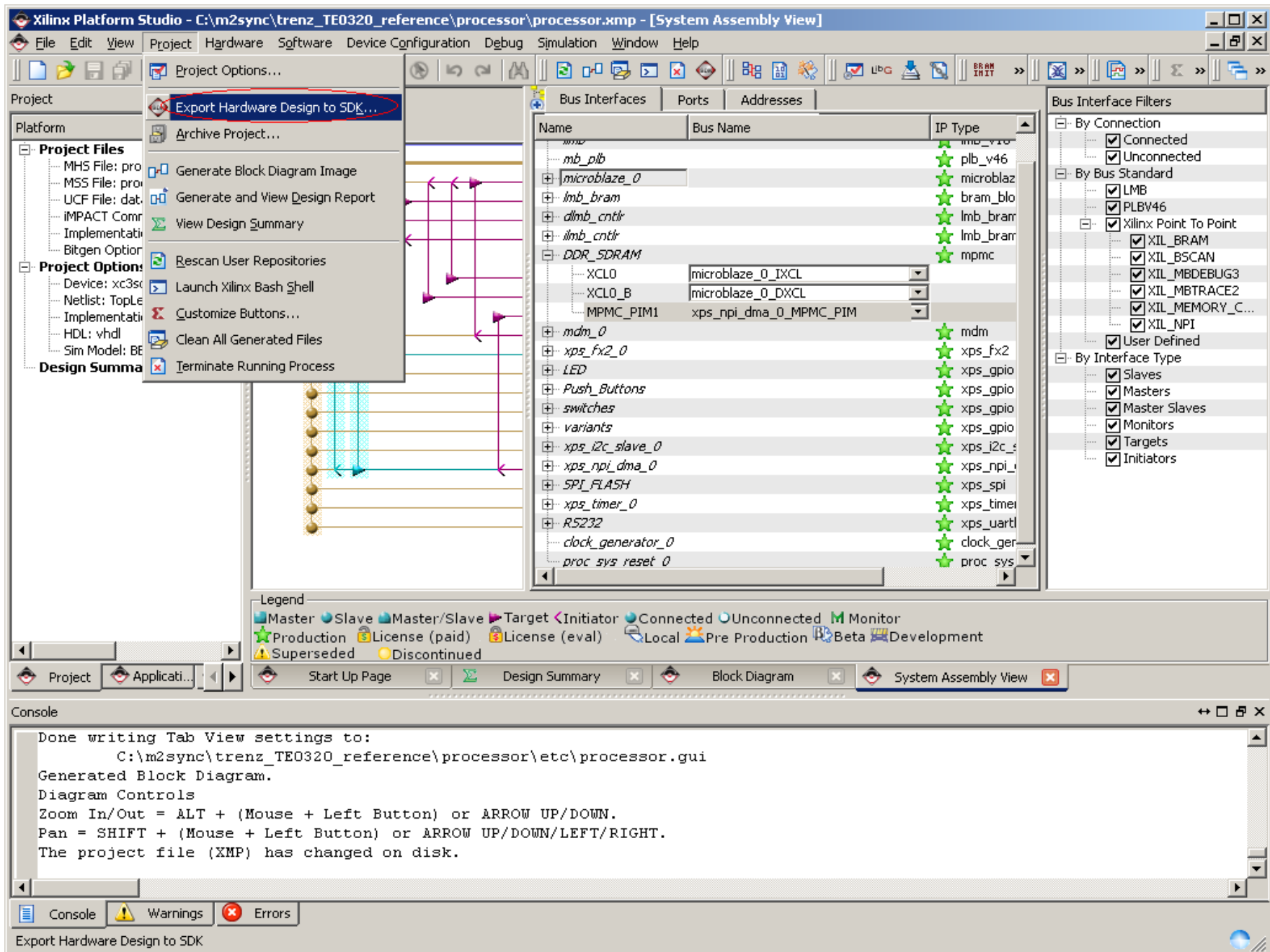
confirm adding Source File by clicking OK



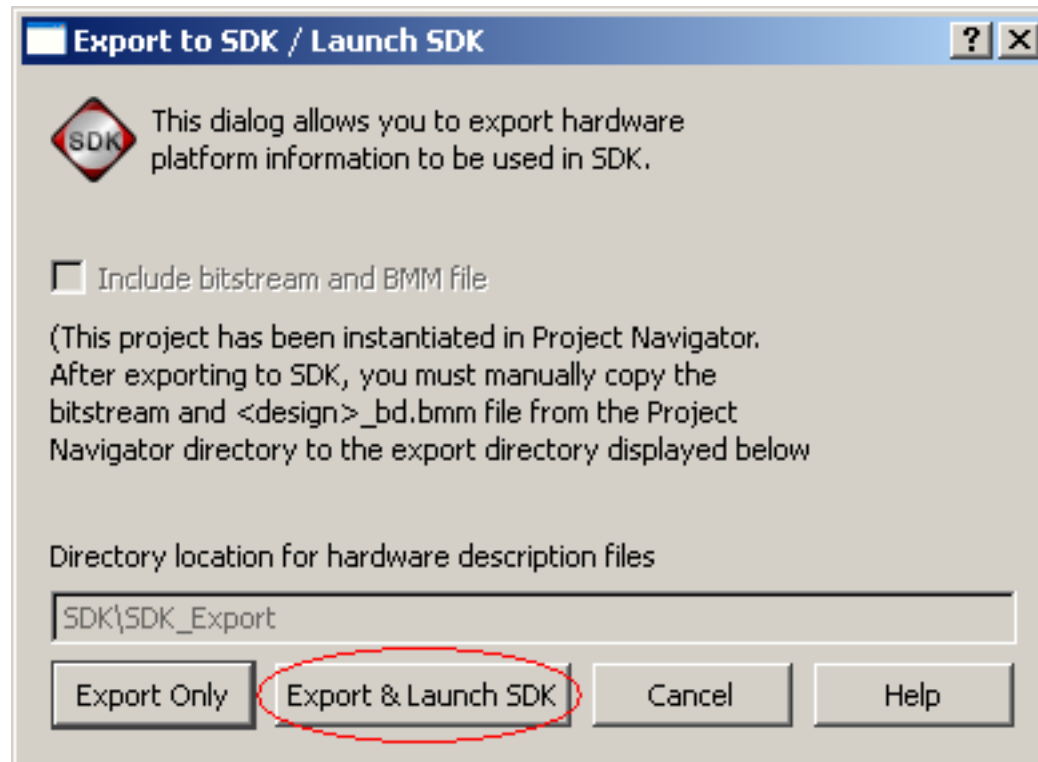
step on processor.xmp, choose Generate Programming File and click Rerun All



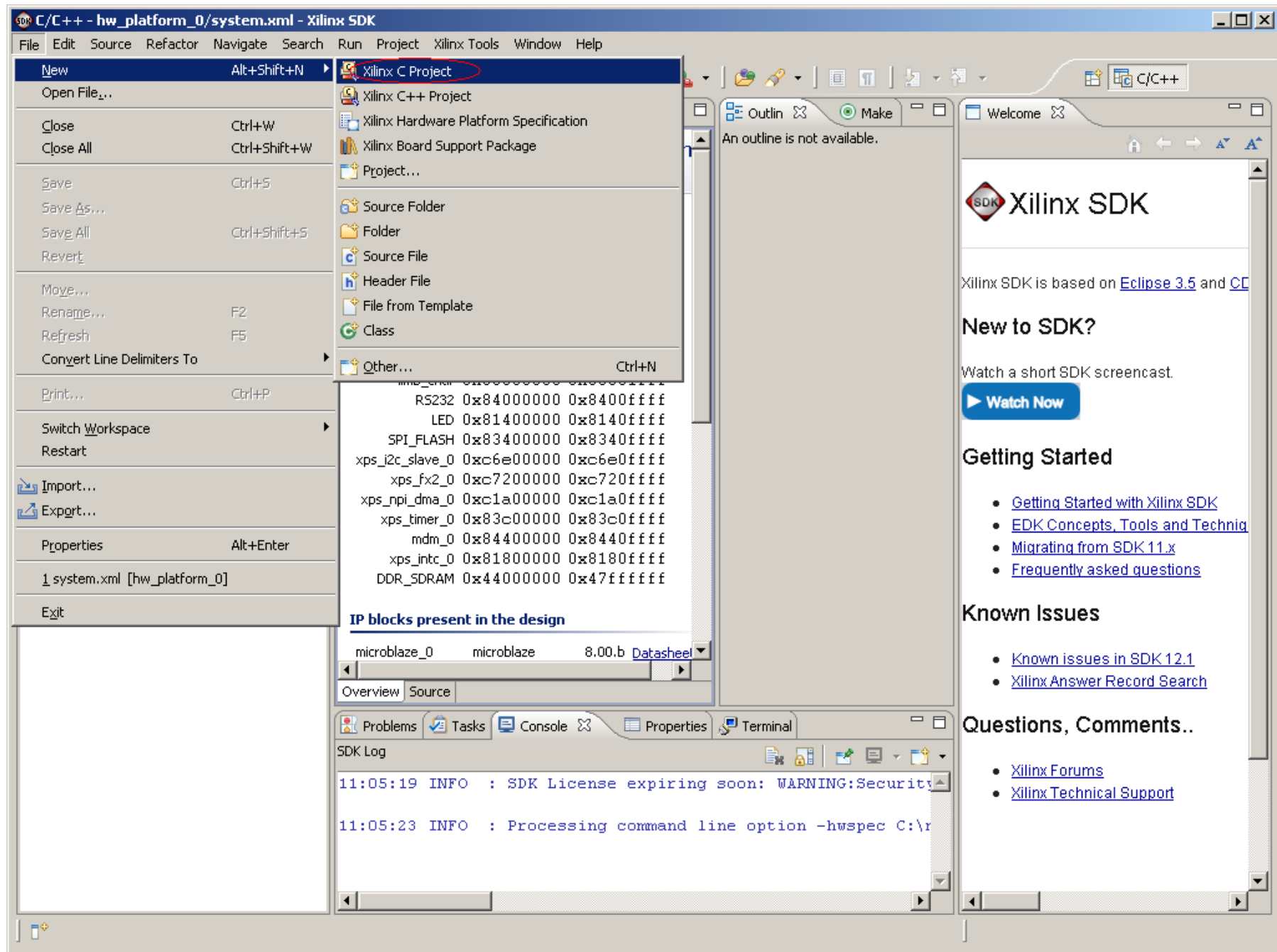
confirm generation success and return to Xilinx
Platform Studio



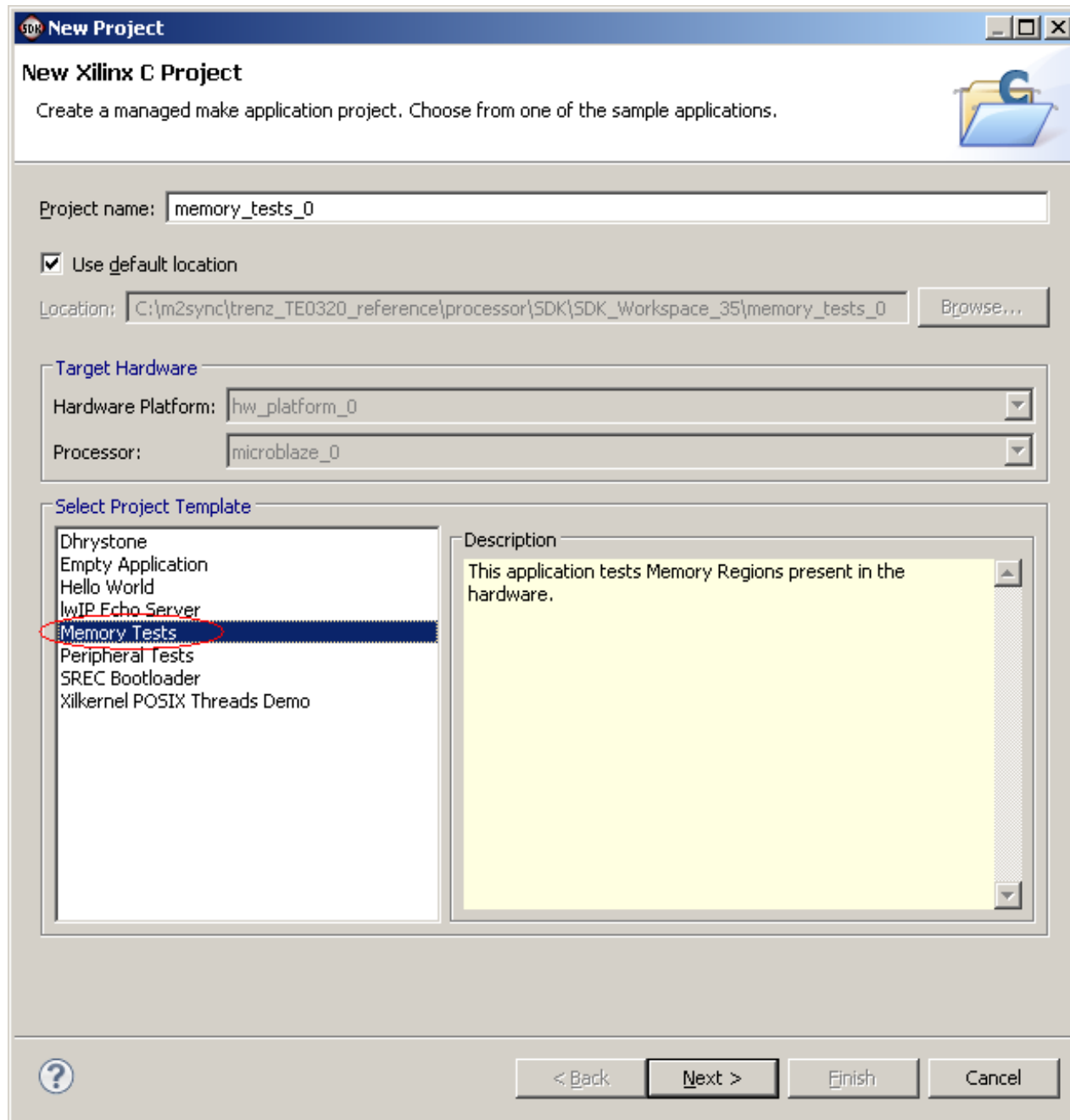
choose from menu Export Hardware Design to SDK



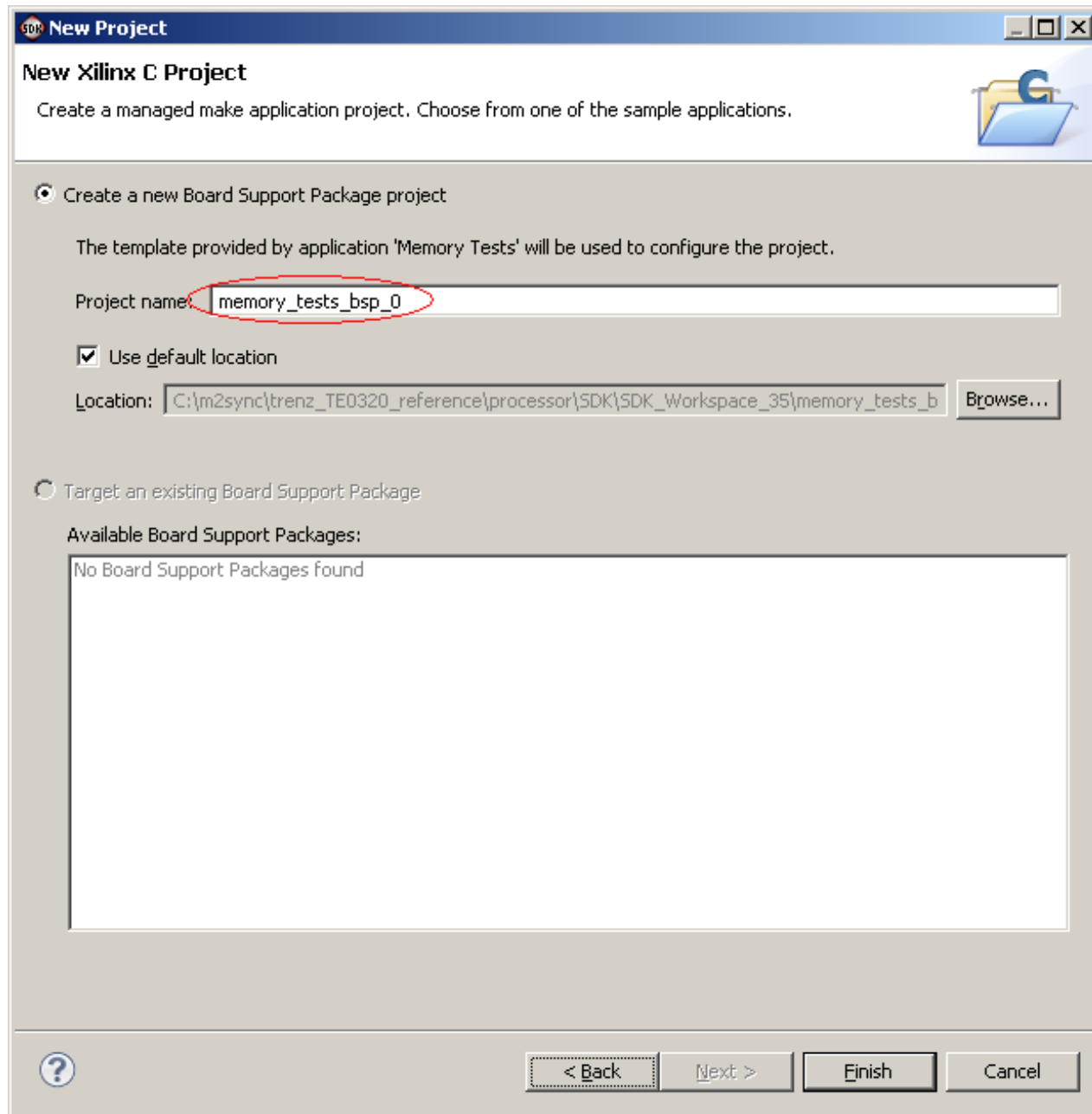
because Xilinx SDK isn't running yet, choose Export & Launch SDK button



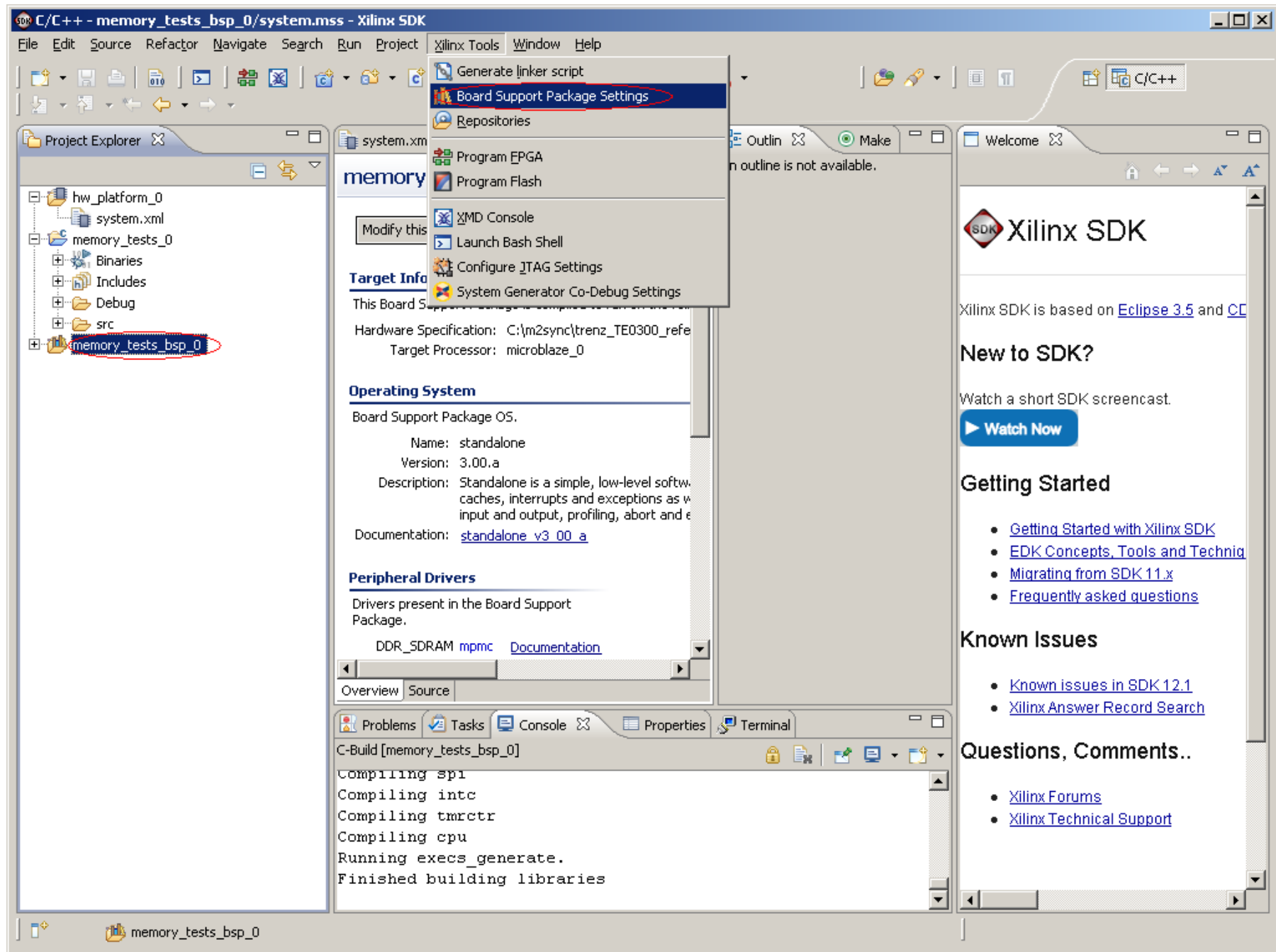
from SDK menu choose to create New Xilinx C Project



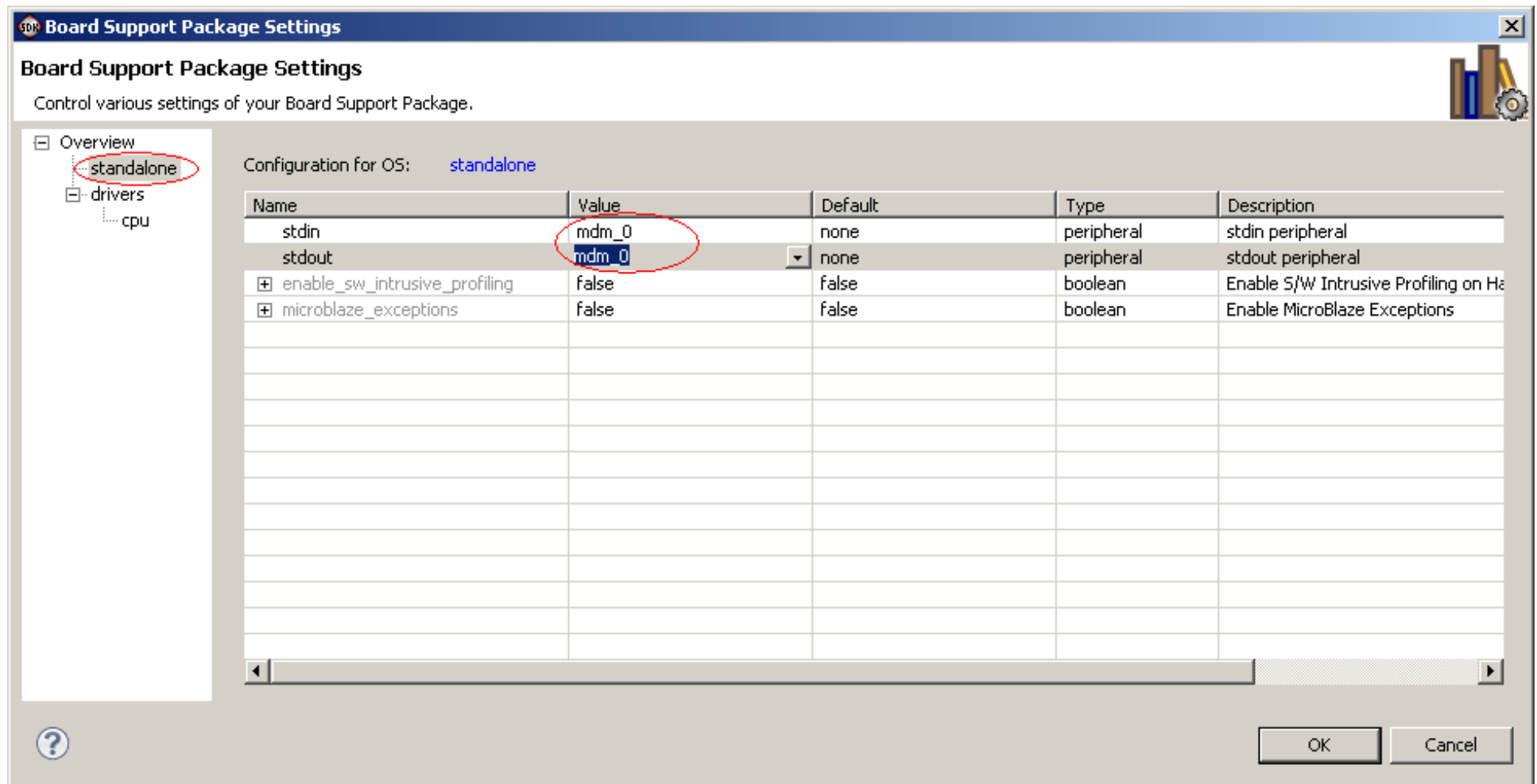
choose Memory Tests template and click Next



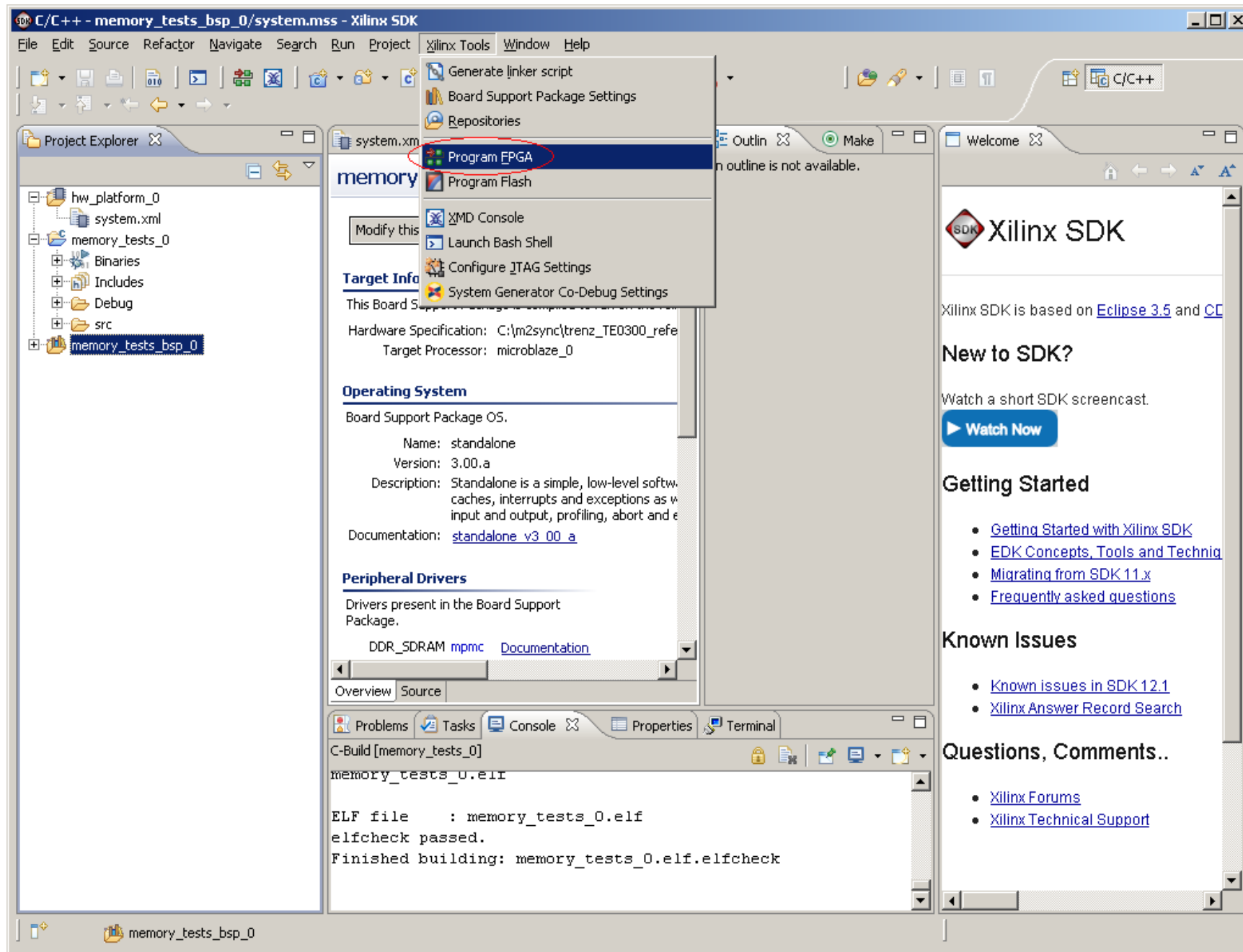
keep default BSP project name
memory_tests_bsp_0 and click Finish



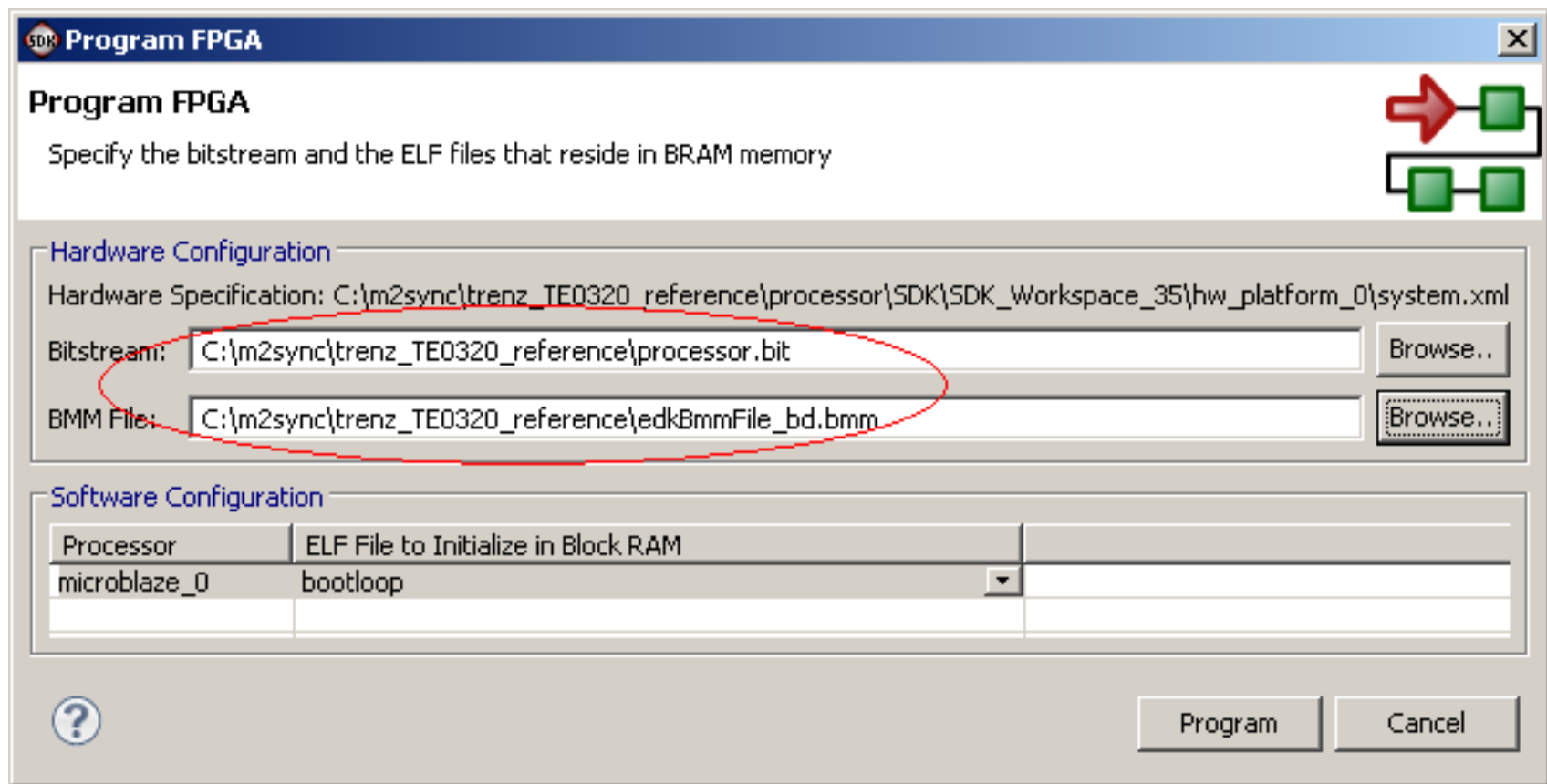
step on memory_tests_bsp_0 and choose Board Support Package Settings menu



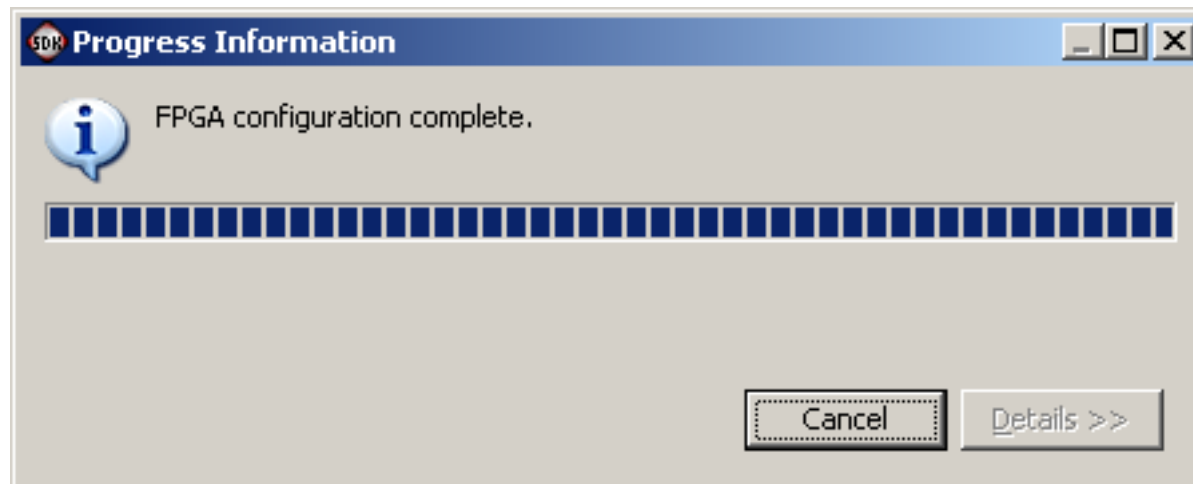
from standalone section apply mdm_0 to stdin and stdout then click OK



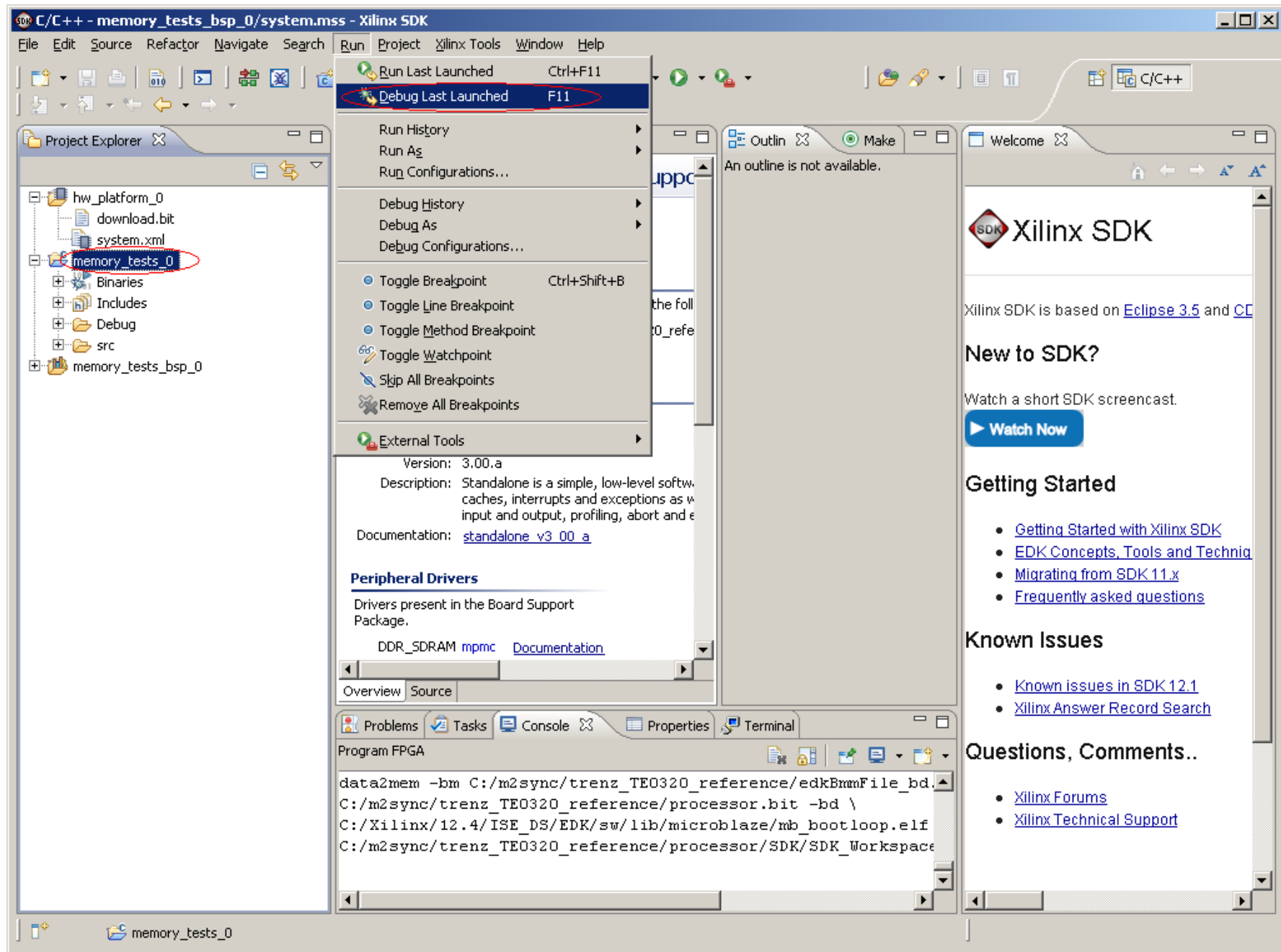
connect the prototype board TE0300 and choose
Program FPGA from menu



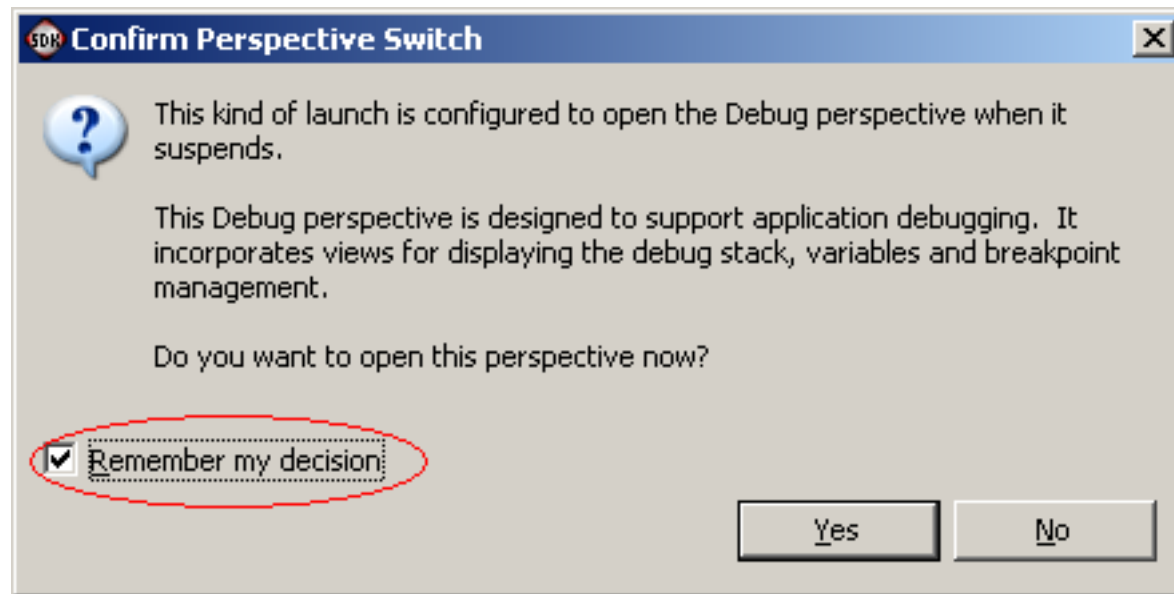
provide correct Bistream and BMM files then click
Program



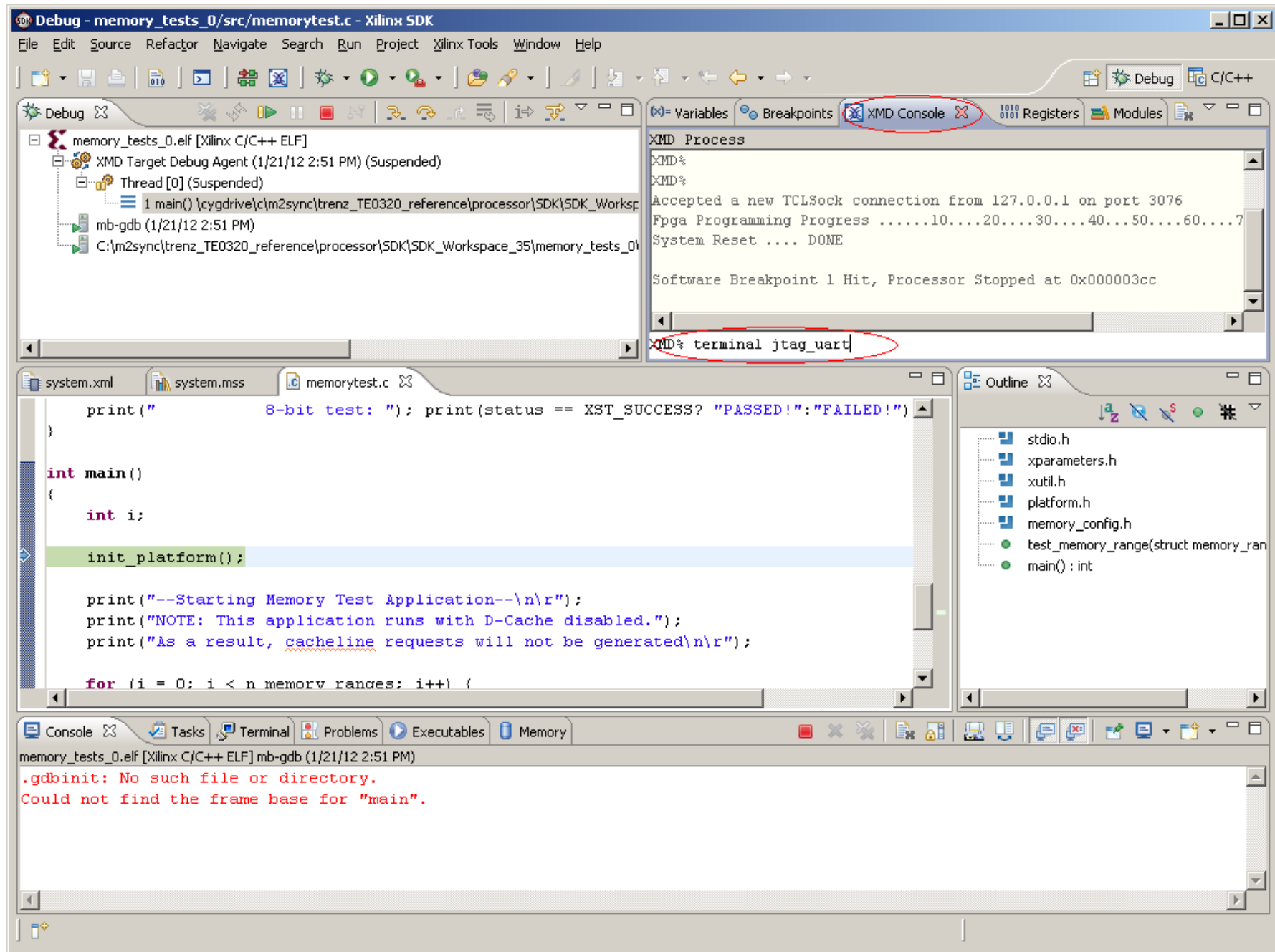
wait for FPGA programming completion



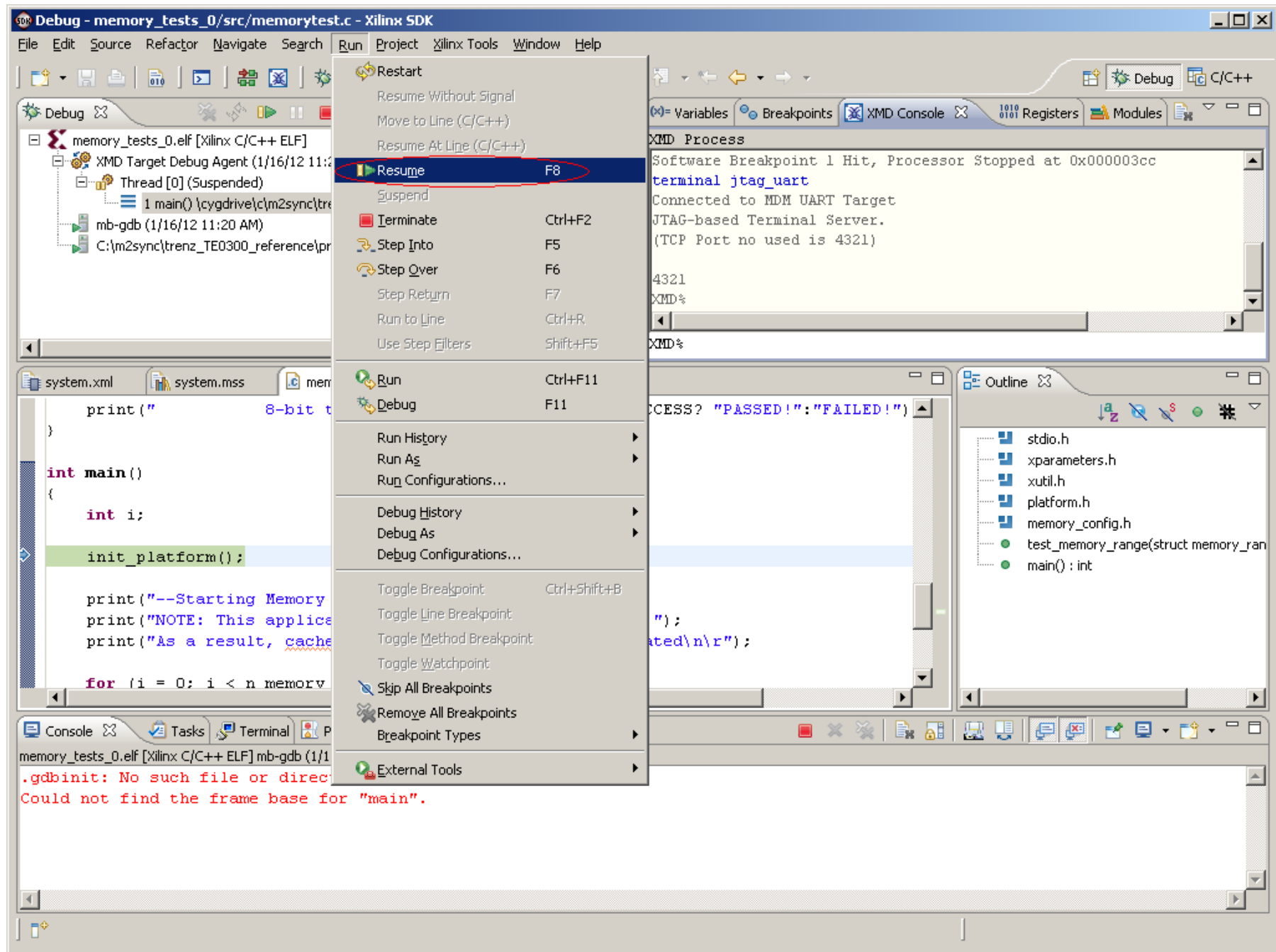
step on memory_tests_0 application and choose
Debug menu



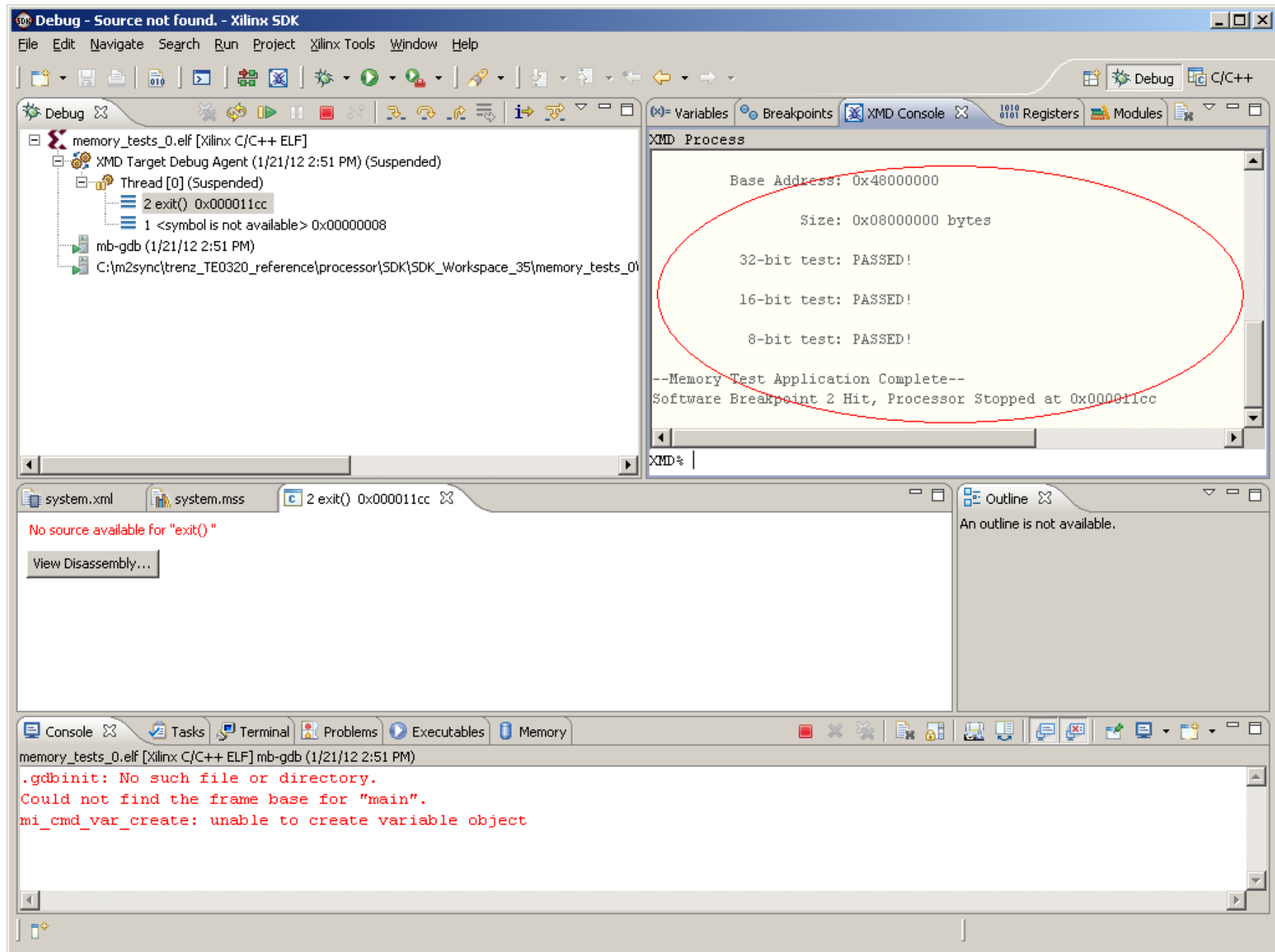
choose remember decision and confirm switching to Debug design by clicking Yes button



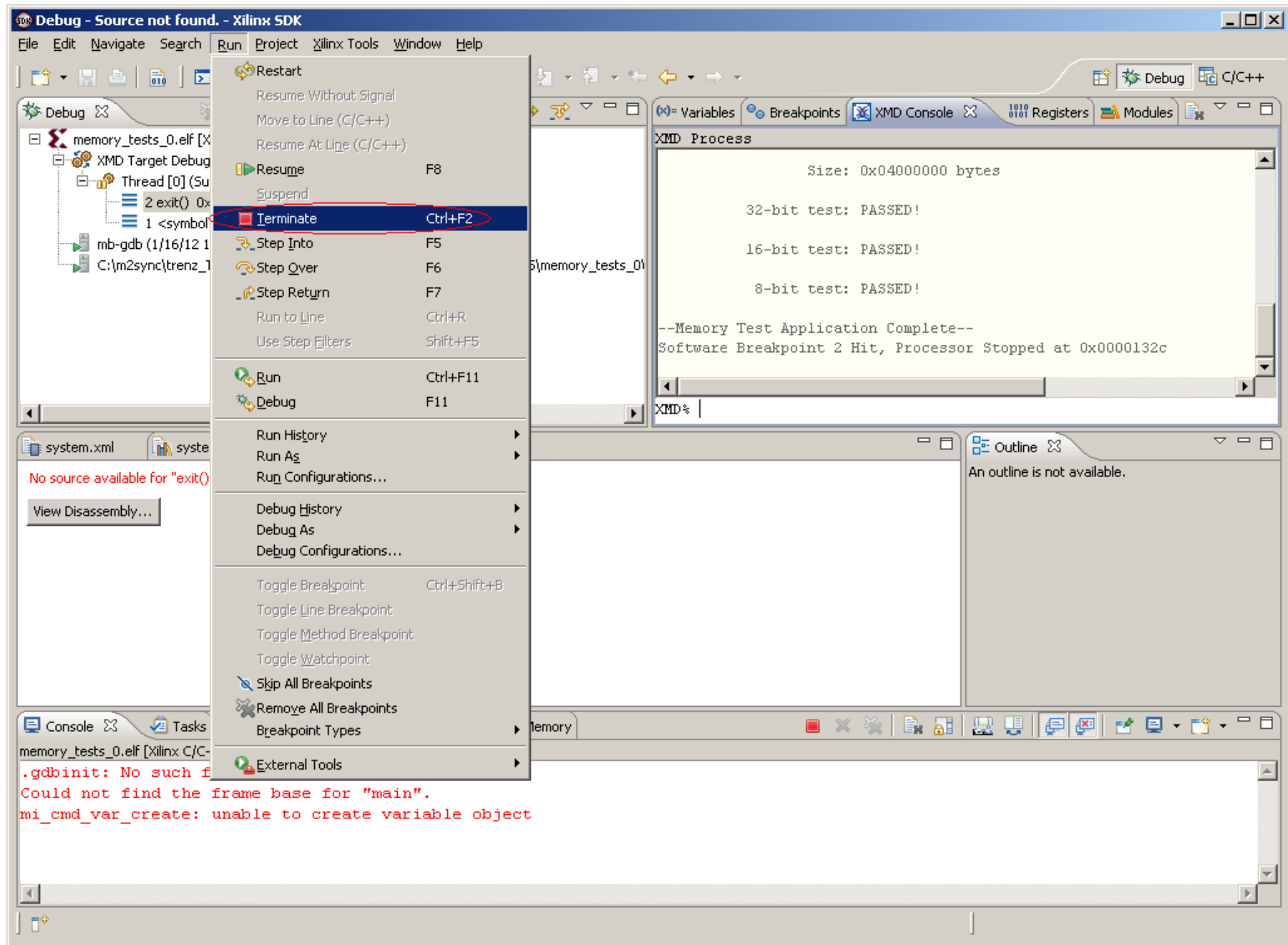
switch to XMD Console tab and type command
"terminal jtag_uart"



resume test application execution from Resume menu



observe memory test execution and report messages



terminate successfully executed application

TE0320 board configuration complete

external memory configuration
confirmed with test application