XPS_FX2_v1_20_a

User Manual v1.3

Introduction

XPS_FX2 is a communication core to interface Xilinx Microblaze soft processor and a popular USB High Speed microcontroller Cypress CY7C68013A (also known as EzUSB FX2). The XPS_FX2 supports 8bit Slave FIFO mode of operation on FX2 side. The FX2 has 4 endpoints with 2kB buffers (EP2, 4, 6, 8). The EP2-6 are FPGA outputs and EP8 is FPGA input. This asymmetry is a consequence of the core being developed for data streaming to the PC (DAQ boards, cameras...). The XPS_FX2 core side is driven by 48MHz IFCLK which is provided by FX2. The other side is driven by PLB clock and two separate clock signals for the data FIFOs. The FIFOs can be accessed with PLB bus and/or through direct high speed FIFO ports. The PLB bus FIFO access is ONLY POSSIBLE IF THE PLB CLOCK MATCHES FIFO CLOCKS.
The FX2 firmware was designed to support 4 high speed slave FIFOs: 3x TX (to PC), 1x RX (from PC). The maximal supported bandwidth is 36 MB/s for TX and 24 MB/s for RX, but significantly depends on PC, since only Bulk (secure) transfer is supported.

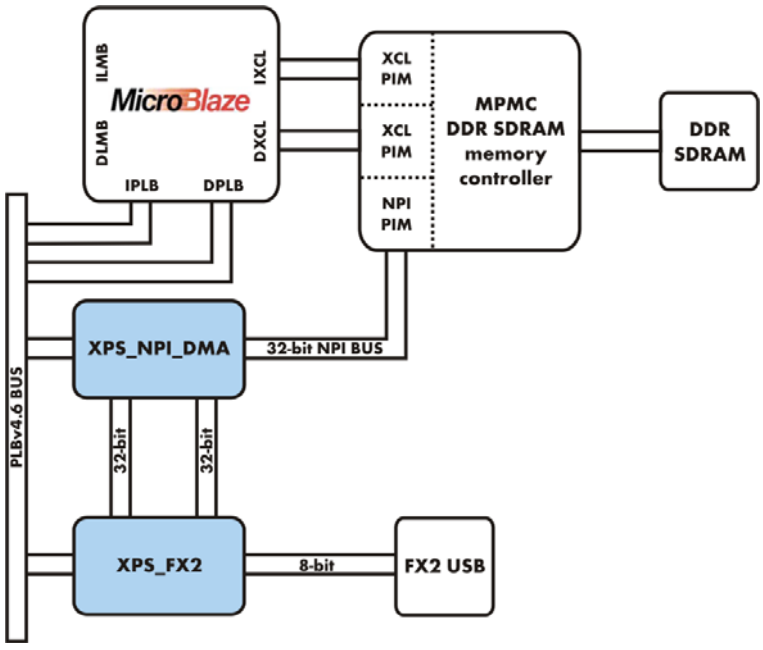

Figure 1: System integration block scheme.

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The XPS_FX2 has 4 interfaces:

- USB FX2 8-bit wide slave FIFO interface synchronous to IFCLK offfering 48MB/s peak bandwidth.
- Xilinx PLBv4.6 created with IPIF wizard for access to 9 32-bit registers. These registers control the whole peripheral.
- Proprietary synchronous 32-bits wide FIFO_OUT bus used for data streaming directly from receive FIFO. The port is synchronous to RX_FIFO_Clk.
- Proprietary synchronous 32-bits wide FIFO_IN bus used for data streaming directly to transmit FIFO. The port is synchronous to TX_FIFO_Clk.

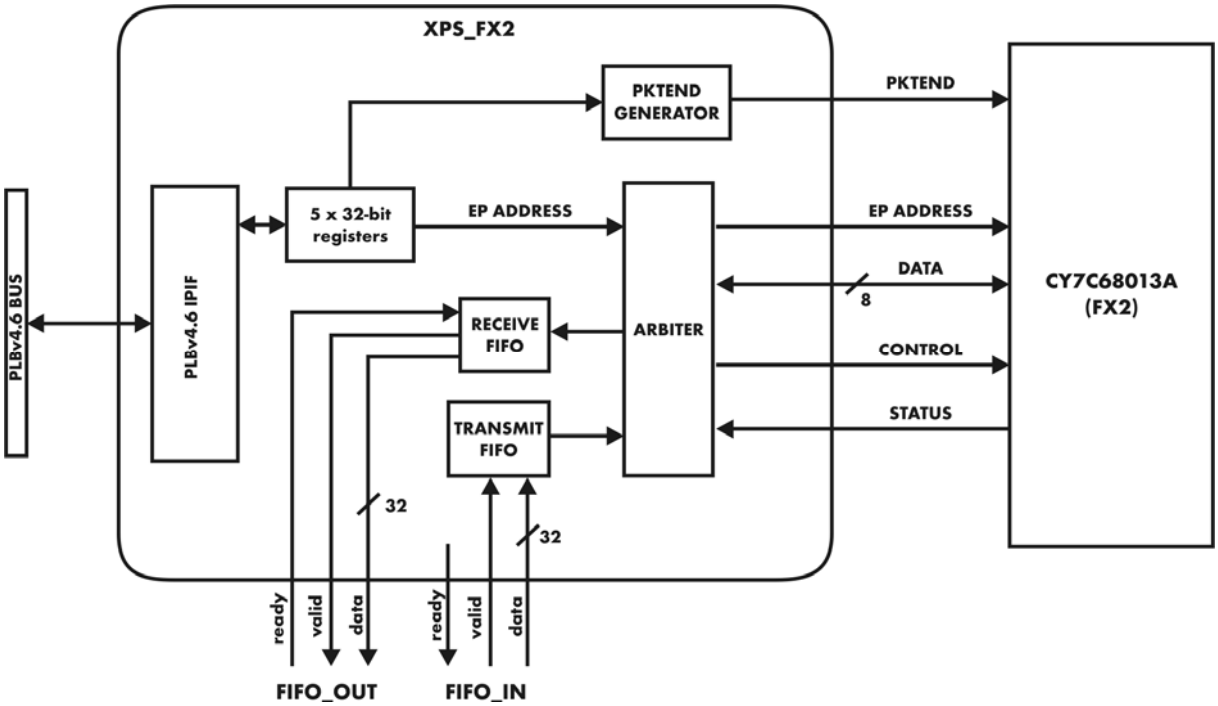

Figure 2: Peripheral internal structure block scheme.

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XPS_FX2 Core Design Parameters

Table 1: XPS_FX2 Core Design Parameters

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters				
Target FPGA family	C_FAMILY	spartan3, spartan3e, spartan3a, spartan3adsp, spartan3an, virtex2p, virtex4, qvirtex4, qrvirtex4, virtex5	virtex5	string
PLB Parameters				
PLB base address	C_BASEADDR	Valid Address	None	std_logic_vector
PLB high address	C_HIGHADDR	Valid Address	None	std_logic_vector
PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer
PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
Shared bus topology	C_SPLB_P2P	0 = Shared bus topology	0	integer
PLB master ID bus Width	C_SPLB_MID_WIDTH	log2(C_SPLB_NUM_MASTERS) with a minimum value of 1	1	integer
Number of PLB masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
Width of the slave data bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
Burst support	C_SPLB_SUPPORT_BURSTS	0 = No burst support	0	integer
XPS_FX2 Parameters				
Size of Transmit FIFO	C_TX_FIFO_KBYTE	2, 4, 8,16,32	2	integer
Size of Receive FIFO	C_RX_FIFO_KBYTE	0, 2	2	integer
Using Address FIFO*	C_USE_ADDR_FIFO	0 (not working)	0	integer
Shift transmit FIFO clock by 180 degrees**	C_TX_FIFO_CLK_180	0, 1	0	integer
Use TX_FIFO almost full signal ***	C_TX_RDY_ALMOST_FULL	0, 1	0	integer

NOTES:
* Address FIFO was designed to avoid FIFO draining before the EP ADDRESS changing. Will be fixed in further releases.
**Set to 1 only if you experience 8-bit data shifting after a received packet of data. Normally set to 0.
***This switch is used to couple TX_FIFO_RDY signal to TX_FIFO almost full signal instead to full signal. This enables 1 cycle latency

XPS_FX2 Core I/O Signals

Table 2: XPS_FX2 I/O Signal Descriptions

Name	Interface	I/O	Initial State	Description
ChipScope[0:31]	-	O	-	Debug port
USB_IFCLK	-	I	-	USB 48MHz clock
USB_SLRD	-	O	0	USB Data Read strobe
USB_SLWR	-	O	0	USB Data Write strobe
USB_FLAGA	-	I	-	USB programmable status flag (not used)
USB_FLAGB	-	I	-	USB TX FIFO full flag
USB_FLAGC	-	I	-	USB TX FIFO empty flag
USB_FLAGD	-	I	-	USB RX FIFO empty flag
USB_SLOE	-	O	0	Toggles FX2 IO buffer (1=read from USB)
USB_PKTEND	-	O	0	Commences current packet (if smaller than 512b)
USB_FIFOADR[1:0]	-	O	0	Selects USB endpoint "00"=EP2,"01"=EP4,"10"=EP6,11"=EP8
USB_FD[7:0]	-	I/O	0	USB tristate data Bus
TX_FIFO_Clk	-	I	-	TX FIFO clock
RX_FIFO_Clk	-	I	-	RX FIFO clock
TX_FIFO_DIN[0:31]	FIFO_IN	I	-	TX FIFO input data
TX_FIFO_VLD	FIFO_IN	I	-	TX FIFO data valid strobe
TX_FIFO_RDY	FIFO_IN	O	0	TX FIFO is ready flag
RX_FIFO_DOUT[0:31]	FIFO_OUT	O	zeros	RX FIFO output data
RX_FIFO_VLD	FIFO_OUT	O	0	RX FIFO data valid strobe
RX_FIFO_RDY	FIFO_OUT	I	-	RX FIFO is ready flag
IP2INTC_Irpt	-	O	0	Processor interrupt
OTHERS ARE PLBv4.6 SIGNALS	PLBv4.6			

Writing and reading to/from FIFO_IN and FIFO_OUT ports

The point to point unidirectional buses use simple handshaking protocol. When (slave) "ready" signal is high the port is open for writing. A write is performed when "valid" signal goes high. The "data" should be valid when valid signal is high. If "valid" signal goes high and the ready is low then the data are discarded. The signals are updated on rising edge of clock. The "valid" signal can be also continuous – burst transfer. FIFO_IN port is ready when it is not under reset or being full. If FIFO_OUT port is not ready then it will not send data ("valid" stays low and data stays in FIFO). FIFO_OUT port latency to act upon "ready" goes low is 1 cycle while the FIFO_IN port can have 0 or 1 latency. The latency from ready goes high to valid high can be as low as 0 cycles.

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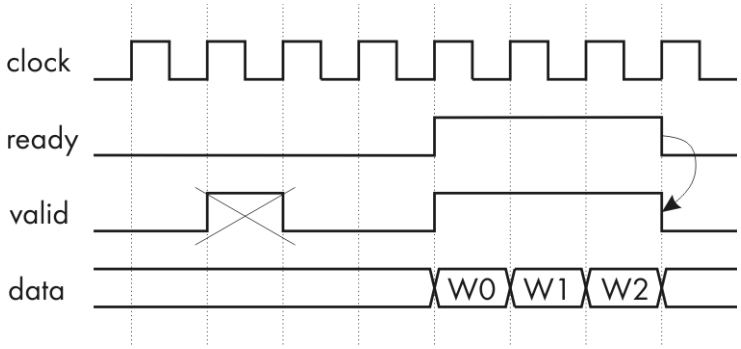


Figure 3: FIFO high speed communication ports principle of operation with latency = 0 (C_TX_RDY_ALMOST_FULL = 0).

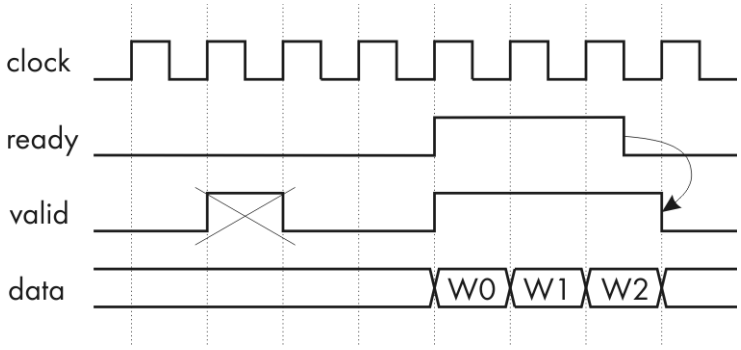


Figure 4: FIFO high speed communication ports principle of operation with latency = 1 (C_TX_RDY_ALMOST_FULL = 1).

XPS_FX2 Core Registers

XPS_FX2 has a full access of a microprocessor to the core functionality through a 5 user 32-bit and 7 IPIF Interrupt registers attached to PLBv4.6 bus.

Table 3: XPS_FX2 Core Registers

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
XPS FX2 IP Core Grouping				
C_BASEADDR + 00	CR	R/W	0x00000000	Control Register
C_BASEADDR + 04	FTR	R/W	0x00000000	FIFOs Threshold Register
C_BASEADDR + 08	SR	Read	0x00000000	Status Register
C_BASEADDR + 0C	FWR	R/W	0x00000000	FIFO Write Register
C_BASEADDR + 10	FRR	Read	0x00000000	FIFO Read Register

IPIF Interrupt Controller Core Grouping				
C_BASEADDR + 200	INTR_DISR	Read	0x00000000	interrupt status register
C_BASEADDR + 204	INTR_DIPR	Read	0x00000000	interrupt pending register
C_BASEADDR + 208	INTR_DIER	Write	0x00000000	interrupt enable register
C_BASEADDR + 218	INTR_DIIR	Write	0x00000000	interrupt id (priority encoder) register
C_BASEADDR + 21C	INTR_DGIER	Write	0x00000000	global interrupt enable register
C_BASEADDR + 220	INTR_IPISR	Read	0x00000000	ip (user logic) interrupt status register
C_BASEADDR + 228	INTR_IPIER	Write	0x00000000	ip (user logic) interrupt enable register

Note: The First (LSB) interrupt from user_logic is masked on the left!!

Details of XPS_FX2 Core Registers

The parts of the registers (or the whole registers) with a non-capital designation (e.g. wr_fifo_rst) are usually the names of the HDL signals connected to the described register.

Control Register (CR)

The Control Register is used to control basic peripheral functions. All the bit flags are assembled here.

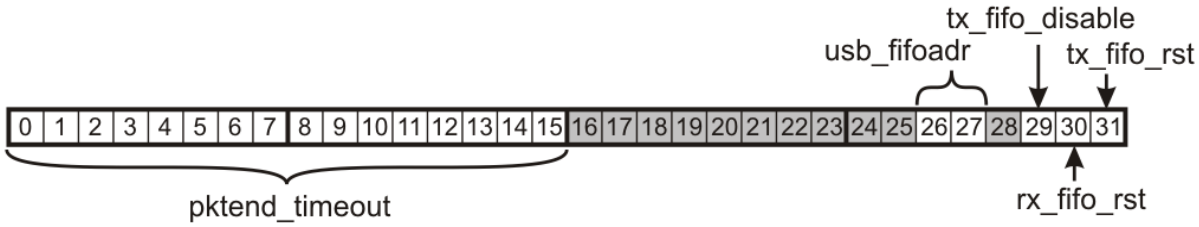


Table 4: Control Register bits

Bits	Name	Description	Reset Value
31	tx_fifo_rst	Transmit FIFO reset	0
30	rx_fifo_rst	Receive FIFO reset	0
30	tx_fifo_disable	When '1' TX_FIFO_RDY='0'	0
26-27	usb_fifoadr	USB endpoint selection*	0x0
0-15	pktend_timeout	Packet end timeout**	0x0

Notes:

*Valid Endpoints:

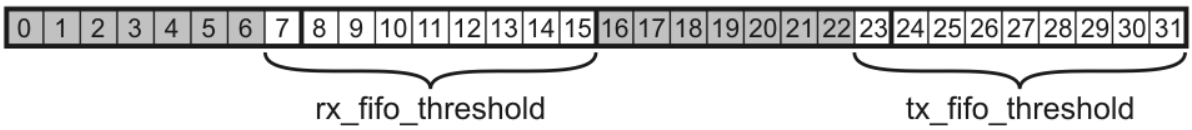
- 0 = EP2
- 1 = EP4
- 2 = EP6

Endpoint EP8 is for READING ONLY and is switched automatically when data arrives. To achieve maximal throughput use only one endpoint and prevent TX FIFO draining (TX FIFO empty should not occur).

**Packet end timeout timer automatically asserts USB_PKTEND signal when TX_FIFO is EMPTY for a programmed number of cycles AND CURRENT USB ENDPOINT FIFO IS NOT EMPTY. Cycle timer is also reset when switched to EP8 – incoming data. The USB_PKTEND commences current packet and enables the PC to receive packet smaller than 512 bytes. If you setup timer properly then the packets are automatically commenced when there is no more data is available in the TX_FIFO.

FIFOs Threshold Register (FTR)

This register is used to setup thresholds for interrupt triggering when FIFO occupancy reaches set number of words. For RX FIFO the prog_full flag goes high when number of words in a FIFO is higher than threshold. For TX FIFO the prog_empty flag goes high when number of words in a FIFO is lower than threshold.
The tx_fifo_threshold can have 9, 10 or 11 bits according to size of the TX_FIFO. This register is usually accessed using 16-bit writes.



Status Register (SR)

In the status register the peripheral reports of the current status. The tx_fifo_count can have 9-13 bits according to size of the TX_FIFO. This register is usually accessed using 16-bit reads.

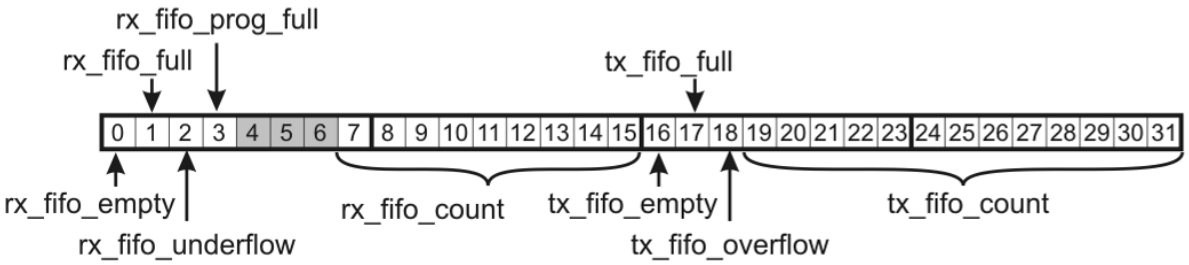


Table 5: Status Register bits

Bits	Name	Description	Reset Value
19-31	tx_fifo_count	Transmit FIFO occupancy in words	0
18	tx_fifo_overflow	Transmit FIFO overflow flag	0
17	tx_fifo_full	Transmit FIFO full flag	0
16	tx_fifo_empty	Transmit FIFO empty flag	1
7-15	rx_fifo_count	Receive FIFO occupancy in words	0
3	rx_fifo_prog_full	Receive FIFO programmable full flag	0
2	rx_fifo_underflow	Receive FIFO underflow flag	0
1	rx_fifo_full	Receive FIFO full flag	0
0	rx_fifo_empty	Receive FIFO empty flag	1

FIFO Write Register (FWR)

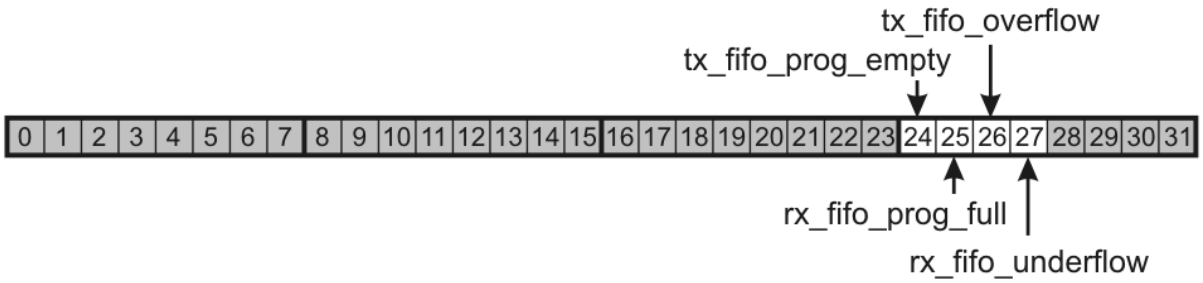
Single beat write to this register puts a single word (4 bytes) to TX FIFO. **For proper operation PLB clock frequency should be less or equal to TX_FIFO_Clk.**

FIFO Read Register (FRR)

Single beat read from this register pops one word (4 bytes) from RX FIFO. **For proper operation PLB clock frequency should be less or equal to RX_FIFO_Clk.**

Interrupt enable/pending registers

With INTR_IPIER register you can enable/disable peripheral interrupt sources. With INTR_IPISR you can identify interrupt source. Writing a value to INTR_IPISR also clears interrupt. MAKE SURE THAT YOU ONLY CLEAR TRIGGERED INTERRUPTS. Otherwise you will trigger "ghost" interrupts which were not triggered by peripheral, but the interrupt controller itself.
Writing 0x7 to INTR_DIER will enable IP interrupt sources and writing 0x80000000 to INTR_DGIER will enable global interrupt.
The image below presents a conection of user logic interrupt to INTR_IPIER and INTR_IPISR.



Programming model

By setting control register (CR) make sure that you NOT OVERRIDE the PREVIOUSLY SET BITS.

Resetting the TX_FIFO:

1. Write 0x00000001 to CR
2. Write 0x00000000 to CR

Resetting the RX_FIFO:

1. Write 0x00000002 to CR
2. Write 0x00000000 to CR

Setting the endpoint address to EP4:

1. Write 0x00000010 to CR

Setting up the packet end timeout to 1 ms (at 50MHz PLB bus frequency this is 50000 cycles):

1. Write 0xC3500000 to CR

To write a single word to TX FIFO write 32-bit data to FWR.

To get TX FIFO occupancy read status register (SR). Then mask the received data with 0xFFF to get a number of words in the TX FIFO.

To read a single word from RX FIFO read 32-bit data from FRR.

For using the software driver read function comments in:
#project#(or IP repository)\drivers\xps_fx2_v1_00_a\src\xps_fx2.c
Software driver version v1_00_a is used with this peripheral!

Revision history

Rev	Date	Author	Description
1.0	15.8.2009	AG	created
1.1	26.10.2009	AG	updated info for FWR, FRR and tx_fifo_disable
1.2	30.06.2010	AG	Updated for Xilinx tools v11, Extended TX_FIFO up to 32kB
1.3	30.01.2011	AG	Added C_TX_RDY_ALMOST_FULL parameter and new figures 3&4

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