

Overview

Virtual COM port interface provide simple and convenient way to communicate with user FPGA project and manage on-board Flash and EEPROM memories. This application note can be used with Trenz Electronic modules with Cypress FX2 microcontroller and FPGA (TE0300, TE0320 and TE0630). Microcontroller firmware can operate in several modes:

- Transit data to and from FPGA
- Command Line Interface
- EEPROM write
- SPI Flash write

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1 System Diagram

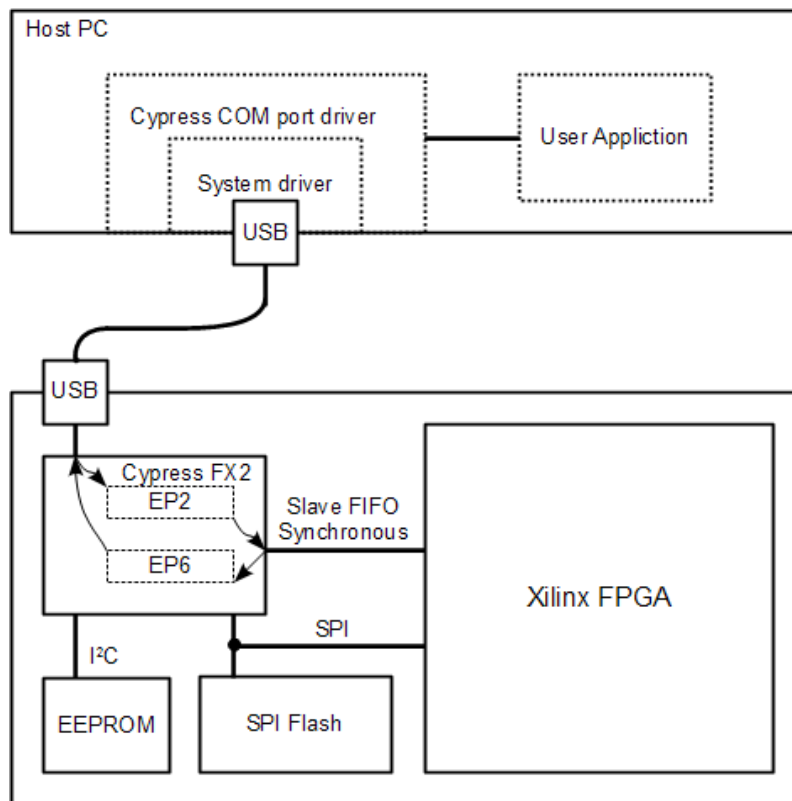


Figure 1: System Diagram

2 System components

2.1 Host PC

Cypress FX2 microcontroller firmware implement standard USB CDC interface which can be easily managed by most modern OS. OS define this interface as serial (COM) port. Microsoft Windows OS require Cypress COM port driver, which can be easily archived and installed. For example [Cypress AN58764](#) contain Virtual COM port driver “inf” file.

Usual COM port have several options (baudrate, parity, stop bits, and others) related to RS protocol and generic serial port controllers management. Virtual COM port don't need this options for work, so it can be used for other purposes.

2.2 Cypress FX2 microcontroller

FX2 microcontroller implement USB CDC class interface, which include 3 endpoints (control endpoint and 2 data endpoints). By default data endpoints configured in “AutoIn” and “AutoOut” modes to transfer data to and from FPGA interface. User can switch microcontroller firmware to CLI, EEPROM or Flash management mode, in this case out endpoints will be reconfigured to manual mode and data from host processed by microcontroller firmware.

2.3 FPGA project

FPGA project communicate with FX2 microcontroller using 8-bit synchronous Slave FIFO interface. All signals configured to active high level. When Host PC send data to COM port it comes to FX2 EP2 FIFO. FPGA project can read data from EP2, process it and write to EP6 FIFO. EP2 and EP6 FIFOs size is 512 bytes, quad buffered.

FPGA project should check FIFOs flags.

Signal	FX2 Flag	Description
FlagA	EP2EF	Receive FIFO empty flag. '1' When EP2 FIFO empty.
FlagB	EP6FF	Transmit FIFO full. '1' When EP6 FIFO full.
FlagC	EP6PF	Transmit FIFO almost full. '1' when less than 128 bytes free in EP6 FIFO.
FlagD	EP2PF	Receive FIFO almost full. '1' when more than 128 bytes in EP2 FIFO.

Table 1: Flags description

3 Firmware modes

FX2 microcontroller firmware can work in several modes. To switch between modes used combination of COM port baudrate and parity parameters.

Mode	Enter	Description	Exit
COM	Power cycle or exit from CLI mode	Default mode. Provide Virtual COM port interface to FPGA.	Change Baudrate/Parity (CLI / EEPROM Write / Flash Write)
CLI	Baudrate = 123456	Command Line Interface. Provide set of module management commands.	Power cycle (COM). Change Baudrate/Parity (EEPROM Write / Flash Write). 'quit' command (COM)
EEPROM Write	Baudrate = 222222 Parity = Odd	Received data written by I2C interface to EEPROM.	Power cycle (COM). Change Baudrate/Parity works, but not recommended.
Flash Write	Baudrate = 333333 Parity = Even	Received data written to SPI Flash.	Power cycle (COM). Change Baudrate/Parity works, but not recommended.

Table 2: Firmware modes

3.1 Command Line Interface mode

CLI mode provide wide set of commands to manipulate module.

To enter CLI mode, switch COM port “Baudrate” to “123456”.

In this mode firmware read user input and process commands. Commands is case sensitive and should be lower-case. “Backspace” can be used for command line correction. “Enter” with empty command line cause re-execution of previous command.

Command	Description
ver	Print firmware version
power off	Disable FPGA power supply
power on	Enable FPGA power supply
flash status	Print SPI Flash Status registers
flash id	Print SPI Flash IDCODE
flash erase	SPI Flash "Bulk erase"
flash unlock	Clear SPI Flash "Status register"
flash read	Read data from SPI Flash
fpga status	Print status of FPGA pins
fpga reset	Reset FPGA
quit	Quit from CLI mode to COM mode

Table 3: CLI mode command set

3.1.1 "ver" command

The "ver" command print firmware version and build date.

Example:

```
> ver
1.01 beta
Build Oct 12 2012 13:02:34
```

3.1.2 "power off" command

The "power off" command disable FPGA power supply.

Example:

```
> power off
OK
```

3.1.3 "power on" command

The "power on" command enable FPGA power supply

Example:

```
> power on
OK
```

3.1.4 "flash status" command

The "flash status" command read and print SPI Flash "Status register 1" and "Status register 2" values. Please refer your Flash datasheet to registers bit layout.

Note: To get full control on SPI bus firmware disable FPGA power supply before this operation. After each flash command, use "power on" command and "fpga reset" command to run FPGA.

Example:

```
> flash status
SR1 00 SR2 00
```

3.1.5 “flash id” command

The “flash id” command read and print first 3 bytes from result of SPI Flash “READ IDENTIFICATION” command.

Byte	Description
1	Manufacturer ID
2	Memory Type
3	Memory Capacity

Table 4: “READ IDENTIFICATION” result layout

For Trenz Electronic modules possible values is.

Flash	Manufacturer ID	Memory Type	Capacity
M25P32	20h - Micron	20h	16h
W25Q64FV	EFh - Winbond	40h	17h

Table 5: Flash IDCODEs

Note: To get full control on SPI bus firmware disable FPGA power supply before this operation. After each flash command, use “power on” command and “fpga reset” command to run FPGA.

Example:

```
> flash id
IDCODE EF4017
W25Q64FV
```

3.1.6 “flash erase” command

The “flash erase” command execute SPI Flash “Bulk Erase” command. Processing of this command usually require some time. User should wait command to complete before power off module or enter next command. Refer your Flash chip datasheet for maximum required time.

Note: To get full control on SPI bus firmware disable FPGA power supply before this operation. After each flash command, use “power on” command and “fpga reset” command to run FPGA.

Example:

```
> flash erase
Done
```

3.1.7 “flash unlock” command

The “flash unlock” command write zero value to status register. This command can be used to clear protection bits. Refer to your Flash chip datasheet for status register layout.

Note: To get full control on SPI bus firmware disable FPGA power supply before

this operation. After each flash command, use “power on” command and “fpga reset” command to run FPGA.

Example:

```
> flash unlock
Done
```

3.1.8 “flash read” command

The “flash read” command read and print data from SPI Flash. Firmware read 8 bytes of data from current flash address and increment address to 8 after execution.

Note: To get full control on SPI bus firmware disable FPGA power supply before this operation. After each flash command, use “power on” command and “fpga reset” command to run FPGA.

Example:

```
> flash read
FF FF FF FF FF FF FF FF
>
FF FF FF FF FF FF FF FF
>
AA 99 55 66 30 A1 00 07
>
20 00 31 A1 06 28 31 41
>
3D 00 31 61 89 EE 31 C2
```

3.1.9 “fpga status” command

The “fpga status” command print FPGA pins information. Information printed in 6 chars sequence {d|D}{i|I}{s|S}{p|P}{-|0}{-|1}.

Char	Value	Description
1	d	“Done” pin is 0
	D	“Done” pin is 1
2	i	“Init” pin is 0
	I	“Init” pin is 1
3	s	FPGA Power supply disabled
	S	FPGA Power supply enabled
4	p	“PROG_B” pin is 0
	P	“PROG_B” pin is 1
5	-	“Int0” pin is 0
	0	“Int1” pin is 1
6	-	“Int1” pin is 0
	1	“Int1” pin is 1

Example:

```
> fpga status
```

DISP--

3.1.10 “fpga reset” command

The “fpga reset” command execute FPGA reset sequence by driving FPGA PROG_B pin low and high after some delay. This command also disconnect FX2 microcontroller from SPI bus to allow FPGA boot from SPI Flash.

Example:

```
> fpga reset
```

Done

3.1.11 “quit” command

The “quit” command switch firmware to COM mode, which allow communication with FPGA. Use “power on” command and/or “fpga reset” command before this command if needed.

3.2 EEPROM Write mode

On-board EEPROM chip contain FX2 microcontroller firmware. To update EEPROM content, several steps required:

- To enter EEPROM Write mode, switch COM port “Parity” option to “Odd” and “Baudrate” to “222222”.
- Send firmware file to COM port in binary mode.
- Power cycle module to apply changes.

For Windows OS this sequence can be done using “bat” file.

```
mode.com COM1: PARITY=O BAUD=222222
```

```
copy /b new_firmware.iic COM1:
```

This example write “new_firmware.iic” file content to EEPROM using COM1 port. Refer your OS information for right COM port number¹.

3.3 Flash Write mode

On-board Flash chip contain FPGA bitstream. To update Flash content, several steps required:

- To enter “Flash Write” mode, switch COM port “Parity” option to “Even” and “Baudrate” to 333333.
- Send bitstream file to COM port in binary mode.
- Power cycle module to apply changes.

For Windows OS this sequence can be done using “bat” file.

¹ Windows can work incorrectly with high port numbers. Change COM port number to COM1-COM4 if you face this problem.


```
mode.com COM1: PARITY=E BAUD=333333
copy /b new_project.bin COM1:
```

This example write “new_project.bin” file content to Flash using COM1 port. Refer your OS information for right COM port number².

Firmware automatically provide sector erase before write data.

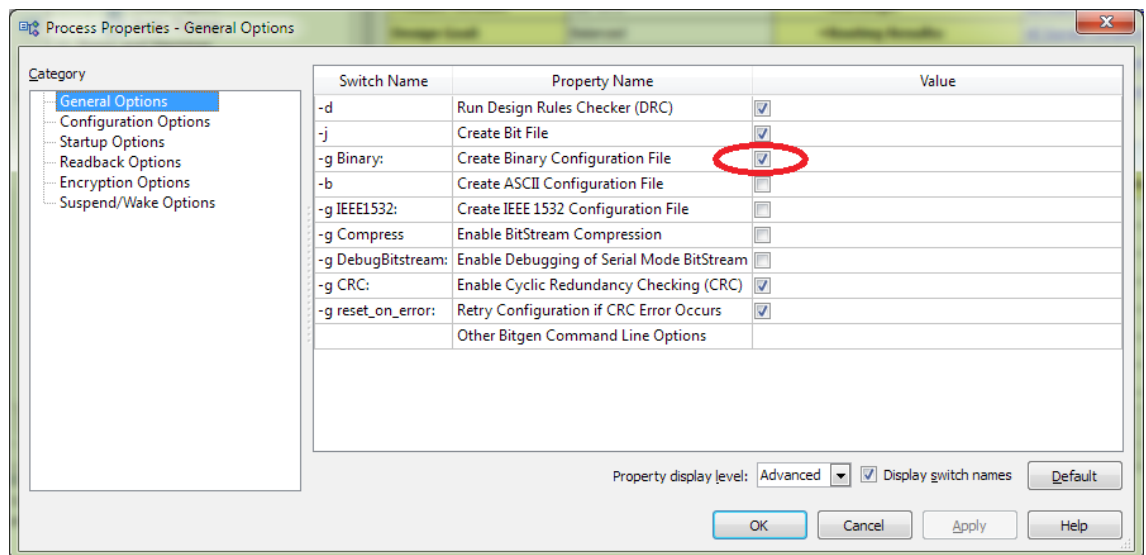


Figure 2: Bitgen option for binary file generation.

To generate bitsream file in binary format use “-g Binary:yes” bitgen option. In Xilinx ISE it can be done by checking “Generate Programming File” → “Process properties” → “Create Binary Configuration File”. In Xilinx XPS this option should be added to etc/bitgen.ut file.

4 Glossary of Abbreviations and Acronyms



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API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit

² Windows can work incorrectly with high port numbers. Change COM port number to COM1-COM4 if you face this problem.

IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.



Document Change History

ver.	date	author	description
1.00	02-10-2012	AIK	Release.
1.01	12-10-2012	AIK	New release for SDCC with CLI.