Klingler Computer 8 bit expanded Machine Operations

Opcode Hex	Addr Stack Direction Bit 15	Addr Stack enable Bit 14	JMP Bit 13	HOP Bit 12	Counter Select Bit 11	Reserved Bit 10	RAM WE Bit 9	Display WE Bit 8	ALU select Bits 7,6,5,3	Source MUX Bits 3,2,1	Register WE Bit 0	Command Hex	Function	Operation	Machine Code
0000	0	0	0	0	0	0	0	0	0000	000	0	00	NO OP	No Operation	00000 0000 0000 0000
0001	0	0	0	0	0	0	0	0	0000	000	1	01	LD Rd DD	Rd <= Data	00001 dddd DDDD DDDD
0005	0	0	0	0	0	0	0	0	0000	010	1	02	MOV Rd Ra	Rd <= Ra	00010 dddd aaaa 0000
0100	0	0	0	0	0	0	0	1	0000	000	0	03	DISP Ra	Display Ra on Display	00011 0000 aaaa 0000
1800	0	0	0	1	1	0	0	0	0000	000	0	05	HOP DD	Counter Position <= Counter Position + DD	00101 0000 DDDD DDDD
C000	1	1	0	0	0	0	0	0	0000	000	0	06	LOC	Stack <= Counter Position + 1	00110 0000 0000 0000
2800	0	0	1	0	1	0	0	0	0000	000	0	07	GOTO DD	Counter Position <= DD	00111 0000 DDDD DDDD
E800	1	1	1	0	1	0	0	0	0000	000	0	08	BRANCH DD	Stack <= Counter Position + 1 Counter Position <= DD	01000 0000 DDDD DDDD
4000	0	1	0	0	0	0	0	0	0000	000	0	09	SPOP	Stack pop[0]	01001 0000 0000 0000
2000	0	0	1	0	0	0	0	0	0000	000	0	0a	LOOP	Counter Position <= Stack	01010 0000 0000 0000
6000	0	1	1	0	0	0	0	0	0000	000	0	0b	RETURN	Counter Position <= Stack Stack pop[0]	01011 0000 0000 0000
0208	0	0	0	0	0	0	1	0	0000	100	0	0d	STORE Ra Rb	RAM[Ra] <= Rb	01101 0000 aaaa bbbb
0009	0	0	0	0	0	0	0	0	0000	100	1	0e	READ Rd Ra	Rd <= RAM[Ra]	01110 dddd aaaa 0000
0003	0	0	0	0	0	0	0	0	0000	001	1	10	NOT Rd Ra	Rd <= NOT Ra	10000 dddd aaaa 0000
0013	0	0	0	0	0	0	0	0	0001	001	1	11	AND Rd Ra Rb	Rd <= Ra AND Rb	10001 dddd aaaa bbbb
0023	0	0	0	0	0	0	0	0	0010	001	1	12	OR Rd Ra Rb	Rd <= Ra OR Rb	10010 dddd aaaa bbbb
0033	0	0	0	0	0	0	0	0	0011	001	1	13	XOR Rd Ra Rb	Rd <= Ra XOR Rb	10011 dddd aaaa bbbb
0043	0	0	0	0	0	0	0	0	0100	001	1	14	SHL Rd Ra	Rd <= Ra << 1	10100 dddd aaaa 0000
0053	0	0	0	0	0	0	0	0	0101	001	1	15	SHR Rd Ra	Rd <= Ra >> 1	10101 dddd aaaa 0000
0063	0	0	0	0	0	0	0	0	0110	001	1	16	ADD Rd Ra Rb	Rd <= Ra + Rb	10110 dddd aaaa bbbb
0073	0	0	0	0	0	0	0	0	0111	001	1	17	SUB Rd Ra Rb	Rd <= Ra - Rb	10111 dddd aaaa bbbb
0083	0	0	0	0	0	0	0	0	1000	001	1	18	MULT Rd Ra Rb	Rd <= Ra * Rb	11000 dddd aaaa bbbb
0093	0	0	0	0	0	0	0	0	1001	001	1	19	DIV Rd Ra Rb	Rd <= Ra / Rb	11001 dddd aaaa bbbb
00a3	0	0	0	0	0	0	0	0	1010	001	1	1a	EQL Rd Ra Rb	Rd <= Ra == Rb (boolean 1 or 0)	11010 dddd aaaa bbbb
00b3	0	0	0	0	0	0	0	0	1011	001	1	1b	GRTR Rd Ra Rb	Rd <= Ra > Rb (boolean 1 or 0)	11011 dddd aaaa bbbb
08c0	0	0	0	0	1	0	0	0	1100	000	0	1c	TEST Ra D	If (Ra == 1) Counter Position <= Counter Position + 1 Else Counter Position <= Counter Position + 1 + D	11100 0000 aaaa DDDD
00d3	0	0	0	0	0	0	0	0	1101	001	1	1d	ASCII0 Rd Ra	Rd <= (ASCII[0]) Ra	11101 dddd aaaa 0000
00e3	0	0	0	0	0	0	0	0	1110	001	1	1e	ASCII1 Rd Ra	Rd <= (ASCII[1]) Ra	11110 dddd aaaa 0000
00f3	0	0	0	0	0	0	0	0	1111	001	1	1f	ASCII2 Rd Ra	Rd <= (ASCII[2]) Ra	11111 dddd aaaa 0000