Nirma University

Institute of Technology

B.tech in Electronics and Communication Engineering

Semester - V

Course Code: 2EC601CC24

Course Name: VLSI Design

Special Assignment

Submitted By :- Het Patel [22BEC050]

Submitted To :- Dr. Piyush Bhatasana

Design Problem :- NMOS inverter with NMOS as a load for the optimized VOL, VIL and VIH.

Introduction :-

In this project, we are working with an NMOS inverter where both the amplifying transistor and the load are NMOS transistors. The main goal of this circuit is to amplify small, time-varying input signals. Instead of using resistors as the load, we use another NMOS transistor, which is known as an active load. This approach has several benefits, including saving space on the chip, as transistors take up less area compared to resistive loads. Additionally, using an active load improves the overall performance of the inverter compared to one with a resistive load.

Enhancement-Load NMOS Inverter :-

The enhancement load NMOS inverter uses an NMOS transistor as the load, which can operate either in the saturation or linear region depending on the gate bias voltage. In the saturated enhancement load inverter, the load operates in the saturation region, requiring only a single power supply but limiting the maximum output voltage (VOH) to VDD−VT. In the linear enhancement load inverter, the load operates in the linear region, allowing VOH to reach VDD and providing better noise margins. However, it requires two power supplies and suffers from higher power dissipation, making these inverters less suitable for large-scale digital applications.

Depletion Load NMOS Inverter :-

The depletion load NMOS inverter addresses the drawbacks of the enhancement load inverter by using a depletion-mode NMOS transistor as the load. Although it requires a few extra fabrication steps, such as a channel implant to adjust the threshold voltage of the load, it offers several advantages. These include a sharper voltage transfer characteristic (VTC) transition, improved noise margins, and the convenience of requiring only a single power supply. Additionally, the overall layout area is smaller compared to the enhancement load inverter, making the depletion load inverter more efficient in design.

Design Problem :-

For given function, assume that all the transistors have been sized to give a worst-case output resistance of 20 K for the worst-case input pattern.

[1] Find out the optimized Boolean equation (If not given).

- As the output Q will be simply inverted, the optimized Boolean equation is given by:

$$\text{Input} = A$$
$$Q = A'$$

- The truth table for this equation would be :-

Input	Output
A	Q = A’
0	1
1	0

Table 1: Truth Table For NOT Gate

[2] Draw the optimized gate level circuit diagram.

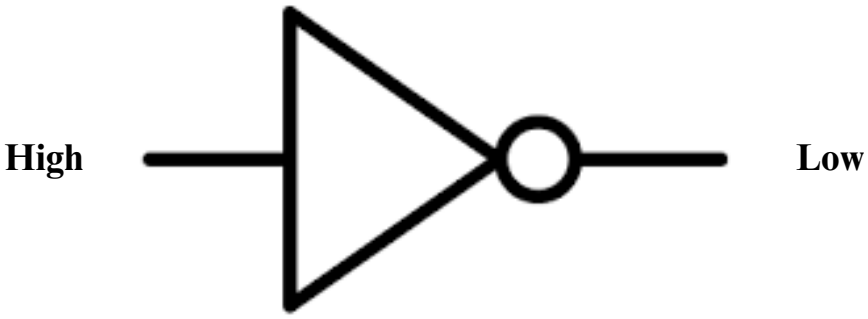


Figure 1: NOT Gate

[3] Draw the transistor level schematic for CMOS/MOS implementation.

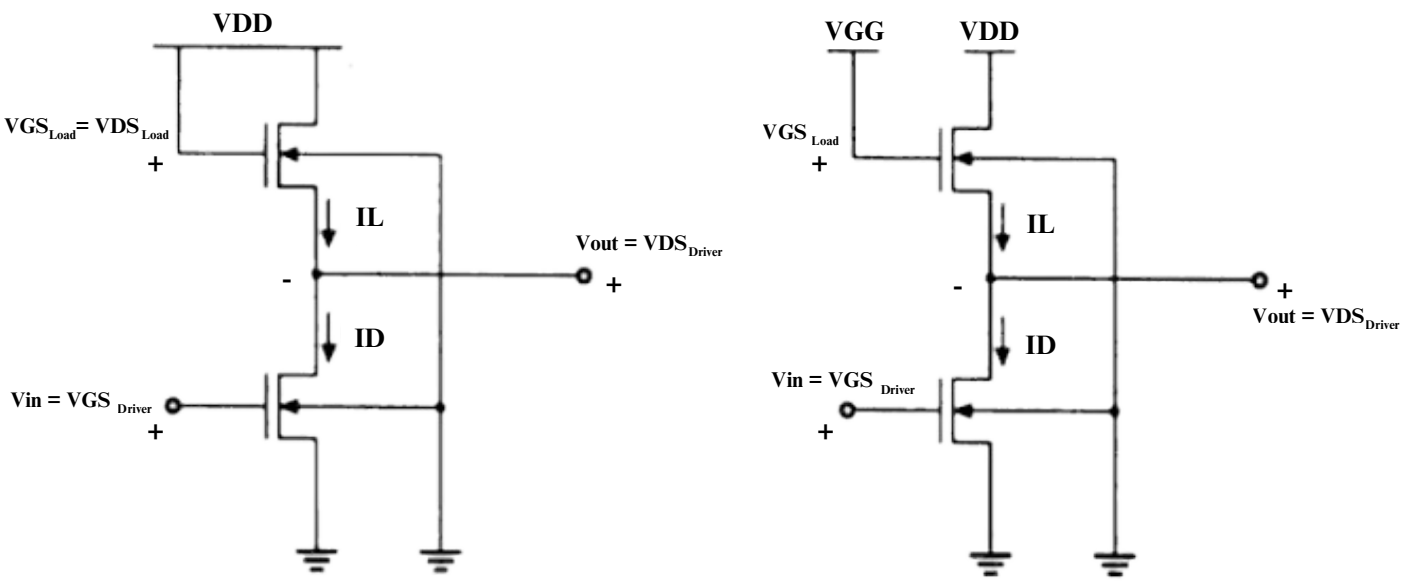


Figure 2: Transistor level schematic diagram

[4] Draw stick diagram for above implementation level using proper color code.

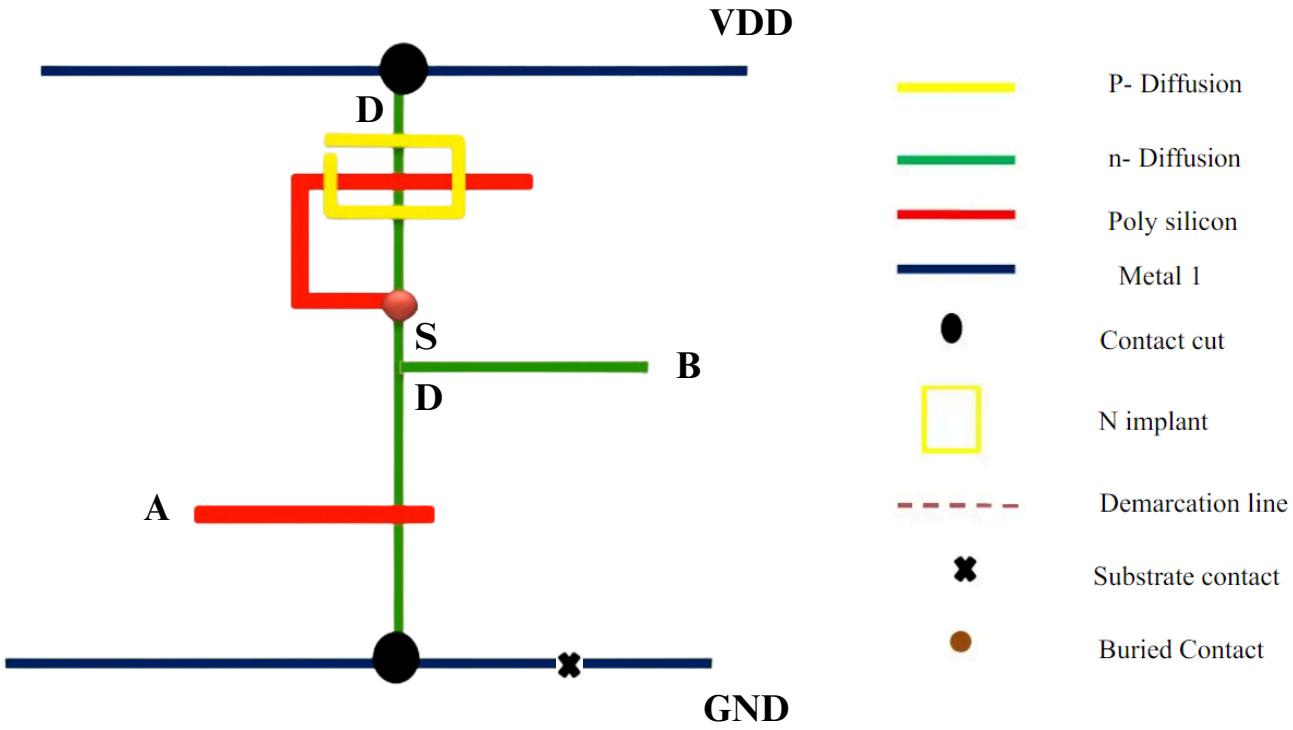


Figure 3: Stick Diagram using proper color code

[5] State the various level of VOL corresponding to various transistor statuses.

- Only one value of VOL (output low voltage) is possible in CMOS logic. When the output is low, it is pulled to a voltage close to 0V by the NMOS transistor. Since CMOS circuits are designed to produce a well-defined low voltage (close to 0V) when the output is low, there aren't varying levels of VOL for different transistor statuses.

[6] Find an equivalent CMOS inverter circuit.

- The above question is not applicable.

[7] For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

- In CMOS circuits, when the output is low (VOL), the NMOS transistor is in saturation (strongly conducting), and the PMOS transistor is off. The resistance at this point is primarily determined by the NMOS transistor, and it has a typical low resistance due to its strong conduction. However, calculating an exact value for output resistance can be complex and depends on specific transistor parameters, which may not be part of this analysis.

[8] For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

- Same as Q.7. The above question is not applicable.

[9]-[10] Prepare the layout using Microwind tool and Simulate it for various combinations of inputs.

- The layout design will represent the transistor-level implementation of the inverter circuit. Once the layout is completed, the circuit will be simulated for various combinations of input signals to analyze the output behavior.

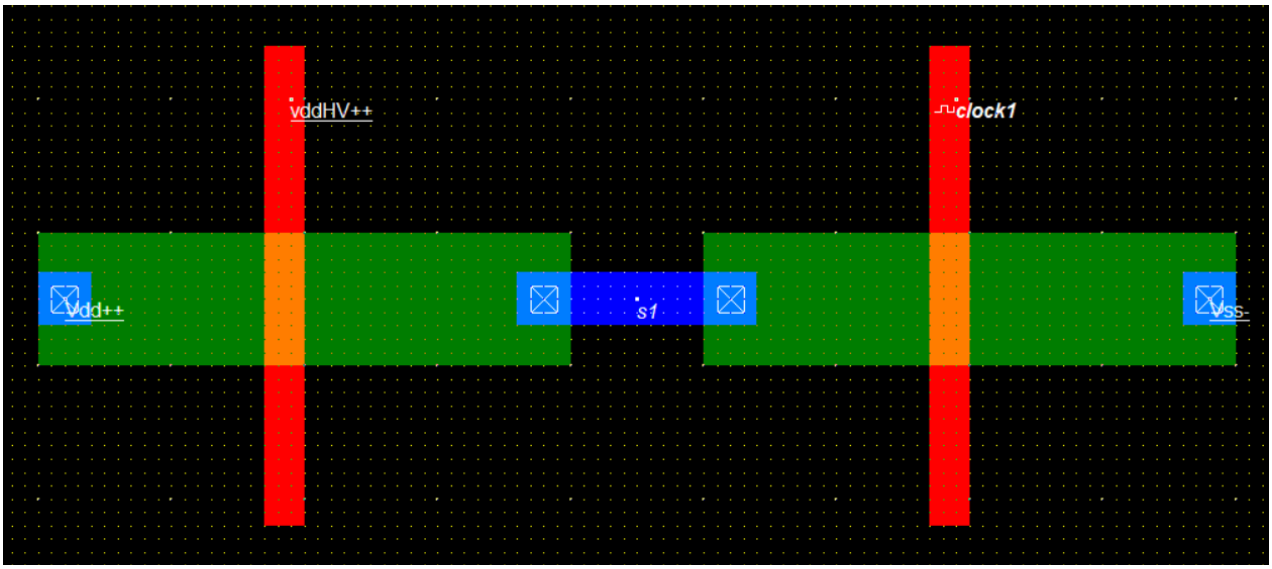


Figure 4: Layout using Microwind tool

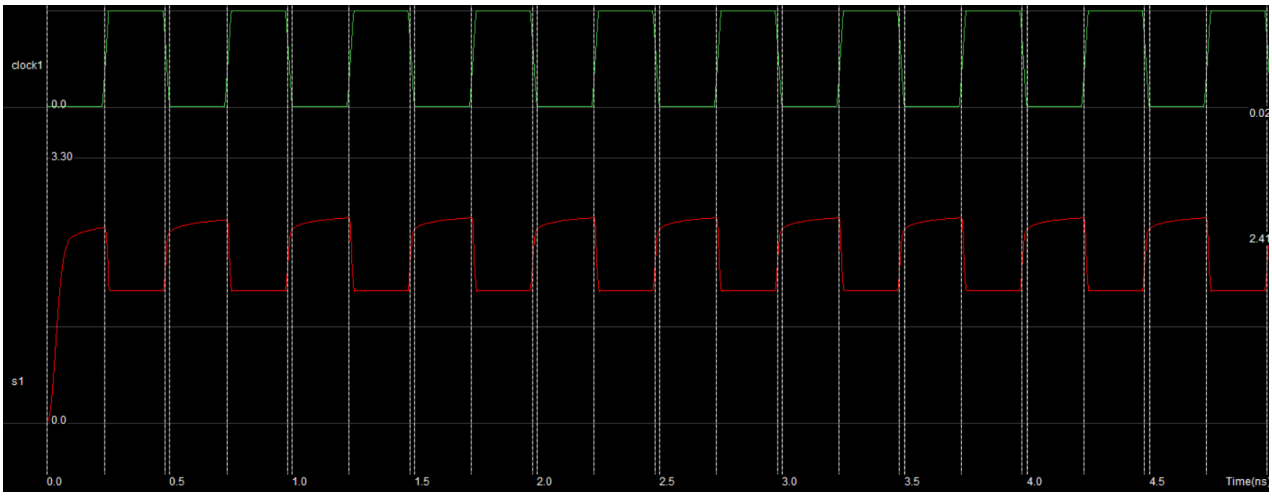
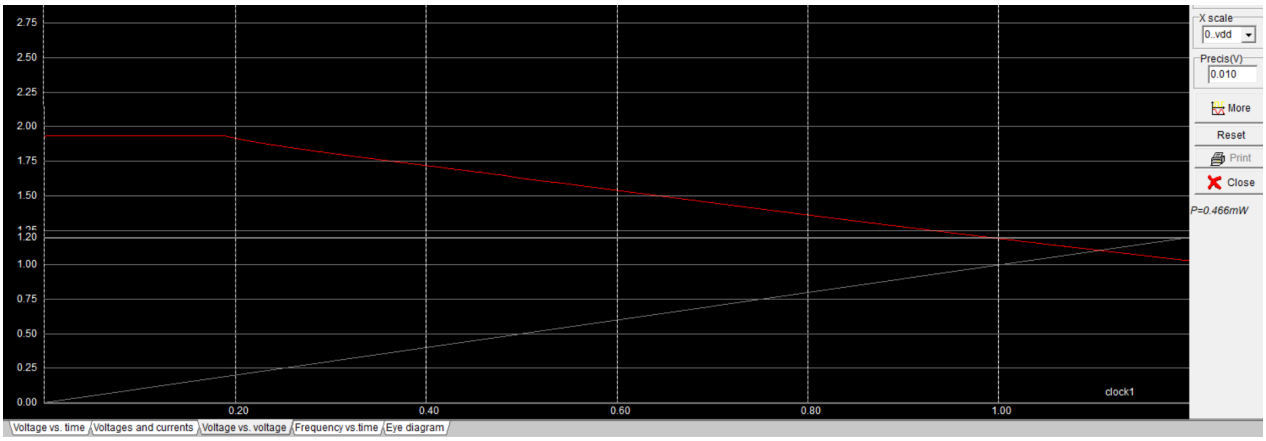


Figure 5: Simulation using Microwind tool



[11] Measure the rise time, fall time, propagation delay and other parameters.

- In Microwind, we can measure rise time, fall time, and propagation delay by simulating the circuit and analyzing the output waveforms. Rise time is the duration for the output to transition from 10% to 90%, while fall time is from 90% to 10%. Propagation delay is the time difference between the input signal's change and the output response.

Vdd=Vgg=1.2V

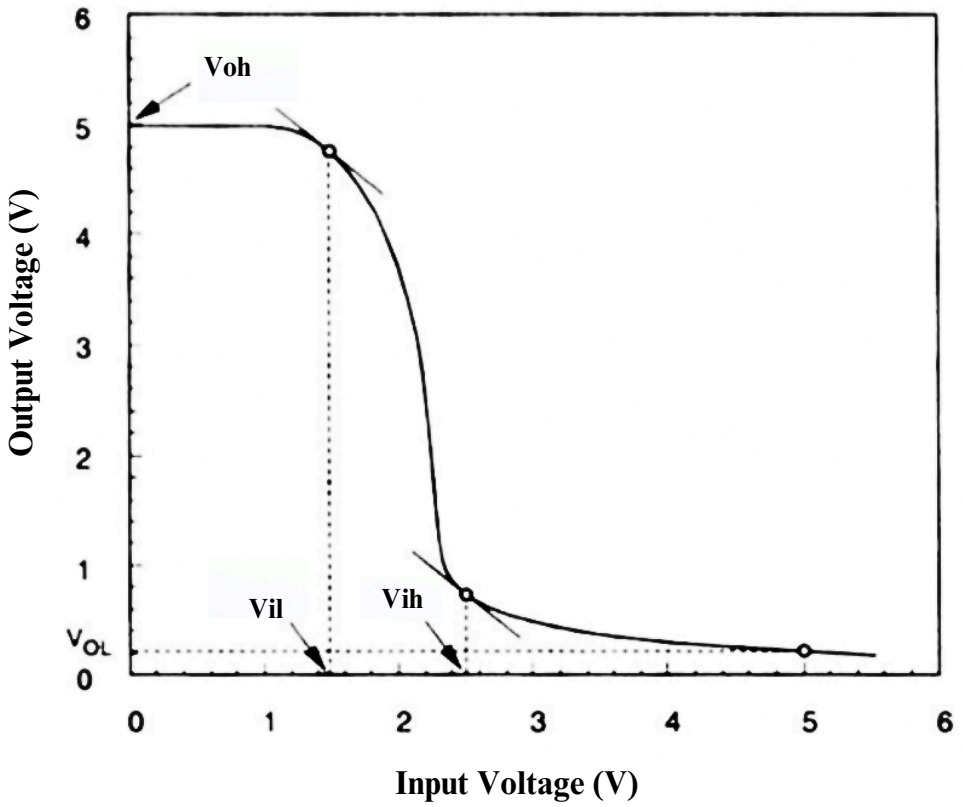
Sr. No.	Technology (L)	W of Load	W of Driver	Driver to Load Ratio	V_{OH}	V_{OL}	V_{IL}	V_{IH}	V_{TH}	τ_{pHL}	τ_{pLH}	Trise	Tfall
1	0.12	15	6	0.33	0.80	0.37	0.16	0.95	0.54	1ps	8ps	0.025	0.025
2	0.12	6	6	1	0.77	0.18	0.15	0.94	0.51	2ps	6ps	0.025	0.025
3	0.12	6	15	2.5	0.75	0.08	0.13	0.71	0.49	-	10ps	0.025	0.025

Vdd=1.2V, Vgg=2.5V

Sr. No.	Technology (L)	W of Load	W of Driver	Driver to Load Ratio	V_{OH}	V_{OL}	V_{IL}	V_{IH}	V_{TH}	τ_{pHL}	τ_{pLH}	Trise	Tfall
1	0.12	15	6	0.33	1.20	1	0.60	1.20	1.11	-	11ps	0.025	0.025
2	0.12	6	6	1	1.20	0.22	0.54	1.15	1.02	-	-	0.025	0.025
3	0.12	6	15	2.5	1.20	0.10	0.53	1.10	1.10	-	5ps	0.025	0.025

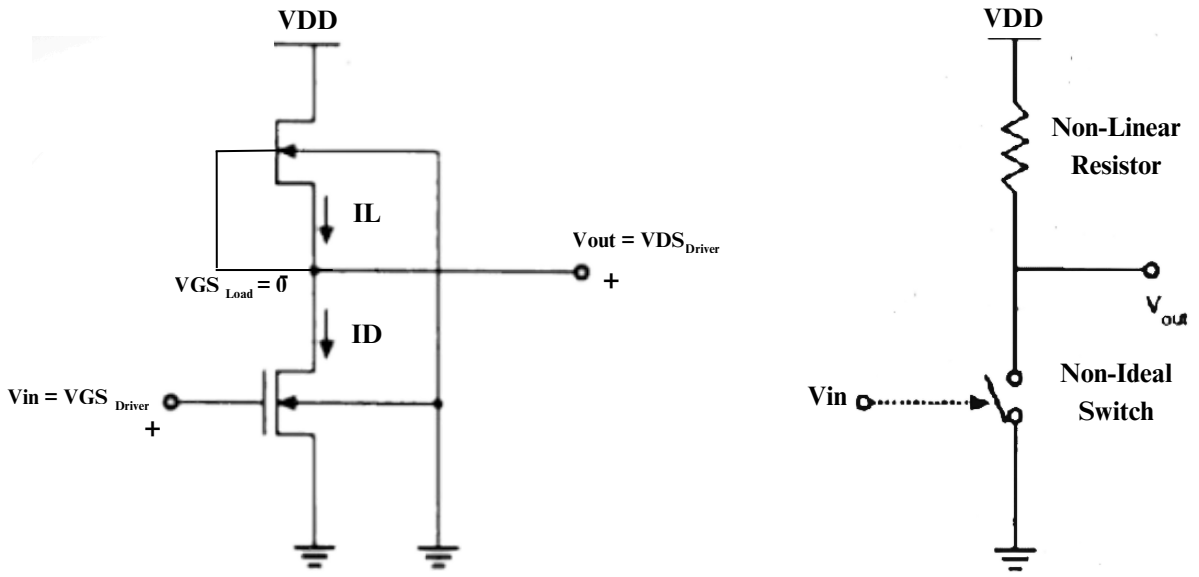
Table 2 & 3: Measured Parameters

[12] Prepare a detailed report with proper plots and theory including the answers of the above given questions. Also include the concluding remarks.



There are five parameters used to characterize the VTC curve voltage.

VOH: VOH voltage is a maximum output voltage at input logic '1'
VOL: VOL voltage is a minimum output voltage at input logic '0'.
VIL: VIL voltage is the maximum input voltage for interpreting as logic '0'.
VIH: VIH voltage is the minimum input voltage for interpreting as logic '1'.
Vth: When the output voltage is equal to the input voltage that the voltage call Vth Voltage.



So basically the above figure is for nMOS as inverter and nMOS as an active load. In this as driver nMOS is connected with the ground and the input is given in the form of VIN that is the clock and the load nMOS is connected to VDD. The gate source nodes of the load transistors are connected, hence VGS= 0. Since the threshold voltage of the depletion type load is negative, the condition VIoad > VT,Load is satisfied, and the load device always has a conducting channel regardless of the input and output voltage levels.

Also note that both the driver transistor and the load transistor are built on the same p-type substrate, which is connected to the ground. Consequently, the load device is subject to the substrate-bias effect, so that its threshold voltage is a function of its source-to substrate voltage, VSB load = Vout.

The operating mode of the load transistor is determined by the output voltage level.

Vin	Vout	Driver Region	Load Region
Vol	= Voh	Cut - off	Linear
Vil	>= Voh	Saturation	Linear
Vih	Near to 0	Linear	Saturation
Voh	Vol	Linear	Saturation

Table 4: Operating Mode of Load Transistor

Conclusion:

~ Using Microwind, accurately simulated the circuit, analyzed waveforms, and verified theoretical results with practical plots.
~ Also checked for different technology like 0.12µ, 0.18µ and 0.35µ by changing the W/L ratio to get proper output.
~ In order to improve VOL, W/L ratio should be increased and to improve VOH, VGS should be increased for NMOS, for appropriate output driver to load ratio should be around 2.5.
~ To improve VOL,W/L of driver has to be greater than W/L of load and for improved value of VOH, value of VGS should be as low as possible.