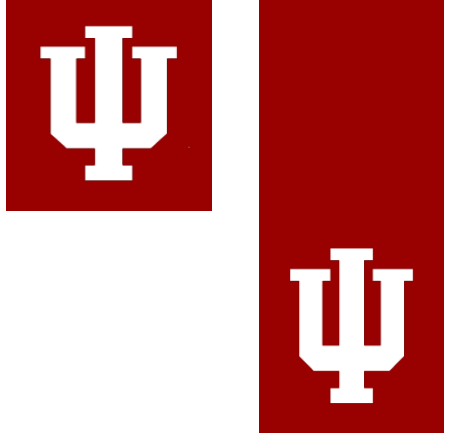
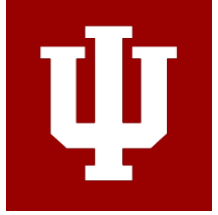


1.1 – Circuits & Layout

ENGR-E 399/599: VLSI Design

Prof. Daniel Loveless, dlovele@iu.edu, 812-856-0703

INDIANA UNIVERSITY – Reliable Electronics and Systems
Center for Reliable and Trusted Electronics (CREATE)



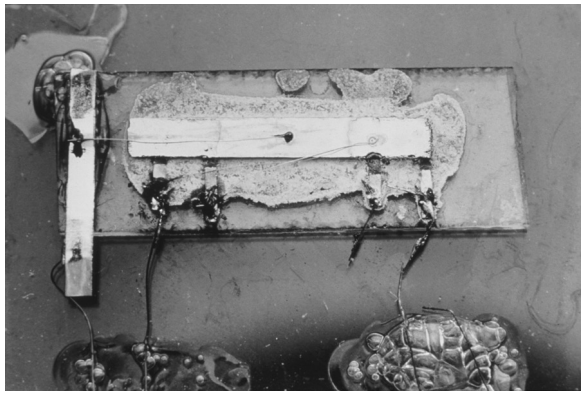
Learning Objectives

At the end of this lecture, you should be able to:

- Draw transistor-level schematics and layouts for complementary CMOS standard cells.
- Use time diagrams to describe the operation of D latch and D Flip-flop.
- Use stick diagrams to sketch and plan cell layouts.

A Brief History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2019
  - Apple A13 microprocessor
    - 8.5 billion transistors
  - Samsung 8 TB Flash memory
    - 2 trillion stacked transistors



Courtesy Texas Instruments

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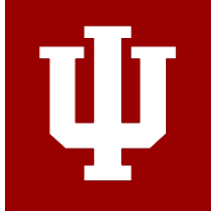
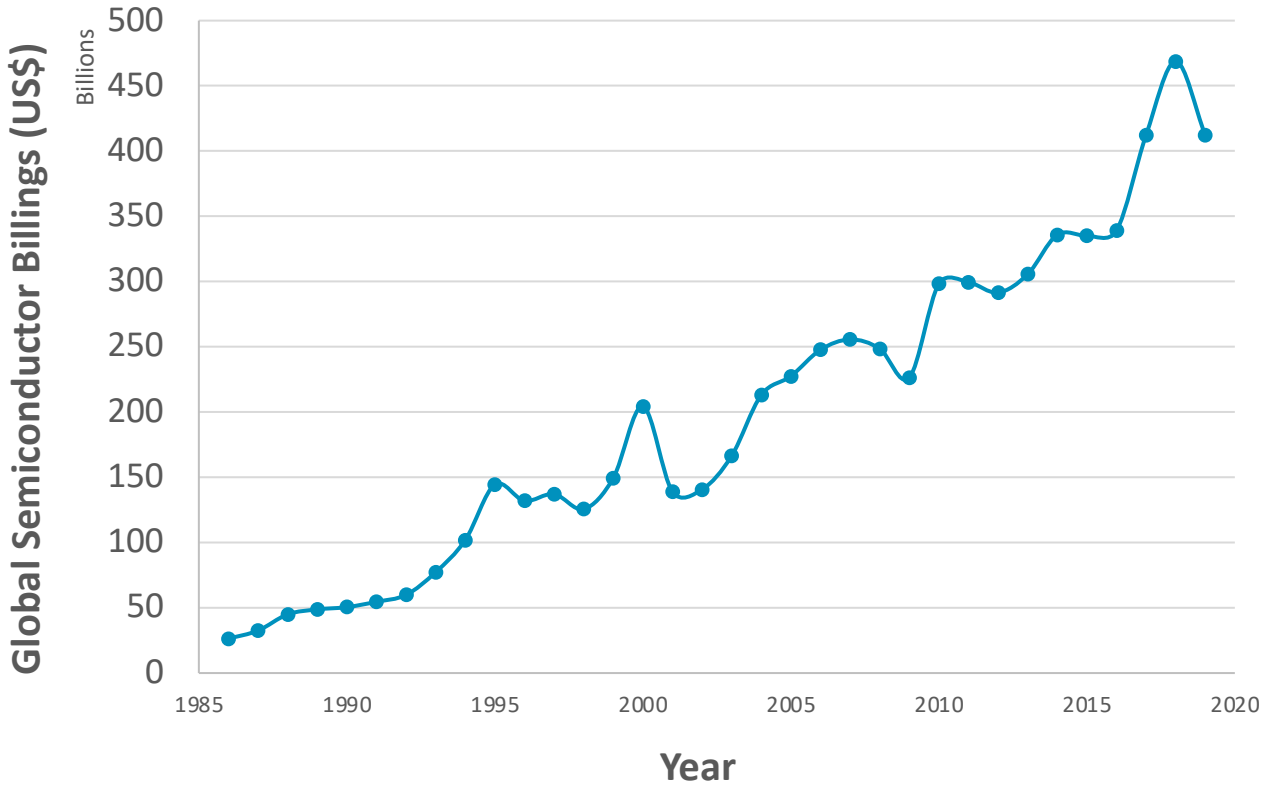


Growth Rate

- 53% compound annual growth rate over 50 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

Annual Sales

- >10^{20} transistors manufactured in 2017
  - 56 billion for every human on the planet



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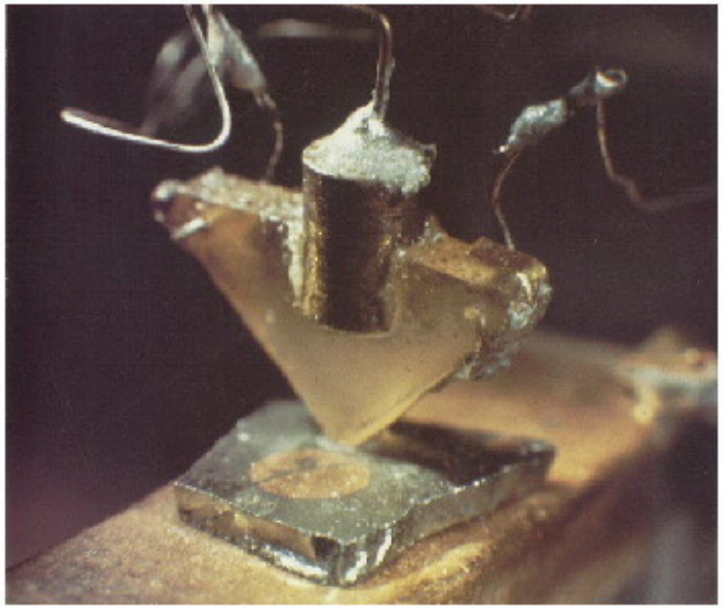
Invention of the Transistor

- Vacuum tubes ruled in first half of 20th century Large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
  - John Bardeen and Walter Brattain at Bell Labs
  - See *Crystal Fire* by Riordan, Hoddeson



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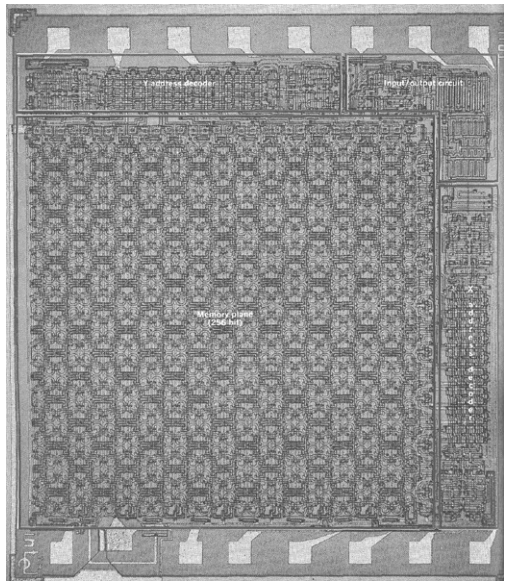
Transistor Types

- Bipolar transistors
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - Base currents limit integration density
- Metal Oxide Semiconductor Field Effect Transistors
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

MOS Integrated Circuits

- 1970's processes usually had only nMOS transistors
  - Inexpensive, but consumed power while idle



[Vadasz69]

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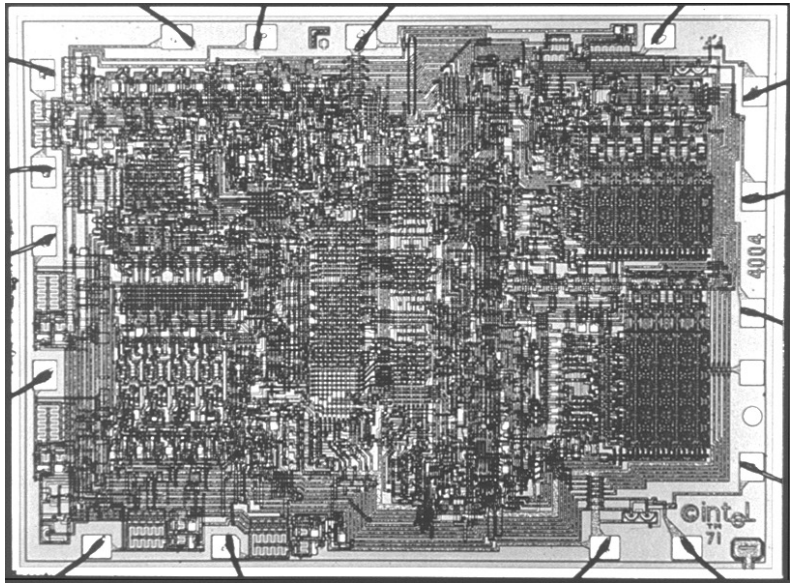

Intel Museum.

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Intel 1101 256-bit SRAM Intel 4004 4-bit μProc

- 1980s-present: CMOS processes for low idle power

Moore's Law: Then

- 1965: Gordon Moore plotted transistor on each chip
  - Fit a straight line on semilog scale
  - Transistor counts have doubled every 26 months

Integration Levels

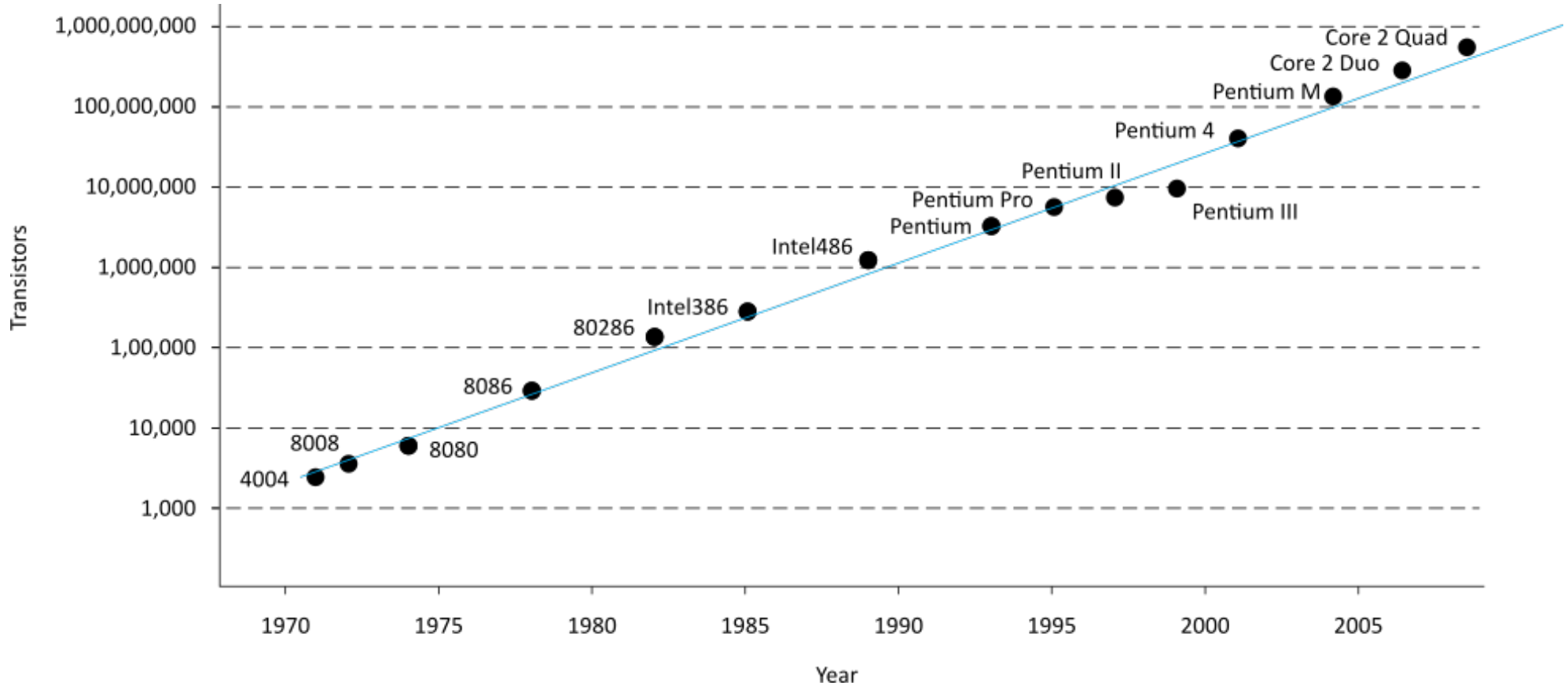
SSI: 10 gates

MSI: 1000 gates

LSI: 10,000 gates

VLSI: >10k gates

And Now…


1,000,000,000
100,000,000
10,000,000
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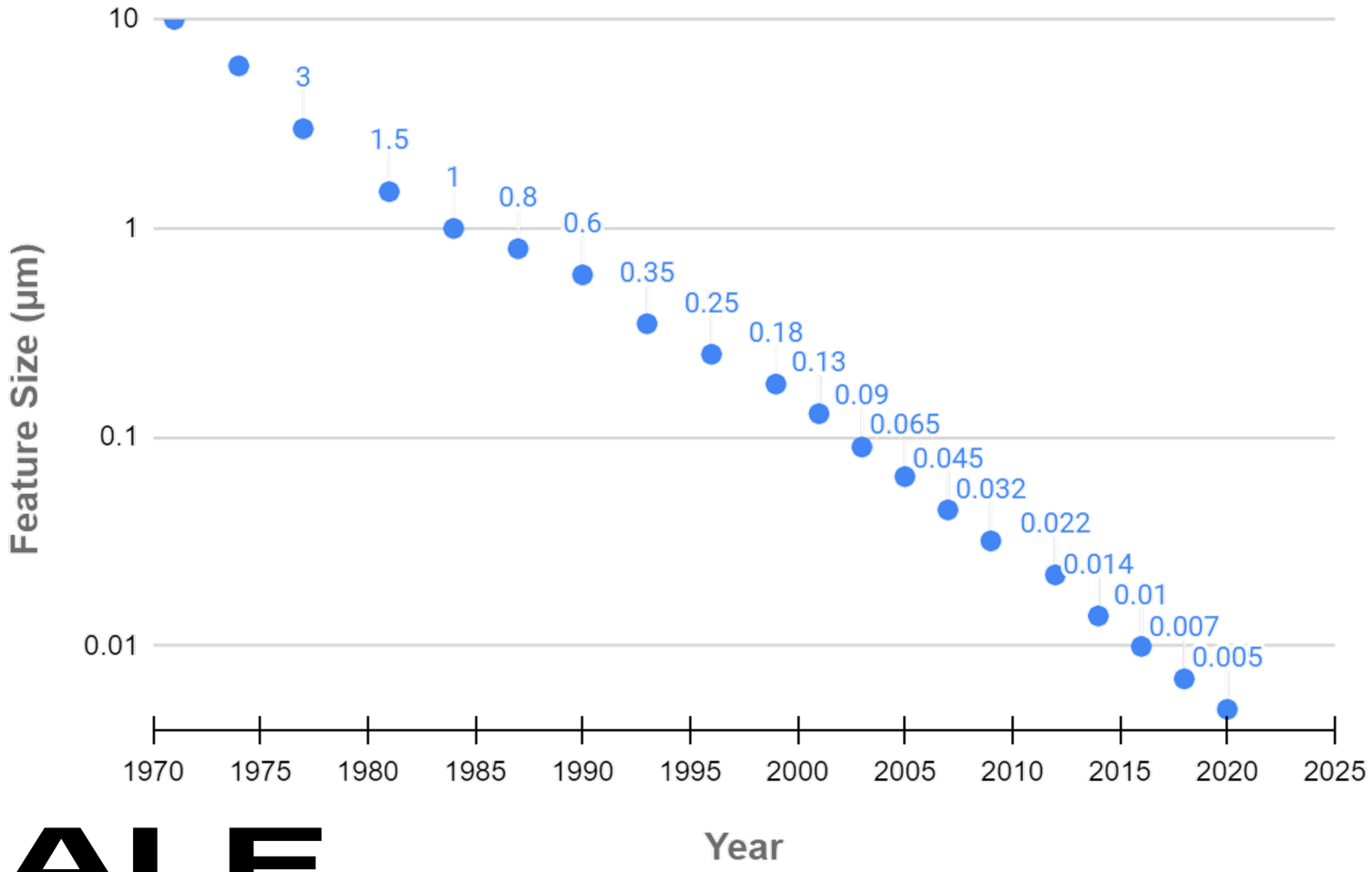
Transistors
1970
1975
1980
1985
1990
1995
2000
2005
Year
4004
8008
8080
8086
80286
Intel386
Intel486
Pentium
Pentium Pro
Pentium II
Pentium III
Pentium 4
Pentium M
Core 2 Duo
Core 2 Quad

Feature Size

- Minimum feature size shrinking 30% every 2-3 years



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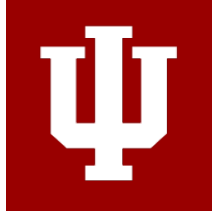


Corollaries

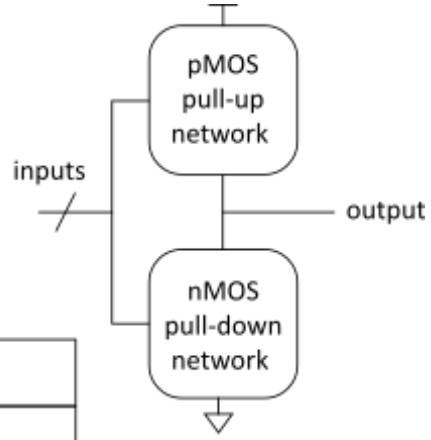
- Many other factors grow exponentially
  - E.g., clock frequency, processor performance

Year	Clock Speed (Hz)	Processor name
1971	740K	4004
1972	500K	8008
1982	6M	80186
1982	8M	80188
1993	66M	Pentium
1999	600M	Pentium III
2000	2G	Pentium 4
2006	2.33K	Core 2 Duo
2008	3.2G	Core i7
2011	2.67G	Xeon E7
2013	4.4G	Intel "Haswell"

Intel Processors, year and clock speed

Complementary CMOS

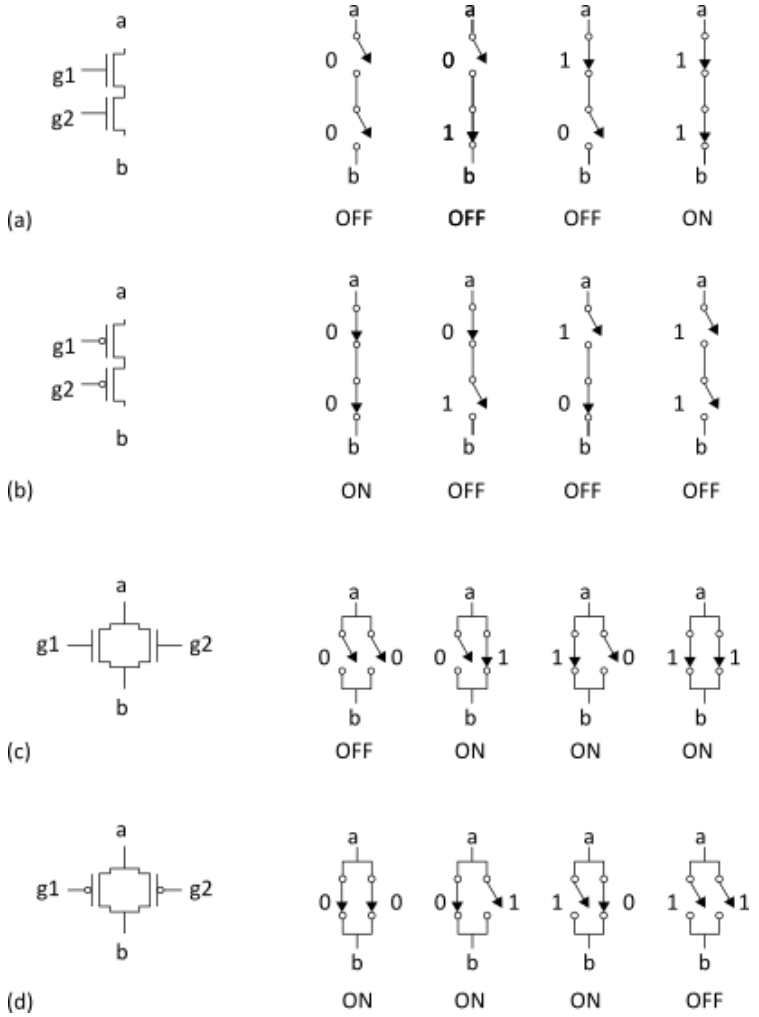
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

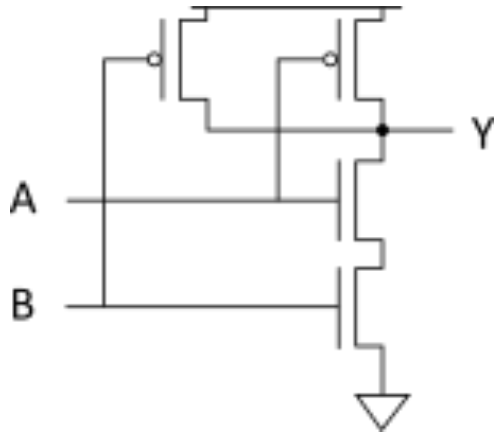
Series and Parallel

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



Conduction Complement

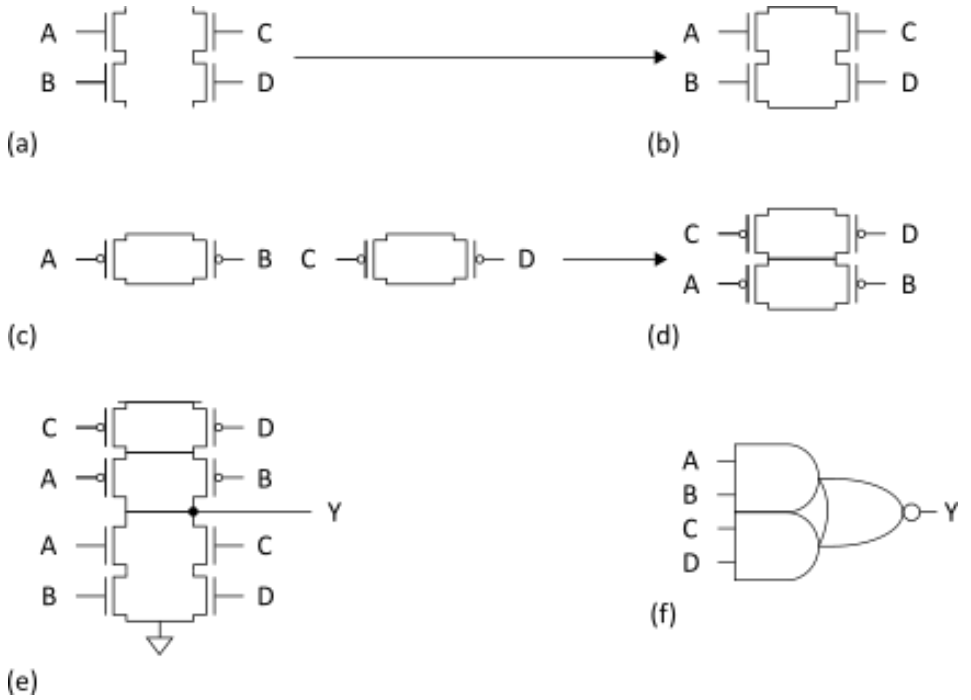
- Complementary CMOS gates always produce 0 or 1
- E.g., NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus, Y=1 when either input is 0
  - Requires parallel pMOS
- Rule of *Conduction Complements*
  - Pull-up network is a complement of pull-down
  - Parallel -> series, series -> parallel



Compound Gates

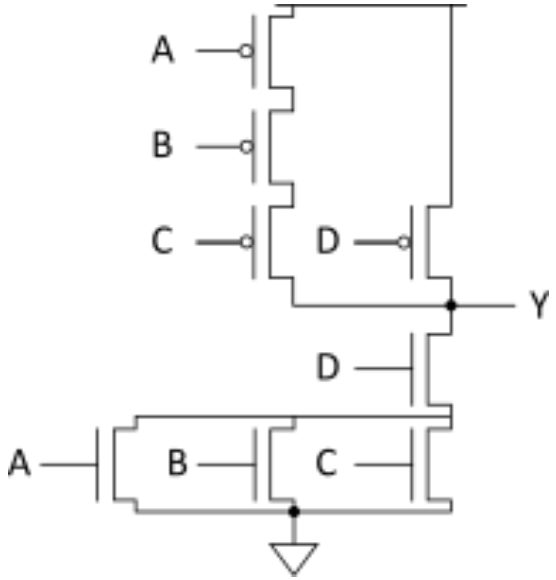
- *Compound gates* can do any inverting function
- E.g.,

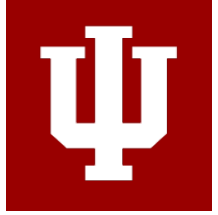
$$Y = \overline{A \bullet B + C \bullet D} \text{ (AND-AND-OR-INVERT, AOI22)}$$



Example: O3AI

$$Y = \overline{\left(A + B + C\right) \bullet D}$$



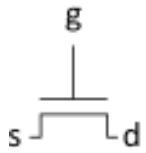


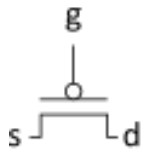
Signal Strength

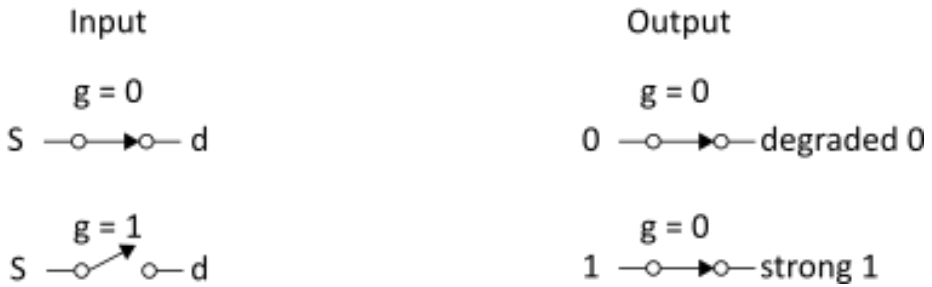
- *Strength* of signal
  - How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus, nMOS are best for pull-down network

Pass Transistors

- Transistors can be used as switches







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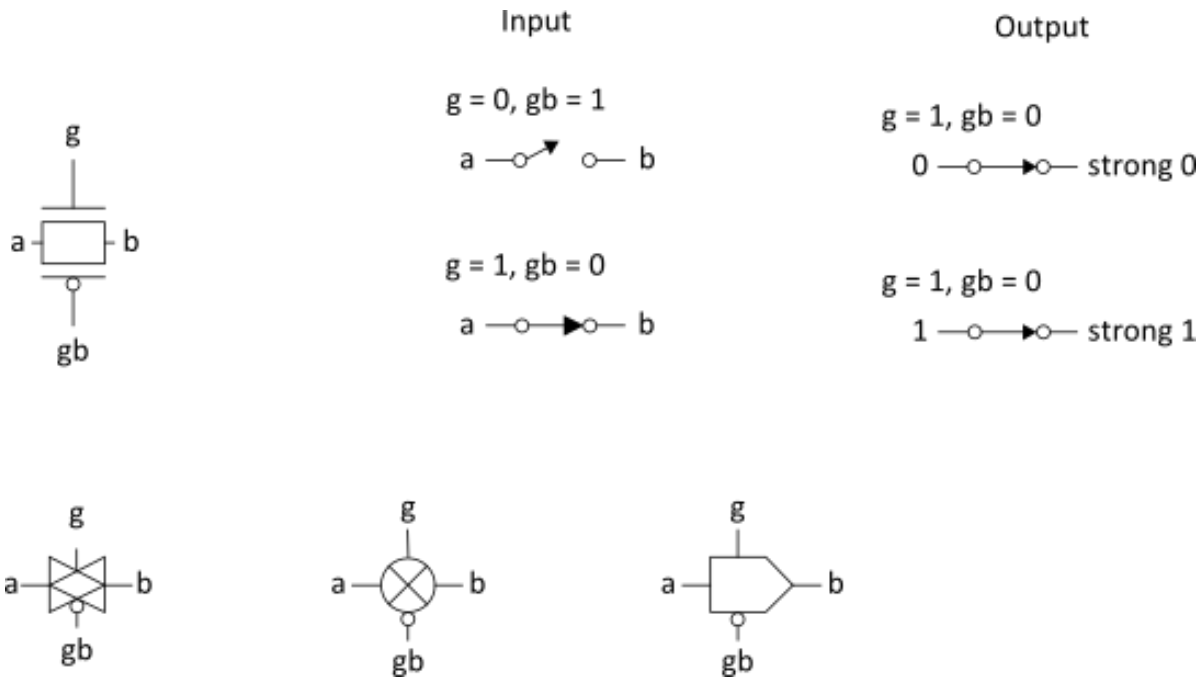
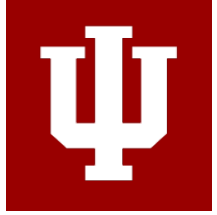
Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

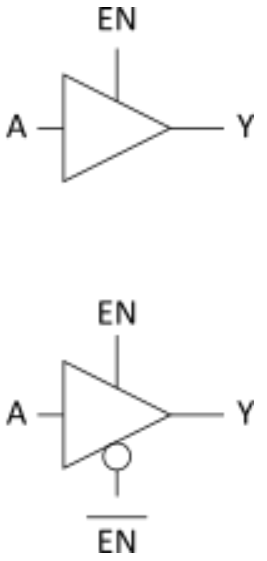




Tristates

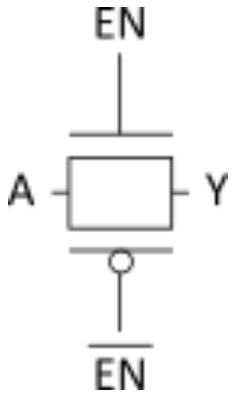
- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



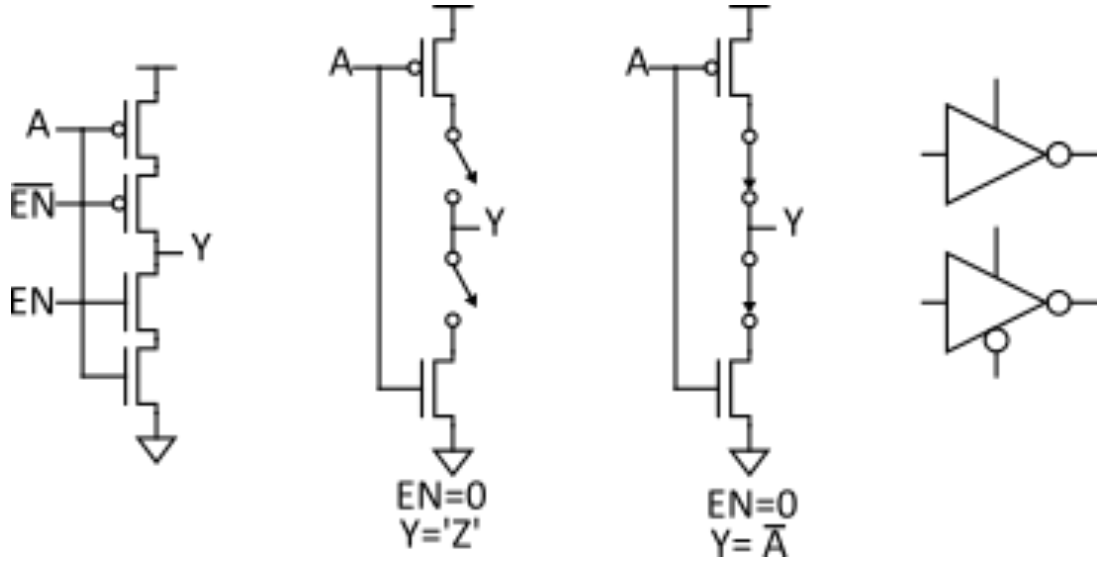
Nonrestoring Tristate

- Transmission gate acts as a tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y



Tristate Inverter

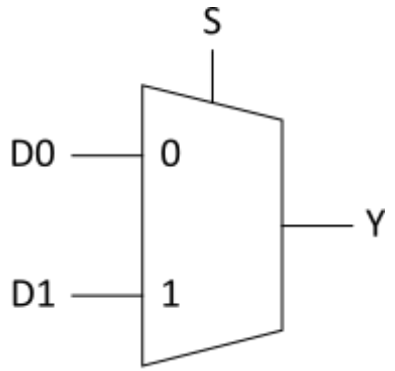
- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output

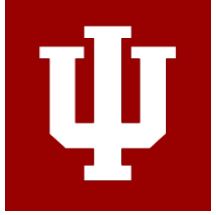


Multiplexers

- 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1





Gate-Level Mux Design

- $Y = SD_1 + \overline{S}D_0$ (too many transistors)
- How many transistors are needed?

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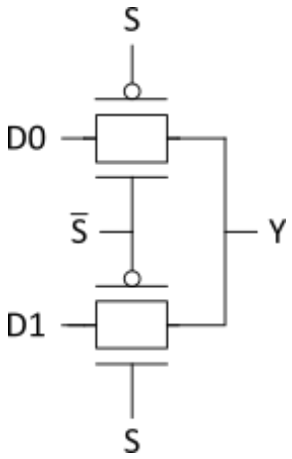
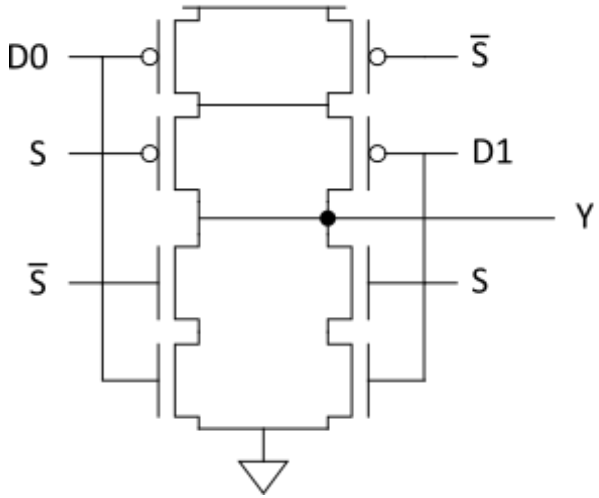
Transmission Gate Mux

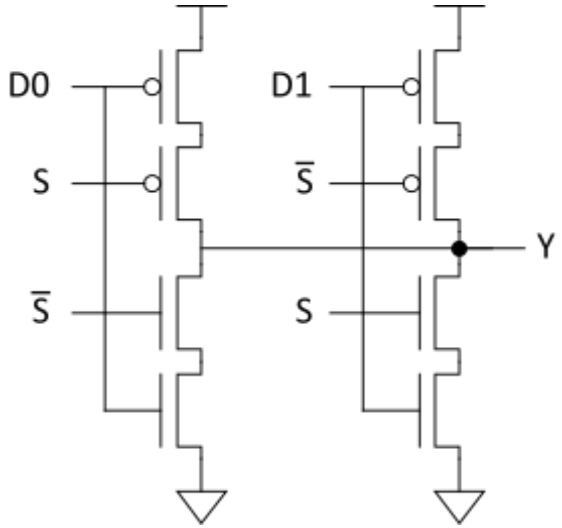
- Nonrestoring mux uses two transmission gates
  - Only 4 transistors

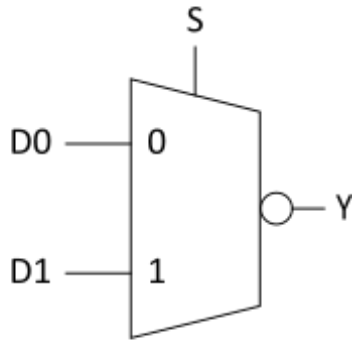


Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or a pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter

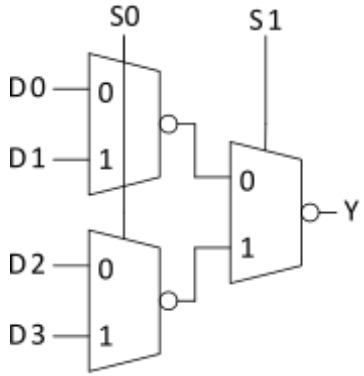


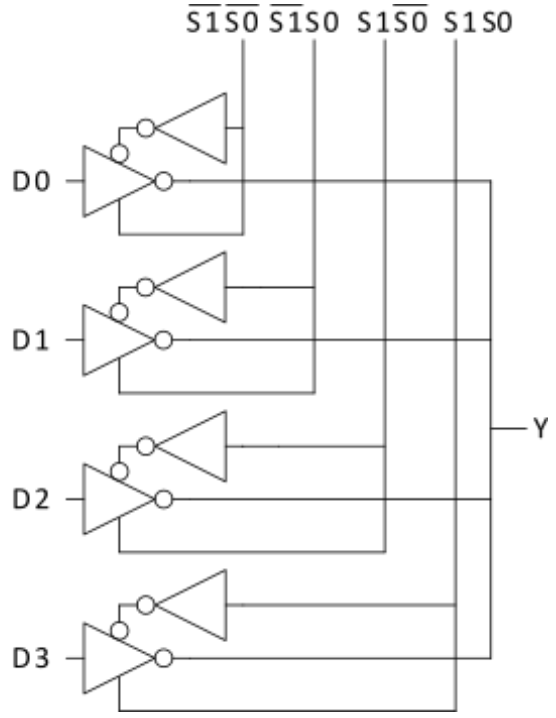




4:1 Multiplexer

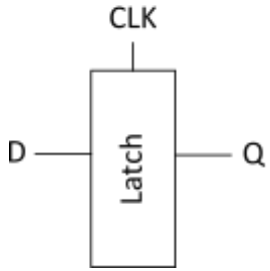
- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates

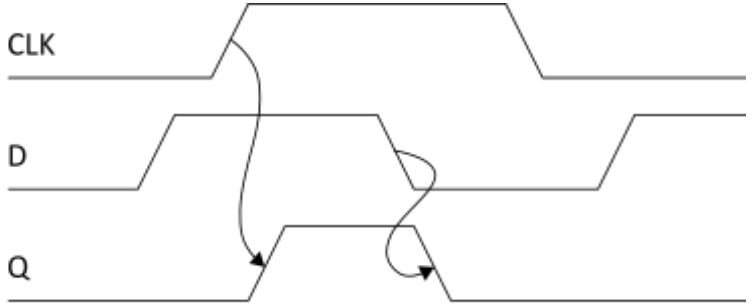




D Latch

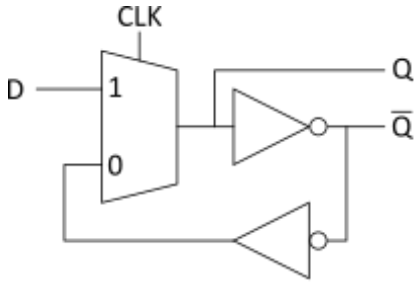
- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- Aka *transparent latch* or *level-sensitive latch*

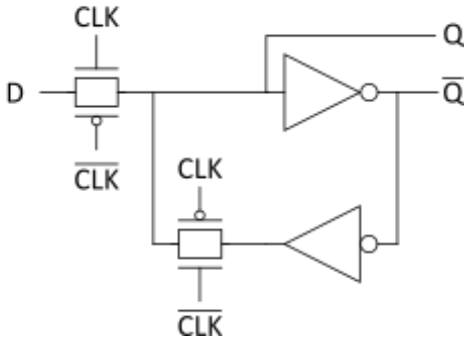




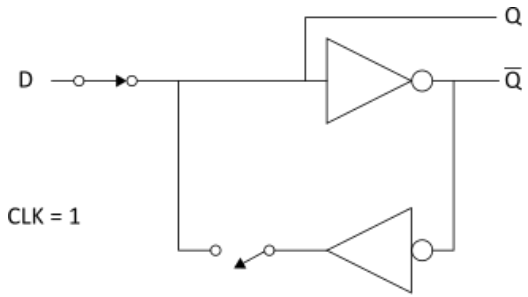
D Latch Design

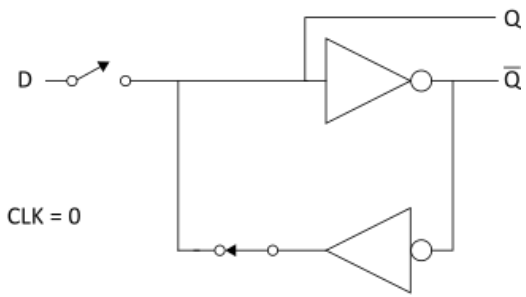
- Multiplexer chooses D or old Q

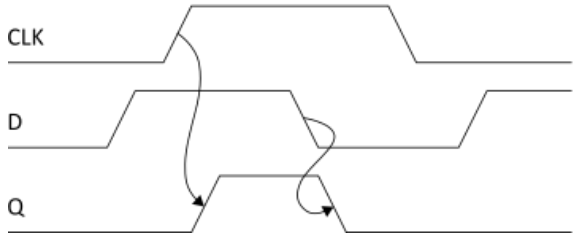




D Latch Operation

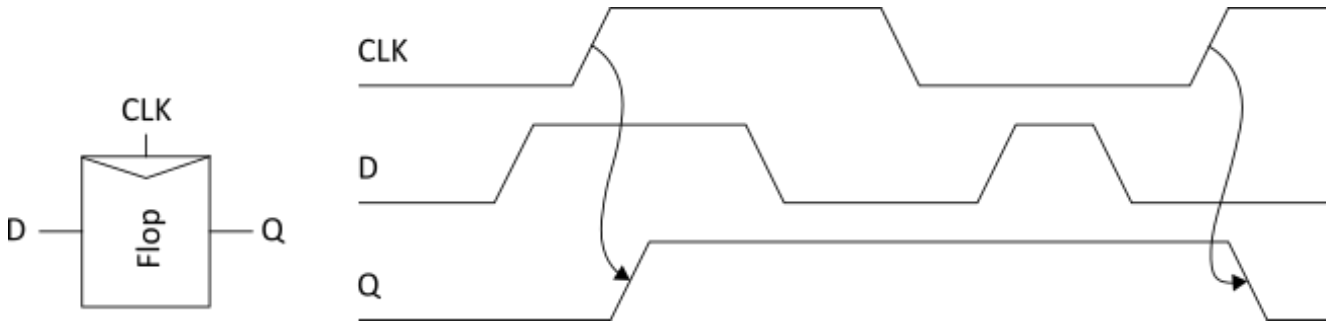






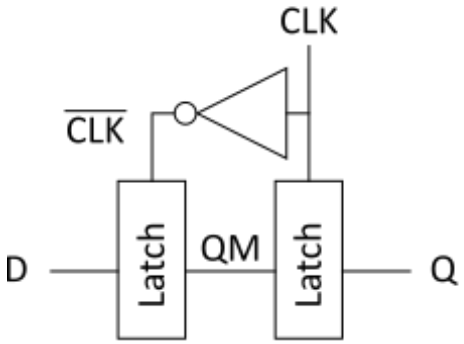
D Flip-flop

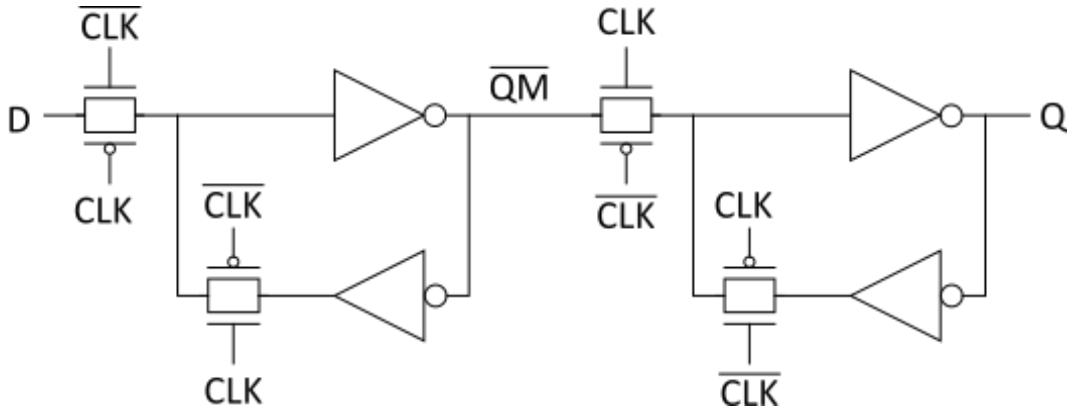
- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- aka *positive edge-triggered flip-flop*, *master-slave flip-flop*



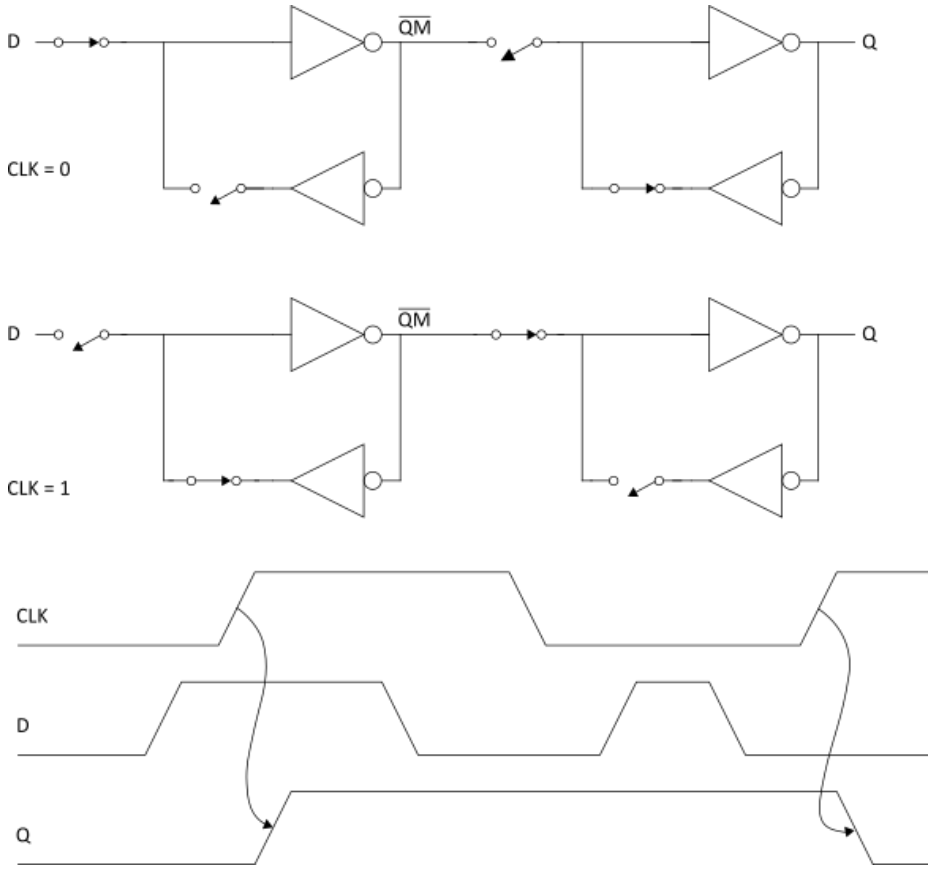
D Flip-flop Design

- Built from two D latches, a primary and secondary D latches



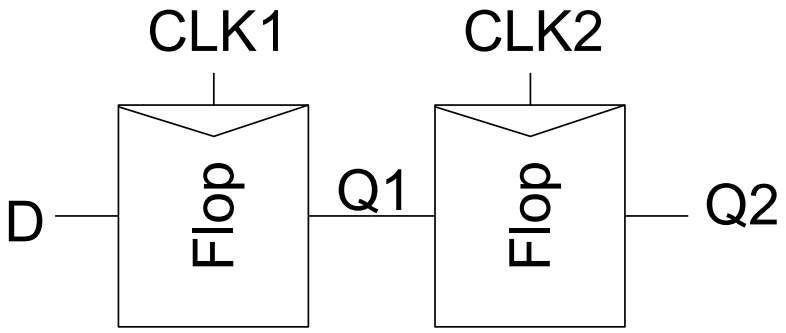


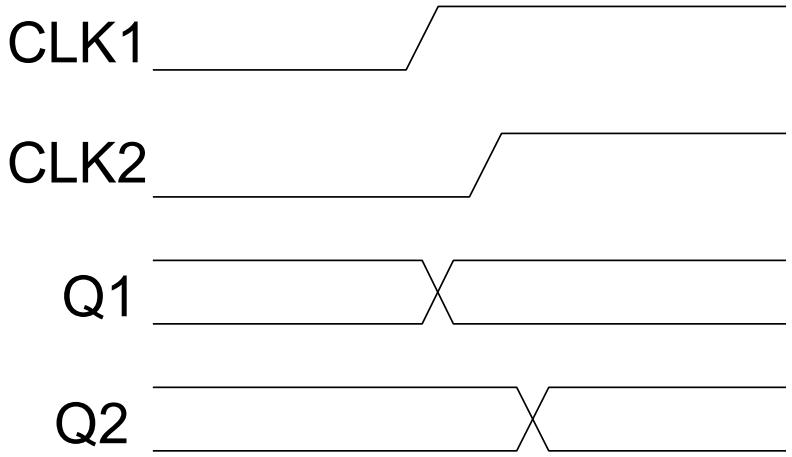
D Flip-flop Operation



Race Condition

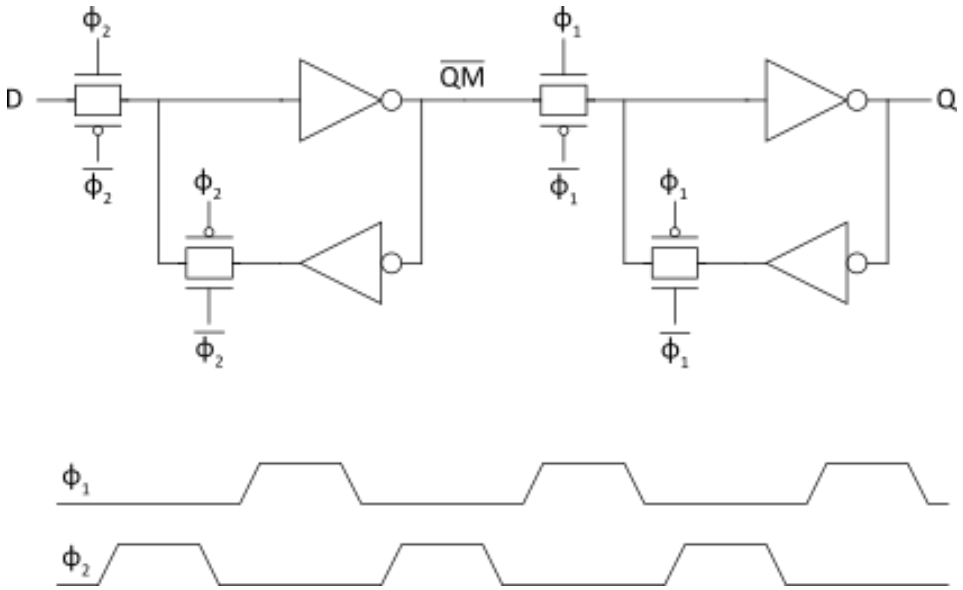
- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*





Nonoverlapping Clocks

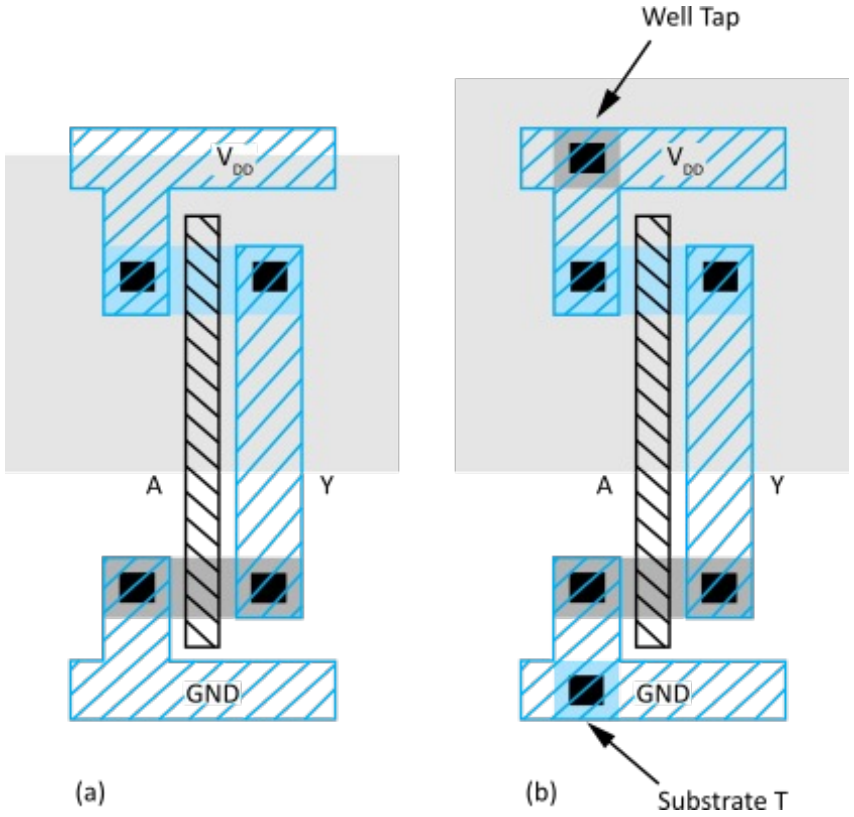
- Nonoverlapping clocks can prevent races
  - As long as nonoverlap exceeds clock skew
- We will use them in this class for safe design
  - Industry manages skew more carefully instead



Gate Layout

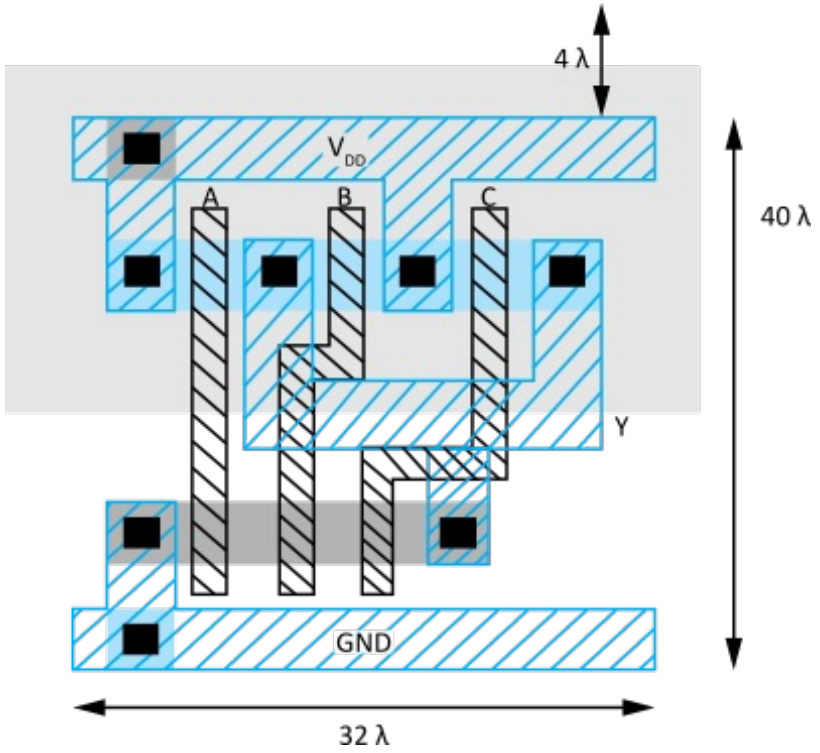
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Example: Inverter



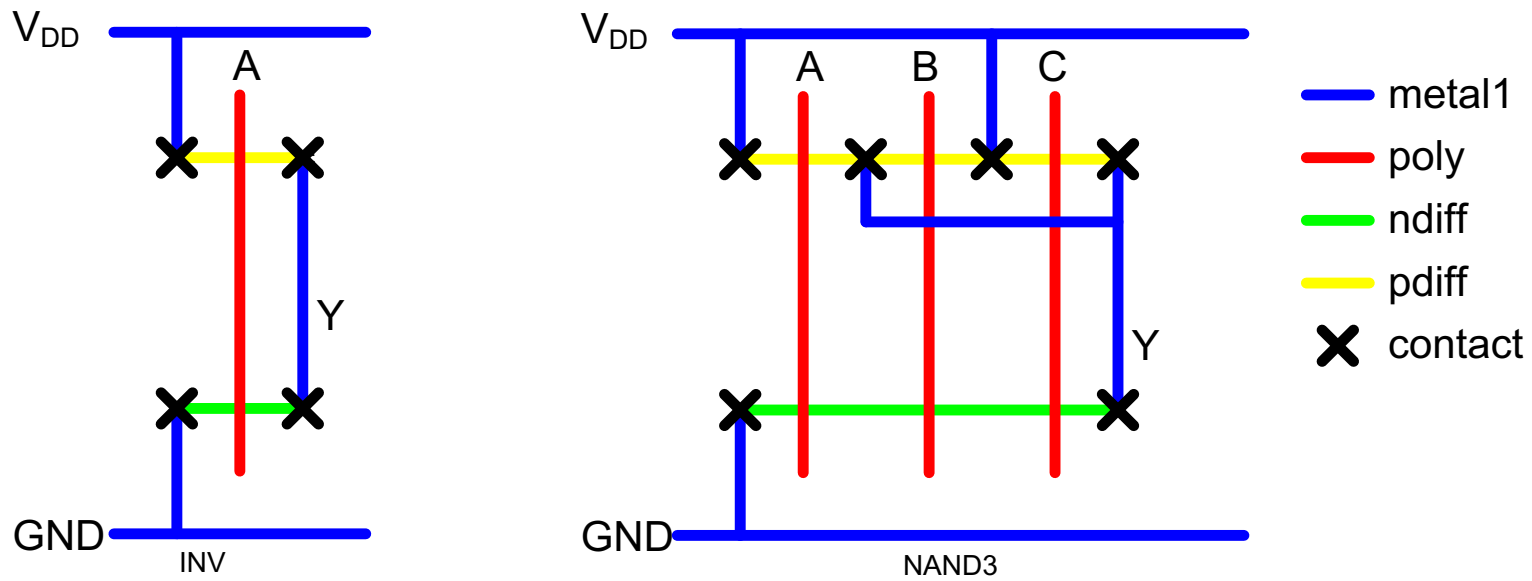
Example: NAND3

- Horizontal n-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal 1 V_{DD} rail at top
- Metal 1 GND rail at bottom
- 32 λ by 40 λ



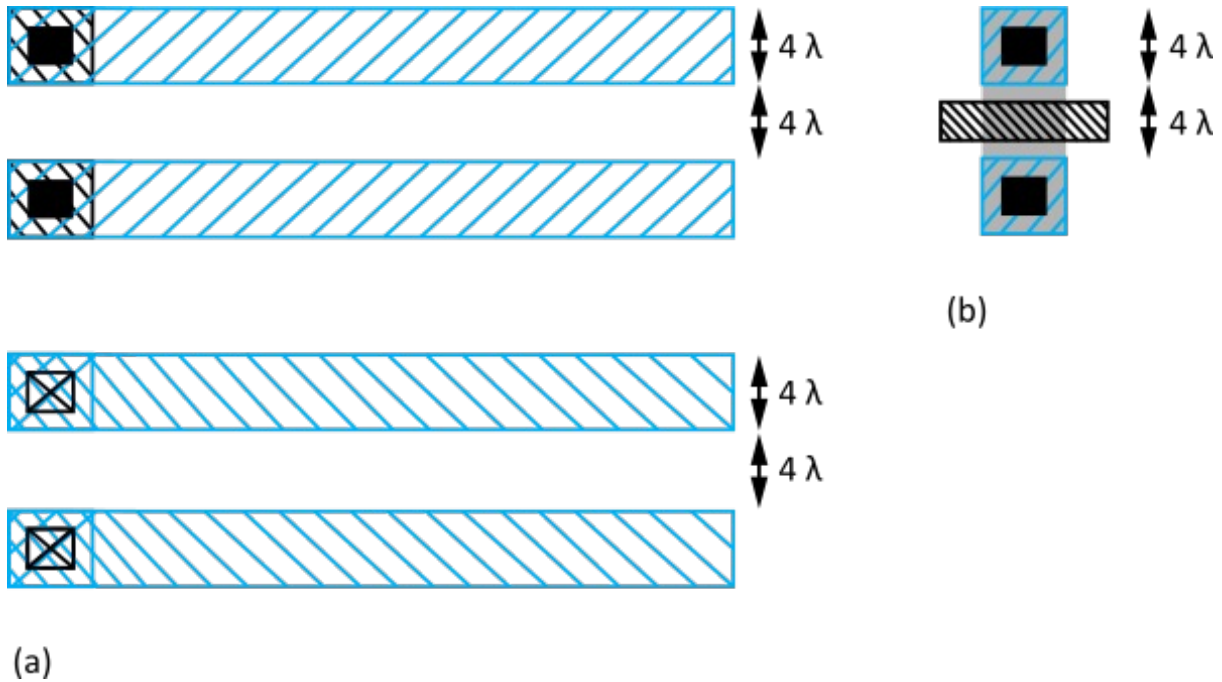
Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be scaled
  - Draw with color pencils or dry-erase markers



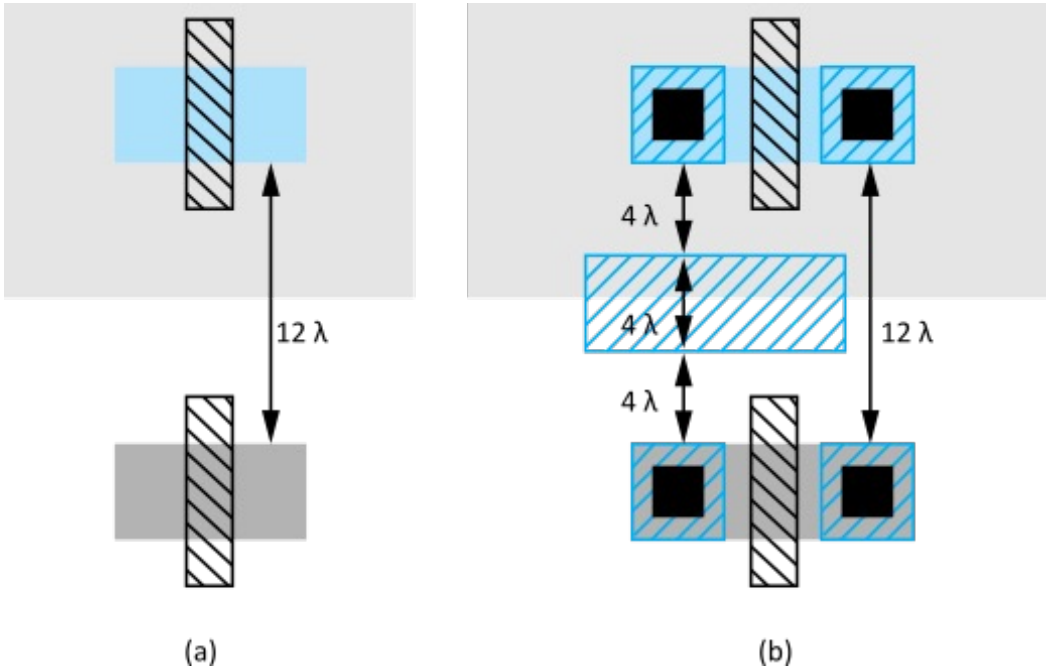
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



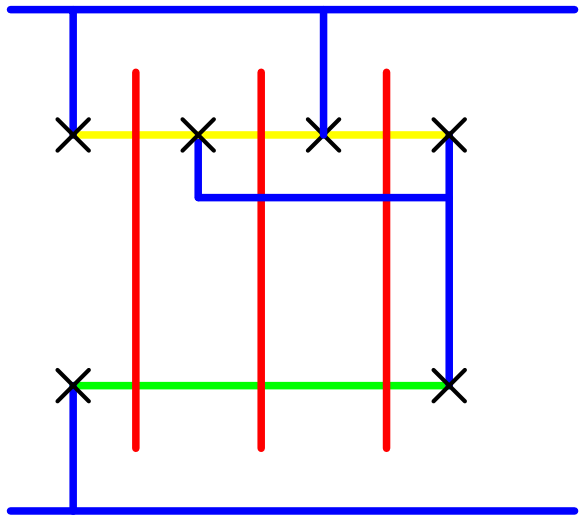
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



Area Estimation

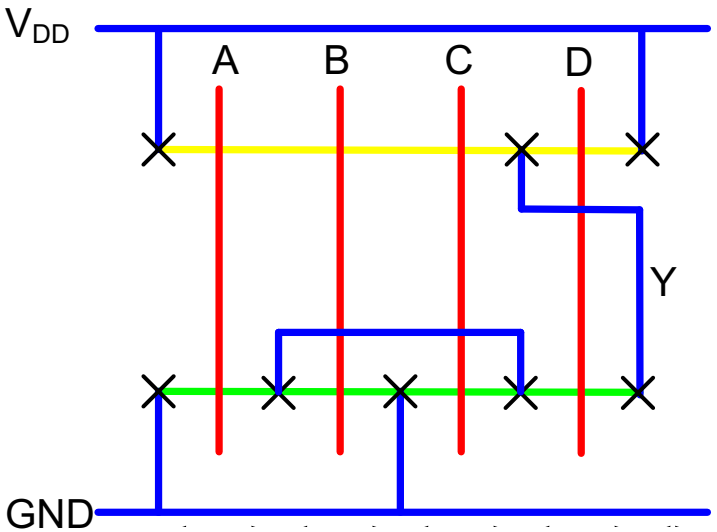
- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

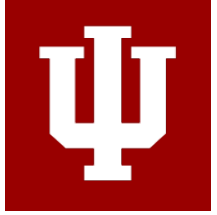


Example: O3AI

- Sketch a stick diagram for O3AI and estimate area
  -

$$Y = \overline{(A + B + C) \bullet D}$$





Modern Design Rules

- Rules are expressed in nanometers, not λ
- Lithography becomes difficult when feature size is less than the wavelength of light
- At 16 nm and below, design rules are highly restrictive
  - Layers have preferred directions, and no bends are allowed
  - Only certain widths are allowed
  - Minimum area of each rectangle
  - Complex rules for power busses
  - Thousands of design rules
  - Layout becomes the domain of full-time experts
- But the principles of layout remain valid