Nanomagnetic Logic Clocked in the MHz Regime

M. Becherer*, J. Kiermaier*, S. Breitkreutz*, I. Eichwald*, G. Csaba†, D. Schmitt-Landsiedel*

*Technische Universität München, Lehrstuhl für Technische Elektronik, 80333 München, Germany

†University of Notre Dame, Center for Nanoscience and Technology, Notre Dame, IN, 46556-5637, USA

Email: markus.becherer@tum.de

Abstract— **Perpendicular Nanomagnetic Logic (pNML) is a computing concept, where the local magnetization and fringing fields of ferromagnets are used to store and process information. So far, pNML devices have been exclusively operated at millisecond time scales. In this work, pNML magnets are clocked by a planar on-chip inductor at frequencies ranging from 100 kHz to 10 MHz. The inherent switching field (SF) and SF distribution (SFD) of an individual magnet is determined. An Arrhenius equation is used in order to model the SFD. Furthermore, a magnetic power-clock, implemented by an on-chip inductor with ferromagnetic cladding, is proposed and analyzed by finite element simulations. With the extracted data, an estimate of the power density of a scaled pNML computing system is given.**

I. INTRODUCTION: THE CONCEPT OF NML

Nowadays, digital computation is almost exclusively performed with charge-based CMOS circuits. However, there are several drawbacks associated with ultimately scaled CMOS implementations. High power consumption due to leakage currents, costly clock trees introducing skew and jitter and high system complexity owing to different levels of embedded memories for data storage.

From an architectural point of view, nonvolatile computing states are very attractive [1] as they inherently combine memory and computing ability. This leads to an alternative implementation of digital computation realized by field-coupled single-domain magnets with perpendicular magnetization: perpendicular NML. It is promising for highly parallel, pipelined, dense and low power applications [2], [3]. Electrical interconnects are reduced to a minimum as computation takes place by magnetic field coupling [4]. However, more research is needed in order to create flexible hybrid pNML-CMOS systems for next generation microelectronic modules.

II. CLOCKING AND NON-RECIPROCITY IN NML

A key element for operational NML circuits is the magnetic clocking field. The magnets are stimulated in such a way, that they locally relax to the lowest energy state (anti-parallel ordering). Thus, digital decisions (such as majority votes) are performed. However, most NML implementations do not provide a simple clocking concept and error rates increase for configurations with more than several magnets [5]. One of the key advantages of our perpendicular NML is the non-reciprocal signal propagation in spatially homogeneous clocking fields. It is implemented by local ion irradiation of magnetic islands as demonstrated in [6] and applied in inverter chains with a synchronous power-clock implementation [7], [8]. Fig. 1 reviews the concept: Focused Ion Beam (FIB) ir-
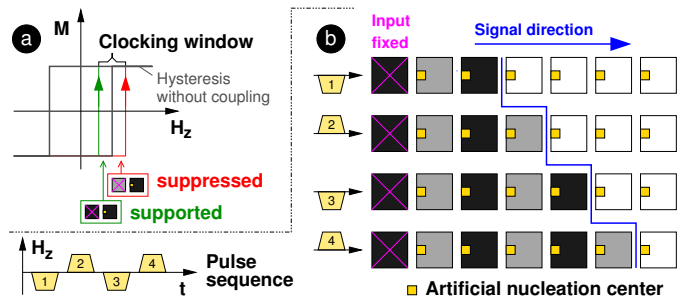

Fig. 1. a) Due to field-coupling, the switching of a magnet is either *supported* or *suppressed*. b) Signal directionality is achieved by alternating field-pulses H_z applied to locally irradiated magnets. The *Signal = 'anti-parallel ordering'*, propagates along a chain of magnets.
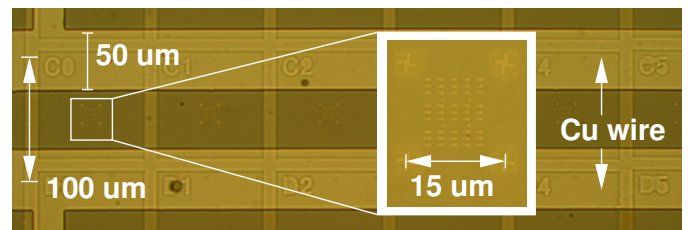

Fig. 2. Optical micrograph of the Cu meander inductor and close-up view of the analyzed magnet array.

radiation is applied to locally reduce perpendicular anisotropy and so-called artificial nucleation centers (ANCs) are formed. At the ANCs the magnetic material is highly susceptible to fringing fields. Alternate field pulses are applied in order to *clock* adjacent magnets into the lowest energy (anti-parallel) state.

III. EXPERIMENTAL DETAILS

A. Sample Preparation

Co/Pt multilayer films are sputtered on oxidized Si-substrates with the composition of $Ta_{3nm}/Pt_{3nm}/4x[Co_{0.8nm}+Pt_{1nm}]/Pt_{4nm}$. Magnetic islands are patterned by FIB lithography and low energy Ar ion beam etching. The meander inductor (Fig. 2) is deposited in a subsequent fabrication step and used to provide magnetic clocking fields. It encloses the array of magnets with a repetition pitch of 100 μm and Cu wires of 50 μm width. A consecutive Ga^+ FIB irradiation at 50 keV and areal dose of $1.7 \cdot 10^{13}$ ions/cm² for ANC creation is visualized in the Scanning Electron Microscopy (SEM) image of Fig. 3.
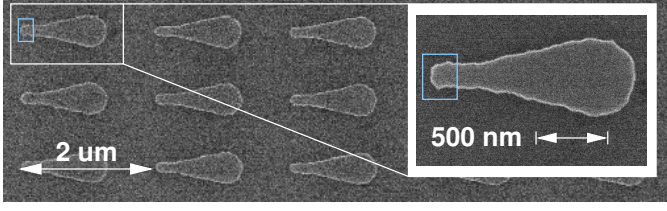
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Fig. 3. SEM image of the fabricated magnet array and close-up view of the analyzed magnet. FIB irradiation is schematically visualized by (blue) rectangles as it is not visible in the measured SEM image.

Fig. 4. Cumulative SFD of the magnet measured for different pulse times t_p and fitted by the Arrhenius model.

t_p/ µs	0.1	0.2	0.5	1	5	10	30 ms	S-Fit
$E_0/k_B T$	80	87	108	87	88	80	83	55
B_{s0}/mT	143	124	109	114	116	118	63	133

B. SFD measurements by magneto-optical Kerr-microscopy

For SFD measurements, a laser scanning magneto-optical Kerr-microscope is applied. The magnetic field is generated with either an external electromagnet for pulse times $t_p \geq 10$ ms or current pulses through the on-chip meander inductor for $t_p \leq 10$ µs. In order to record the cumulative SFD of the nanomagnet at fixed pulse time t_p, 100 positive pulses of constant amplitude, each followed by a negative saturation pulse for resetting the magnetic state, are applied. After this sequence, the pulse amplitude is increased by typically $\Delta B = 0.5$ mT at which the next sequence is recorded. This procedure is continued until the pulsing amplitude yields 100% switching probability of the device under test (DUT).

IV. SFD OF A SUB-MICRON MAGNETIC ISLAND

In this work, two sets of equations are used to model the magnetization reversal of the magnet. Both describe the probability of overcoming an energy barrier by applying an external field under existing thermal excitation. Both equations are derived from the ideal case of a so-called *Stoner-Wohlfarth particle*. Here these models are applied to a switching process, where a nucleation event triggers the reversal by domain wall motion.

A. Arrhenius switching model

The probability P_{sw} that the magnetization of a magnet is reversed in an external field is given by [9]

$$P_{sw}(t_p, B) = 1 - \exp\left(-t_p/\tau(B)\right) \qquad (1)$$

$$\tau(B) = f_0^{-1} \exp\left(\frac{E_0 \cdot (1 - \frac{B}{B_{s0}})^2}{k_B T}\right) \qquad (2)$$

with $\tau(B)$: inverse of the switching rate, $B = \mu_0 H$: magnetic induction, t_p: pulse time, $f_0 = 2 \cdot 10^9$ Hz: reversal attempt frequency, E_0: energy barrier at zero field, μ_0: magnetic vacuum permeability, B_{s0}: magnetic switching field[1] at zero temperature, k_B: Boltzmann constant and $T = 293$ K: ambient temperature. For this study, the Arrhenius-model is fitted to the measured cumulative SFDs and the widths of the SFDs by percentiles are determined.

[1]For brevity, the magnetic flux density B is denoted by a *'field'* as it is easily converted to a magnetic field H with the equation $H = B/\mu_0$.
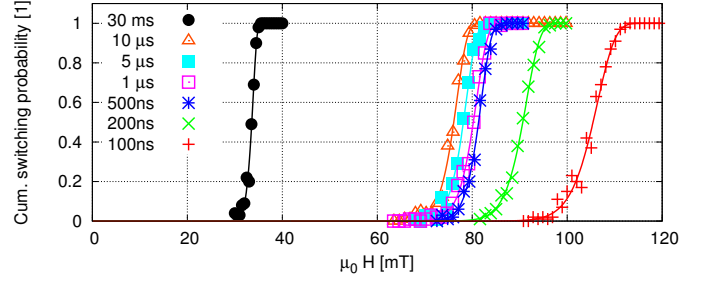
B. Sharrock formula

The switching *field* B_{sw} for various pulse times t_p can be expressed by the Sharrock equation [10]

$$B_{sw} = B_{s0} \left[1 - \left(\frac{k_B T}{E_0} ln\left(\frac{f_0 t_p}{ln(2)} \right) \right)^{1/2} \right] \qquad (3)$$

with the parameters as given in Eqn. (1) and (2). The Sharrock equation is used to describe the increase in the mean SF on time scales with possibly several orders of magnitude.

C. SFD measurements of Co/Pt magnets

In the following, the switching of a nanomagnet is analyzed by fitting the presented Arrhenius and Sharrock models to the measurement data. Fig. 4 shows the measured cumulative switching probability for off-chip generated field pulses with $t_p = 30$ ms and on-chip pulse times ranging from 100 ns $\leq t_p \leq 10$ µs. The measured values are fitted by Eqn. (1) with B_{s0} and E_0 as free parameters. The slopes of the cumulative switching probability are less steep for shorter pulse times (equivalent to a broadened SFD) and are asymmetric with the longer *tail* at lower fields. Table I summarizes the calculated fit-parameters for each pulse time t_p by the Arrhenius model. Even though the fitted curves reproduce the measured SFDs very well, the values for B_{s0} and E_0 are fluctuating. This is a strong hint, that the model can not fully describe the magnetic switching mode studied here.

For modeling the mean SF for various pulse times, the Sharrock equation (3) is fitted to the measured switching field B_{sw} and displayed by means of percentiles in Fig. 5, *'Measurement'*. The values for $t_p = 100$ ns are excluded for the fit, as at domain wall speeds of ≈ 20 m/s the DUT is not fully switched when nucleated in the second fraction of the pulse. The $t_p = 30$ ms pulses are excluded, as the field generation method is different: Additional in-plane fields due to inadequate adjustment of the external magnet cannot be excluded. This would lead to smaller switching fields during
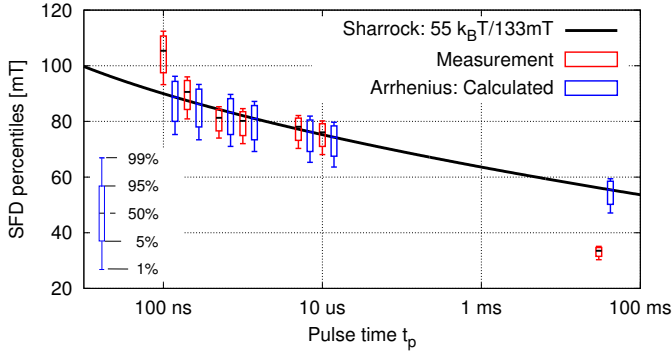
Fig. 5. Sharrock fit (black line) for the measured median SF of the DUT. Corresponding measured percentiles (red) and calculated (blue) percentiles reproduced by the Arrhenius model of the SFDs.

Fig. 6. On-chip clocking inductor. a) Close-up cross-section and b) top-view of the meander inductor.

coherent reversal of the ANC. However, it is obvious that the regions of interesting time-scales for pNML applications are exclusively in the (sub)-microsecond range and we restrict ourselves to most accurately model those by the fit.

For the DUT, the barrier and the switching field at zero temperature from the Sharrock-equation fit are determined to $E_0 = 55\,k_B T$ and $B_{s0} = 133\text{mT}$. The trend of an increased switching field at short time scales is obtained as expected. However, the Sharrock fitted values E_0 and B_{s0} differ from the Arrhenius-fitted values (see Tab. I, S-Fit column). By inserting the Sharrock fit values E_0 and B_{s0} into the Arrhenius equation (2), the width of the SFD can be compared with the measurements. For long pulses $t_p = 30$ ms the calculated SFD width is $\approx$ 2.5-times wider than the measured values as displayed in Fig. 5, 'Arrhenius: Calculated'. This pulse-time has been deliberately excluded from the Sharrock fit. It might be a hint, that the model is to simplistic to describe switching with many orders of magnitude varying time scales. More important, for short pulse-times which are interesting for NML applications, the SFDs are sufficiently reproduced by the Arrhenius model with fit-parameters taken from the Sharrock equation.

From the previous discussion the following guideline is given for efficient SFD modeling. First, the median values are determined by pulsed measurements at the application relevant timescale. Second, values for E_0 and B_{s0} are determined by a Sharrock fit and third, the SFD width is calculated by the Arrhenius model. Overall, the measurements and analytical modeling shows, that switching distributions are broadened at short time scales, demanding bigger margins in the pNML clocking window. The discussed measurement techniques and analytical models enable to identify prospective pNML films and devices.

V. ON-CHIP INDUCTOR DESIGN FOR pNML CIRCUITS

A magnetic power-clock, generated by on-chip inductors can be used to provide sufficient energy for Boolean operation of the magnets. In general, for on-chip inductors *inductance per area* and *quality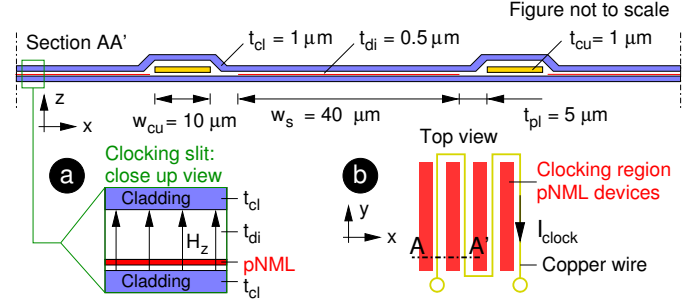 factor* are to be optimized [11]. By contrast, figure of merit for pNML clocking structures are *homogeneous field distributions* and *high field amplitudes*.

A. Assumptions for a realistic clock-field amplitude

The preceding sections showed that amplitudes $\mu_0 H_z \approx$ 100 mT would be necessary for clocking the pNML devices in the sub-microsecond range. However, this is almost impossible to achieve on large clocking regions and in anticipated applications, as planar air coils are very inefficient in field generation and available soft-magnetic cladding materials are limited by their saturation magnetization. Very recent measurements of our group on Co/Ni magnets show, that switching fields on sub-microsecond time-scales of $\mu_0 H_z < 25$ mT can be achieved. Hence, the following section discusses the design of an on-chip inductor and identifies the major loss mechanisms with the following assumptions: a clocking amplitude of $\mu_0 H_z \approx 20$ mT is targeted with emphasis on *low driving currents* for minimum power dissipation.

A possible geometry for efficient pNML clocking is shown in Fig. 6. Copper metalization lines with dimensions w_{cu} and t_{cu} are cladded by a soft-magnetic material of thickness t_{cl}. The pNML circuitry is directly fabricated on top of the lower cladding film, separated by thin dielectric material (Fig. 6a). After pNML fabrication, the copper metalization is processed. For electrical insulation, a dielectric planarizing layer of thickness t_{di} is deposited above the metalization lines, followed by the top magnetic cladding layer. Due to the high permeability of the soft-magnetic layers, magnetic flux is guided to the *slit*, where the pNML is exposed to a perpendicular field H_z. The copper metalization forms a meander pattern generating pNML clocking regions of equal size (Fig. 6b), typically tens of micrometer wide and several millimeters long.

B. Finite element simulation of the on-chip inductor

Time harmonic finite element simulations are performed with the 2D Maxwell solver FEMM [12]. In Fig. 7a, the B-H loops for three soft-magnetic cladding materials are plotted: SPy corresponds to *Supermalloy* as supported by [12]. NiFe and CoZrTa are described in [11] from which the material data are taken. The slope in the graph corresponds to the effective permeability, which is highest for SPy, moderate for NiFe and
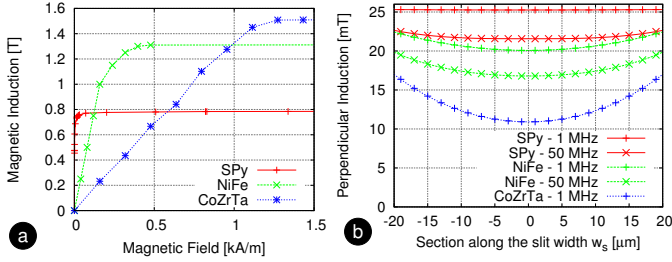
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Fig. 7. a) BH-loops for the soft-magnetic materials SPy, NiFe and CoZrTa. b) Perpendicular flux density across the 40μm wide pNML clocking region.
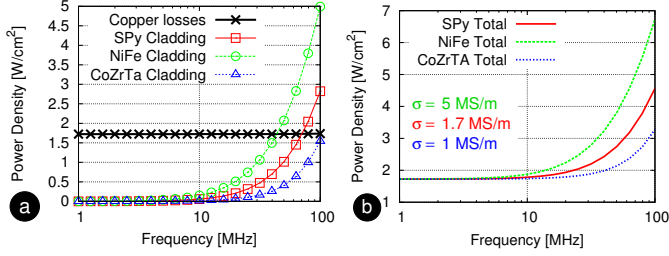

Fig. 8. a) Power dissipation due to losses in the Cu-metalization and cladding material. b) Total power dissipation over frequency.

lowest for CoZrTa. The generated magnetic flux density $\mu_0 H_z$ across the pNML-clocking region (x-direction in Fig. 6) for the three soft-magnetic materials is plotted in Fig. 7b. The field data are calculated for a current density of $j_{rms} = 2 \cdot 10^9$ A/m^2 at 1 MHz and 50 MHz. SPy with highest μ_r gives the most homogeneous spatial amplitude.

For power calculations, losses in the metalization (mainly resistive losses) and in the cladding (mainly hysteresis effects and Eddy-currents) are compared in Fig. 8a. Hysteresis losses are modeled by the loss tangent $tan\,\delta_\mu = \mu''/\mu'$. For CoZrTa, $tan\,\delta_\mu = 2 \cdot 10^{-9} \cdot f$, whereas for SPy and NiFe a value of $tan\,\delta_\mu = 2 \cdot 10^{-8} \cdot f$ is assumed [11]. For frequencies below 20 MHz, hysteresis and Eddy current losses in the cladding are negligible. For higher frequencies, CoZrTa shows minimal cladding losses as the films conductivity $\sigma_{CoZrTa} = 1$ MS/m and loss tangent are low. Simulations show, that highest μ_r at lowest cladding conductivity and low loss tangent are needed, in order to built a pNML power-clock inductor. A power loss density of $P \leq 3$ W/cm^{-2} at 50 MHz is feasible.

So far, the switching energy of the pNML magnets was excluded from loss calculations. The barrier between two states of a scaled Co/Pt magnet can be approximated to $\approx 100 \cdot k_B T$ (Sec. IV). This is a good estimate of the amount of energy dissipated during the switching process in the computing magnets. Power calculations for pNML devices results in $P_{loss} = 100 \cdot k_B T \cdot 2.5 \cdot 10^{10}$ cm$^{-2} \cdot 50$ MHz ≈ 0.5 W/cm^{-2} for a realistic scenario, where one magnet per NAND is switched in each clocking cycle. Assumptions are: NAND footprint (200 nm x 200 nm), 10 functional pNML layers, 50 MHz clocking frequency. This value is still a factor of 6 smaller than the power dissipated in the on-chip inductor.

It can be concluded, that SPy fulfills all demands for pNML clocking and results in a computing system, where binary throughputs of 1.25 GB ns^{-1}cm^{-2} at 2.8 aJ per NAND/NOR operation can be achieved. For comparison, the switching energy for Si-CMOS is 100 aJ at $\approx 30\%$ increased binary throughput [1].

VI. CONCLUSION

In this work, pNML Co/Pt magnets are characterized up to 10 MHz. It is found, that the measured SFDs can be described by an Arrhenius model. By measuring SFDs at application relevant frequencies, the SF is estimated by the Sharrock formula. Both, increased SFs and broadened SFDs at short time scales have to be taken into account for accurate pNML design.

Based on the presented measurements, an on-chip meander inductor design with ferromagnetic cladding for pNML clocking was presented. It allows for rectangular clocking regions of practical size. Three magnetic cladding materials were compared and an estimate for power consumption in a pNML system was given. The results show, that clocking of pNML devices in the MHz frequency range with on-chip inductors is feasible as soon as switching fields of the magnets can be reduced to $\mu_0 H_c \approx 20$ mT.

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