**Junzheng® T10**

Hardware Design Guide

### Version: 1.0

### Date: December 2015



**Junzheng T10**

**Hardware Design Guide**

Copyright © Ingenic Semiconductor Co. Ltd 2015. All rights reserved.

#### Release history

|  |  |  |  |
| --- | --- | --- | --- |
| **Date** | **Revision** |  | **Change** |
| 2015.12 | 1.0 | 1. First edition |  |

**Disclaimer**

This documentation is provided for use with Ingenic products. No license to Ingenic property rights is granted. Ingenic assumes no liability, provides Ingenic assumes no liability, provides no warranty either expressed or implied relating to the usage, or intellectual property right infringement except as provided for by Ingenic Terms and Conditions of Sale. No license to Ingenic property rights is granted.

Ingenic products are not designed for and should not be used in any medical or life sustaining or supporting equipment.

All information in this document should be treated as preliminary. Ingenic may make changes to this document without notice. Anyone relying on this documentation should contact Ingenic for the current documentation and errata. Anyone relying on this documentation should contact Ingenic for the current documentation and errata.

#### Hefei Junzheng Technology Co.

#### Address: 9/F, C3 Building, Innovation Industrial Park, No. 800 Wangxi Road, High-Tech Zone, Hefei, Anhui Province, China Postal Code: 230088

#### Tel: 86-10-68995472 Fax: 86-551-68998701

#### Website: Http:[//www.ingenic.com](http://www.ingenic.com/)

#### catalogs

1. [Schematic Design Considerations 1](#_TOC_250025)

[DDR2 1](#_TOC_250024)

[Power supply 1](#_TOC_250023)

[Clock 2](#_TOC_250022)

[JTAG Debug Interface 2](#_TOC_250021)

[DVP Interface 2](#_TOC_250020)

[USB OTG 3](#_TOC_250019)

[MAC Interface 3](#_TOC_250018)

[SFC Interface 3](#_TOC_250017)

[MSC Interface 3](#_TOC_250016)

[Audio Interface 3](#_TOC_250015)

[ADC Interface 3](#_TOC_250014)

[EFUSE Features 3](#_TOC_250013)

1. [PCB Design Considerations 4](#_TOC_250012)

[PCB stacking 4](#_TOC_250011)

[Layout Notes 4](#_TOC_250010)

[Setting of the perforation 4](#_TOC_250009)

[DDR Power and Ground Handling 4](#_TOC_250008)

[Setting of copper laying 4](#_TOC_250007)

[Thermal Design 4](#_TOC_250006)

[Design of other power supplies 5](#_TOC_250005)

[Clock Alignment 6](#_TOC_250004)

[USB cable routing 6](#_TOC_250003)

[Audio Alignment 6](#_TOC_250002)

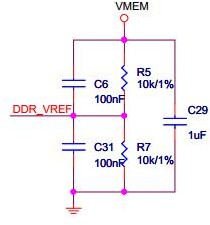
[DVP Alignment 6](#_TOC_250001)

[MAC Alignment 6](#_TOC_250000)

# Schematic Design Considerations

## DDR2

* 1. ZQ: Connect 240Ω 1% resistor to ground.
  2. VREF is a voltage divider, obtained from the VDDMEM divider with a 10K 1% divider resistor and 100nF decoupling capacitor.



## power supply

1. The high frequency impedance of the power supply is related to the inductance factor of the power supply. Add multi-stage capacitor filtering between VDDMEM, VDDCORE and ground, such as 10uF+0.1uF+0.01uF, to increase the filtering range of the capacitor and reduce the high-frequency impedance on the power supply.
2. If a module is not required in the product, the filter capacitors and beads for the power PIN can be omitted, but not the power supply.

Omitted.

3) Power supply division of T10

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Symbol | Description | Min | Typical | Max. | Unit |
| VDDMEM | VDDQ voltage for DDR PHY | 1.7 | 1.8 | 1.9 | V |
| DDRVDD | VDDQ and VDD voltage for DDR2 in T10 | 1.7 | 1.8 | 1.9 | V |
| VDDIO | IO digital power for GPIO power  domain | 3 | 3.3 | 3.6 | V |
| VDD\_DVP | IO digital power for DVP power  domain | 1.62 | 1.8 | 3.6 | V |
| VDD\_CORE | VDD core voltage | 0.99 | 1.1 | 1.21 | V |
| PLL\_AVDD | AVDPLL analog voltage | 1.08 | 1.1 | 1.32 | V |
| PLL\_AVDDHV | PLLAVDDHV analog voltage | 1.62 | 3.3 | 3.63 | V |
| VDDEFUSE | AVDEFUSE voltage | 2.25 | 2.5 | 2.75 | V |
| RTC\_VDD | VDDRTC11 voltage | 0.99 | 1.1 | 1.21 | V |
| RTC\_VDDIO | VDDRTC33 voltage | 1.8 | 3.3 | 3.6 | V |
| AVDOTG | AVDOTG33 voltage | 3.0 | 3.3 | 3.6 | V |
| ADC\_AVDD | ADC\_AVDD voltage | 3.0 | 3.3 | 3.6 | V |
| CODEC\_AVDD | CODEC\_AVDD voltage | 2.97 | 3.3 | 3.63 | V |

VDDCORE requires a power supply capability of not less than 1A, VDDMEM requires a power supply capability of not less than 1A; PLLAVDD and

PLLAVDDHV is isolated from other power supplies of the same level using a magnetic bead (1kΩ@100MHz).

T10's BOOT method

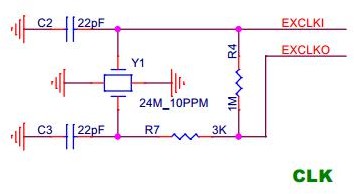
|  |  |  |
| --- | --- | --- |
| **BOOT\_SEL1** | **BOOT\_SEL0** | **Boot From** |
| 0 | 0 | MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B.)  MSC1 use GPIO Port C) |
| 0 | 1 | SFC boot @ CS4 (SPI boot @ SSI0) |
| 1 | 0 | NOR boot@ CS2 (just for FPGA testing) |
| 1 | 1 | USB boot@ USB 2.0 device, EXTCLK=24MHz |

Supports commonly used SFC boot, SD boot, and USB boot.

## clocks

T10 requires an external 24MHz operating clock with a maximum deviation of 30ppm. R9 needs to be soldered as a feedback resistor, otherwise the crystal will not work.

It may not oscillate, typical circuit is as follows:



The RTC clock requires a 32.768K clock circuit, and also requires a 10M ohm feedback between the two crystal pins.

resistor, otherwise the crystal may not oscillate.

## JTAG Debug Interface

T10 JTAG interface conforms to IEEE1149.1 standard, PC can be connected to ICE emulator through this interface. TCK, TRST are used as JTAG clock input and reset input respectively, and it is recommended to use single-board pull-down; TDI, TMS, TDO are used as data input, mode selection input and data output, and it is recommended to use single-board pull-up, and it is recommended to use 10K ohms for pull-down and pull-up resistors.

## DVP Interface

T10 supports 12-bit DVP interface, which is distributed in PA group PA00~PA22 of GPIO, and can be connected to different sensors according to the following ways:

1. When the sensor is a 10-bit DATA interface, it needs to be connected to PA00 to PA09 in order from low to high.
2. When the sensor is a 12-bit DATA interface, it needs to be connected to PA00 to PA11 in order from low to high.
3. When the sensor is a 12-bit DATA interface, only the high 10 bits of the sensor side are connected to PA00 to PA09 in order from low to high.

The PA00~PA22 GPIO power domain of T10 is VDDIO\_D, which supports IO voltages from 1.8V to 3.3V, and the rest of the PA group IO power domain is VDDIO. 1.8V needs to be supplied to VDDIO\_D when the VDDIO is 3.3V and the CMOS Sensor IO level is 1.8V. For the GPIO allocation of the DVP interface, please refer to the "T10 Software Coordination Design Conventions". T10 Hardware/Software Coordinated Design Specification Conventions.

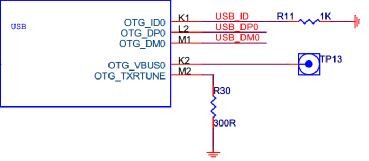
It is worth noting that the IO drive capability of CMOS sensors from different manufacturers varies, so pay attention to whether the DVP interface is reserved or not when designing.

Resistive-capacitive matching devices.

## USB OTG

When configured in OTG\_HOST mode, the USB\_ID pin needs to be grounded and the OTG\_VBUS pin is reserved for the measurement point, as follows

Shown:



If USB is only used in DEVICE mode, the USB\_ID pin needs to be pulled high and the VBUS pin can be left empty.

M2 pin OTG\_TXRTUNE with 300 ohm 1% resistor to ground, otherwise OTG HOST port when connected to USB WIFI.

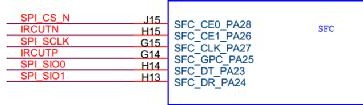
The MTK 7601 module has an abnormal function.

## MAC Interface

The T10 MAC interface supports 10/100M RMII mode; the 50Mhz clock required for RMII mode can be output through the P10 pin of the T10; MDIO requires a pull-up resistor; 33 ohm resistors are recommended to be connected in series with MDCK, TXCK, TXD0, TXD1, and RXCK, RXD0, and RXD1 signals at the source side to obtain better signal quality. The following are some examples of the signals that can be used in this application.

## SFC Interface

The SFC interface of T10 is located in PA23~PA28, this interface can be connected to SPI NOR FLASH, the connection method is as follows:



## MSC Interface

T10 supports two MSC interfaces, if external TF card is connected, MSC0 of PB group is used; if external SDIO WIFI module is connected, MSC0 of PB group is used; if external SDIO WIFI module is connected, MSC0 of PB group is used.

Use the PC Group MSC1 interface.

## Audio interface

The T10 audio section supports 1 analog input and 1 analog output; the analog input supports differential mode and single-ended mode, when using single-ended mode, the analog input is connected to the MICN pin.

## ADC Interface

The T10 supports two 12-bit resolution ADC interfaces with a reference voltage of ADC\_VREF.

## EFUSE Function

In burn-in mode, a voltage of 2.5V+/-10% needs to be supplied to the AVDEFUSE pin, and the burn-in time must not exceed 1s;

In read mode, the voltage of AVDEFUSE is 0V or suspended.

# PCB Design Considerations

## PCB stacks

The T10 is a 0.65 pitch, 181-pin BGA package. PCB stacking can be designed in a 4-layer structure with the stacking layer setup as follows

TOP-GND-VCC-BOTTOM. the TOP layer is referenced to L2 and the BOTTOM layer is referenced to L3. the stacked layer structure is shown below:

|  |  |  |
| --- | --- | --- |
| floor (of a building) |  | thicknesses |
| TOP | ================================== | 1Oz |
|  | PP | 3(mil) |
| L2 | ================================== | 1Oz |
|  | Core | Adjustment to plate thickness |
| L3 | ================================== | 1Oz |
|  | PP | 3(mil) |
| BOT | ================================== | 1Oz |

## Layout Considerations

* 1. Meet SMT process requirements.
  2. Keep heat-sensitive devices as far away as possible, e.g., the CPU should be placed as far away as possible from the CMOS Sensor.
  3. Note the location of structural height limits.

## Setting of the over-hole

1. Normal via holes are 8 mil aperture, 16 mil outer ring.
2. Ground and electrical perforations utilize a 12 mil aperture with a 24 mil outer ring.
3. The CPU and DDR part of the vias should be arranged in a reasonable way, and the spacing should preferably not be less than 30 mils, so as not to break the circuit of the ground and the electrical layer.

## DDR Power and Ground Handling

On the backside of CPU and DDR, it is better to place a decoupling capacitor corresponding to each power supply PIN, and the vias should be placed next to the pins, and the wires should be as thick and short as possible to avoid increasing the inductance of the wires, and the planes of VDDMEM and DDRVDD must ensure the actual width of the wires. When switching layers, make as many holes as possible to avoid becoming the bottleneck of the whole plane. It is recommended that the POWER layer be set to Split/Mixed, and the wire width of the copper layer should be as small as possible (e.g., 2 mils), so that the copper layer can be used for better results.

Crosstalk is fundamentally dependent on the PCB stack and the minimum line spacing. The best way to avoid crosstalk is to ensure that the signal has a very good return path. Each signal layer should be close to a complete ground plane to provide the shortest return path. It is very important that the ground plane is complete in order to maintain consistent characteristic impedance and that the ground plane cannot be interrupted. After traveling the signal lines, the remaining space must be filled with GND and the copper laying line width is as small as possible, which can be used to better effect.

VREF is the reference for the DDR input buffer. the VREF divider circuit should be located as close to the chip as possible, and the alignment should be as short as possible, with a recommended line width of 20 mils.

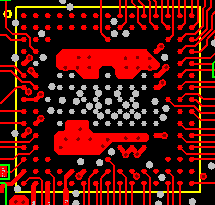
And keep a distance of more than 3W from other data lines to ensure that there is no interference, and add a 0.01uF capacitor near the VREF PIN pin.

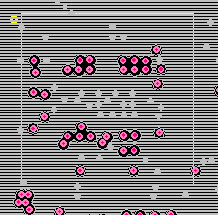
## Setting of copper laying

1. The safe spacing between the overbore and the copper spread is 6 mil.
2. The copper laying line width is set to 2 mil for the ground and electrical layers, and can be set to 4 mil for the other layers.

## Thermal Design

1. CuPt thickness of 1OZ is recommended to improve the heat dissipation of the PCB.
2. Once the CPU outlets are complete, drill as many ground holes as possible without compromising the integrity of the power plane, as shown below:



1. The ground must be complete, and the ground inside the CPU can have multiple pathways to the outside of the CPU.
2. The high-current alignment should be as short as possible, try to lay copper design to widen the alignment width, while the thickness of the layer is required to be more than 1OZ, for the inner layer of the alignment, it should be arranged in the adjacent layer of the ground layer.
3. The PCB board edge is surrounded by ground holes (through holes) and exposed copper, which is favorable to the metal grounding of the shell and ESD, and is also good for heat dissipation.
4. In the layout, the CPU and other heat-generating devices separated by a certain width (at least 20mm), the use of shell openings (such as thermal windows, large connector openings, etc.) so that the most heat-generating devices placed in the vicinity of a straight line (the CPU can be arranged in this way). For several heat-generating devices, cross-layout, not rows and columns of layout.

## Design of other power supplies

1. The power supply chip should be laid out as close to the CPU as possible.
2. The layout of the power supply chip must pay attention to the location of the DC/DC input and output capacitors, and the input and output capacitors should be as close as possible.

DC/DC PIN pins and make sure that the distance between their ground and the CPU ground is as short as possible.

1. CPU VDDCORE, VDDMEM, VDDPLL, VDDIO, etc. filter capacitors should be placed as close as possible to the CPU PIN.

The feet are in position.

1. VDDCORE, VDDMEM, VDDIO To lay copper on the power supply layer without using the wire routing method.
2. Power supply layer changeover are punched with as many over-holes as possible to avoid becoming a bottleneck in the transmission of power signals.
3. CPU related capacitor layout:

Priority 1: PLLAVDD, PLLAVDDHV, VDDCORE, VDDMEM, DDRVDD, VREF, VDDIO.

Priority 2: ADC\_AVDD, AVDOTG33, CODEC\_AVDD, VDDIO\_D.

Priority 3: VDDRTC, VDDEFUSE.

1. Ensure the integrity and continuity of the copper (ground and power) underneath the CPU to provide a good signal return path.

Improve the quality of signal transmission, improve the stability of the product; also can improve the performance of heat dissipation.

1. All grounding pads are to be perforated close to the grounding layer.

## Clock alignment

It is recommended that the whole board clock alignment is recommended to wrap the top and bottom of the ground, and other signals to maintain the principle of 3W, and string matching resistors to get a better signal quality.

## USB alignment

To ensure good signal quality, the USB 2.0 port data signal lines are routed according to the differential line method. In order to achieve USB 2.0 high

With a speed requirement of 480MHz, the following principles are recommended for PCB wiring design:

1. Differential data line alignment as short as possible, straight, differential data line to the inner alignment length is strictly equal length, alignment length deviation control in ±

Within 5 mil.

1. Differential data line control Uniform differential impedance of 90Ω±10%.
2. Differential data cable routing should be routed in the wiring layer adjacent to the ground plane whenever possible and without changing layers.
3. Differential data line alignments should have a complete ground plane layer as a reference plane and should not be split across planes.
4. Differential data cable alignments should be routed with the least number of vias and corners possible. Corners may be considered rounded or 135-degree angles, avoiding right angles to minimize reflections and impedance variations.
5. Avoid proximity to other high-speed cyclic signals and high-current signals and ensure spacing greater than 50 mils to minimize crosstalk. In addition

Keep away from low-speed non-periodic signals, ensuring a distance of at least 20 mils.

1. The REXT resistor should be as close to the T10 side as possible.

## Audio Alignment

The audio section should be routed with separate input and output routes, and the MICP/MICN should be routed differentially. And avoid other signal

Interference.

## DVP alignment

Data and clock line alignment length deviation is controlled within ±300 mil; DVP\_MCLK, DVP\_PCLK, DVP\_HSYNC,

The DVP\_VSYNC alignment should be spaced apart from other alignments to meet the 3W requirement to avoid crosstalk.

## MAC alignment

Due to the high GMAC signal rate, the following principles are recommended for PCB wiring design to minimize crosstalk between bus signals:

1. Avoid signal alignments that cross power split areas and keep signal reference planes intact.
2. The signal line length is based on the clock line, and the deviation of the alignment length is controlled within ±200mil.
3. The ground directly under the transformer chip needs to be excavated and treated.
4. Maintain the "3W" principle for the spacing of neighboring signal alignments.
5. It is recommended to connect a 33Ω resistor in series with the clock signal for better signal quality.

MDI\_TP, MDI\_TN, MDI\_RP, MDI\_RN differential pairs at the PHY side should be as equal as possible, and the deviation of the alignment length should be controlled within ±5mil.

The differential impedance is controlled within 100Ω±10%.