```
$date
     Sun Aug 21 20:24:04 2022
$end
$version
     Icarus Verilog
$end
$timescale
     1s
$end
$scope module adder_tb $end
$var wire 4 ! Sum [3:0] $end
$var wire 1 " Cout $end
$var reg 4 # A [3:0] $end
$var reg 4 $ B [3:0] $end
$var reg 1 % Cin $end
$scope module uut $end
$var wire 4 & A [3:0] $end
$var wire 4 ' B [3:0] $end
$var wire 1 % Cin $end
$var wire 1 ( c3 $end
$var wire 1 ) c2 $end
$var wire 1 * c1 $end
$var wire 4 + Sum [3:0] $end
$var wire 1 " Cout $end
$scope module FA1 $end
$var wire 1 , A $end
$var wire 1 - B $end
$var wire 1 % Cin $end
$var wire 1 * Cout $end
$var wire 1 . s1 $end
$var wire 1 / c2 $end
$var wire 1 0 c1 $end
$var wire 1 1 S $end
$scope module HA1 $end
$var wire 1 , A $end
$var wire 1 - B $end
$var wire 1 0 C $end
$var wire 1 . S $end
$upscope $end
$scope module HA2 $end
$var wire 1 . A $end
$var wire 1 % B $end
$var wire 1 / C $end
$var wire 1 1 S $end
$upscope $end
$upscope $end
$scope module FA2 $end
```

```
$var wire 1 2 A $end
$var wire 1 3 B $end
$var wire 1 * Cin $end
$var wire 1 ) Cout $end
$var wire 1 4 s1 $end
$var wire 1 5 c2 $end
$var wire 1 6 c1 $end
$var wire 1 7 S $end
$scope module HA1 $end
$var wire 1 2 A $end
$var wire 1 3 B $end
$var wire 1 6 C $end
$var wire 1 4 S $end
$upscope $end
$scope module HA2 $end
$var wire 1 4 A $end
$var wire 1 * B $end
$var wire 1 5 C $end
$var wire 1 7 S $end
$upscope $end
$upscope $end
$scope module FA3 $end
$var wire 1 8 A $end
$var wire 1 9 B $end
$var wire 1 ) Cin $end
$var wire 1 ( Cout $end
$var wire 1 : s1 $end
$var wire 1 ; c2 $end
$var wire 1 < c1 $end
$var wire 1 = S $end
$scope module HA1 $end
$var wire 1 8 A $end
$var wire 1 9 B $end
$var wire 1 < C $end
$var wire 1 : S $end
$upscope $end
$scope module HA2 $end
$var wire 1 : A $end
$var wire 1 ) B $end
$var wire 1 ; C $end
$var wire 1 = S $end
$upscope $end
$upscope $end
$scope module FA4 $end
$var wire 1 > A $end
$var wire 1 ? B $end
$var wire 1 ( Cin $end
```

```
$var wire 1 " Cout $end
$var wire 1 @ s1 $end
$var wire 1 A c2 $end
$var wire 1 B c1 $end
$var wire 1 C S $end
$scope module HA1 $end
$var wire 1 > A $end
$var wire 1 ? B $end
$var wire 1 B C $end
$var wire 1 @ S $end
$upscope $end
$scope module HA2 $end
$var wire 1 @ A $end
$var wire 1 ( B $end
$var wire 1 A C $end
$var wire 1 C S $end
$upscope $end
$upscope $end
$upscope $end
$upscope $end
$enddefinitions $end
#0
$dumpvars
0C
0B
0A
0@
0?
0>
0=
0<
0;
0:
09
08
07
06
05
04
03
02
01
00
0/
0.
0-
0,
```

```
b0 +
0*
0)
0(
b0 '
b0 &
0%
b0 $
b0 #
0"
b0 !
$end
#100
b1 !
b1 +
11
1.
1,
b1 #
b1 &
#110
1=
1)
b1101 !
b1101 +
1C
16
1@
1-
13
0,
12
1>
b11 $
b11 '
b1010 #
b1010 &
#120
1(
1C
1"
15
1)
0=
1;
1*
0@
```

```
1B
14
06
1:
b1000 !
b1000 +
01
1/
0-
1?
1,
02
18
1%
b1010 $
b1010 '
b1101 #
b1101 &
```