

Micro Commercial Components 20736 Marilla Street Chatsworth

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SI2302

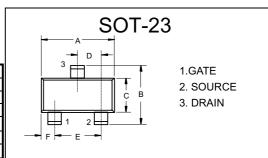
Features

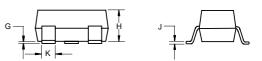
- 20V,3.0A, $R_{DS(ON)}$ =55m Ω @ V_{GS} =4.5V $R_{DS(ON)}$ =82m Ω @ V_{GS} =2.5V
- High dense cell design for extremely low R_{DS(ON)}
- Rugged and reliable
- Lead free product is acquired
- SOT-23 Package Marking Code: S2
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0

Maximum Ratings @ 25°C Unless Otherwise Specified

Symbol	Parameter	Rating	Unit	
V_{DS}	Drain-source Voltage	20	V	
I_D	Drain Current-Continuous	3	Α	
I _{DM}	Drain Current-Pulsed ^a	10	Α	
V_{GS}	Gate-source Voltage	±8	V	
P _D	Total Power Dissipation	1.25	W	
R _{+JA}	Thermal Resistance Junction to Ambient ^b	100	°C/W	
TJ	Operating Junction Temperature	-55 to +150	$^{\circ}$	
T _{STG}	Storage Temperature	-55 to +150	$^{\circ}\!\mathbb{C}$	

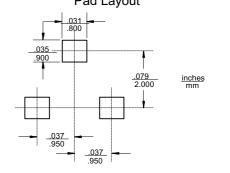
N-Channel Enhancement Mode Field Effect Transistor



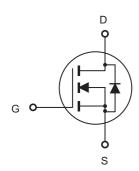


DIMENSIONS					
	INCHES		ММ		
DIM	MIN	MAX	MIN	MAX	NOTE
Α	.110	.120	2.80	3.04	
В	.083	.098	2.10	2.64	
С	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
Е	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
Н	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	015	020	37	51	

Suggested Solder Pad Layout



Internal Block Diagram





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$\textbf{Electrical Characteristics} \quad \textbf{T}_{A} = 25^{\circ} \textbf{C} \text{ unless otherwise noted}$

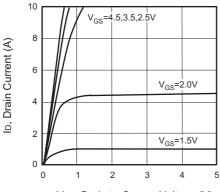
Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Off Characteristics	•					
Drain-Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0V, I_{D} = 10\mu A$	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I _{GSSF}	$V_{GS} = 8V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	Igssr	V_{GS} = -8V, V_{DS} = 0V			-100	nA
On Characteristics °						
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}$, $I_D = 50\mu A$	0.65		1.2	V
Static Drain-Source		$V_{GS} = 4.5V, I_D = 3.6A$		55	72	mΩ
On-Resistance	R _{DS(on)}	$V_{GS} = 2.5V, I_D = 3.1A$		82	110	mΩ
Forwand Transconductance	9 _{FS}	$V_{DS} = 5V, I_{D} = 3.6A$		8.5		S
Dynamic Characteristics d						
Input Capacitance	C _{iss}			237		pF
Output Capacitance	C _{oss}	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1.0 MHz		120		pF
Reverse Transfer Capacitance	C _{rss}	1		45		pF
Switching Characteristics d						
Turn-On Delay Time	t _{d(on)}			23	45	ns
Turn-On Rise Time	t _r	$V_{DD} = 10V, I_D = 3.6A,$		11	30	ns
Turn-Off Delay Time	t _{d(off)}	$V_{GS} = 4.5V, R_{GEN} = 6\Omega$		34	70	ns
Turn-On Fall Time	t _f			36	70	ns
Total Gate Charge	Qg	\/ 40\/ L 0.0A		6	10	nC
Gate-Source Charge	Q _{gs}	$V_{DS} = 10V, I_{D} = 3.6A,$ $V_{GS} = 4.5V$		1.4		nC
Gate-Drain Charge	Q _{gd}	- GS 1.0 V		1.8		nC
Drain-Source Diode Characteristics ar	Drain-Source Diode Characteristics and Maximun Ratings					
Drain-Source Diode Forward Current b	I _S				0.94	Α
Drain-Source Diode Forward Voltage c	V _{SD}	$V_{GS} = 0V, I_{S} = 0.94A$			1.2	V

Notes:

a.Repetitive Rating: Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.



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VDS, Drain-to-Source Voltage (V)

Figure 1. Output Characteristics

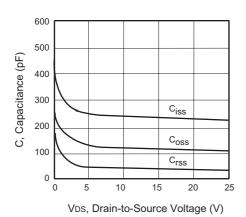


Figure 3. Capacitance

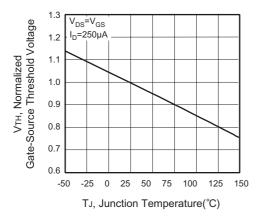


Figure 5. Gate Threshold Variation with Temperature

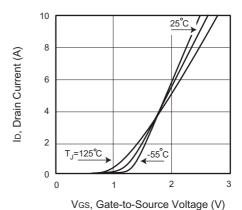


Figure 2. Transfer Characteristics

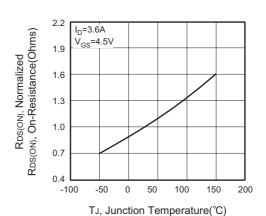
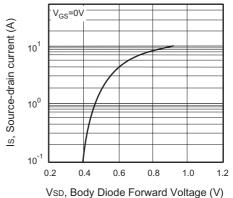


Figure 4. On-Resistance Variation with Temperature





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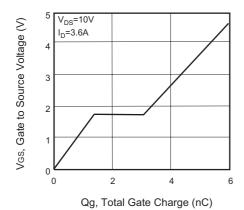


Figure 7. Gate Charge

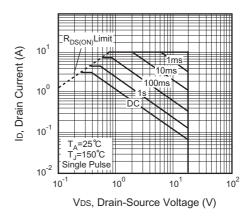


Figure 8. Maximum Safe Operating Area

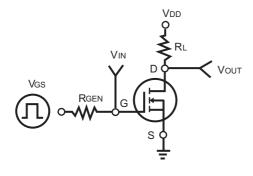


Figure 9. Switching Test Circuit

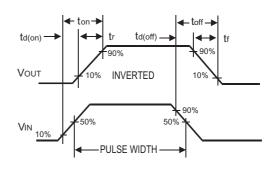


Figure 10. Switching Waveforms

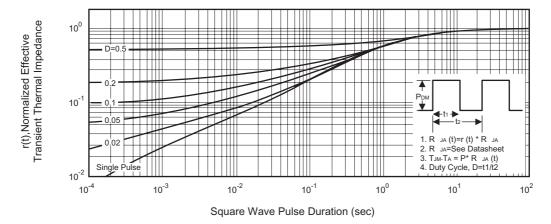


Figure 11. Normalized Thermal Transient Impedance Curve



Ordering Information

Device	Packing
(Part Number)-TP	Tape&Reel3Kpcs/Reel

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