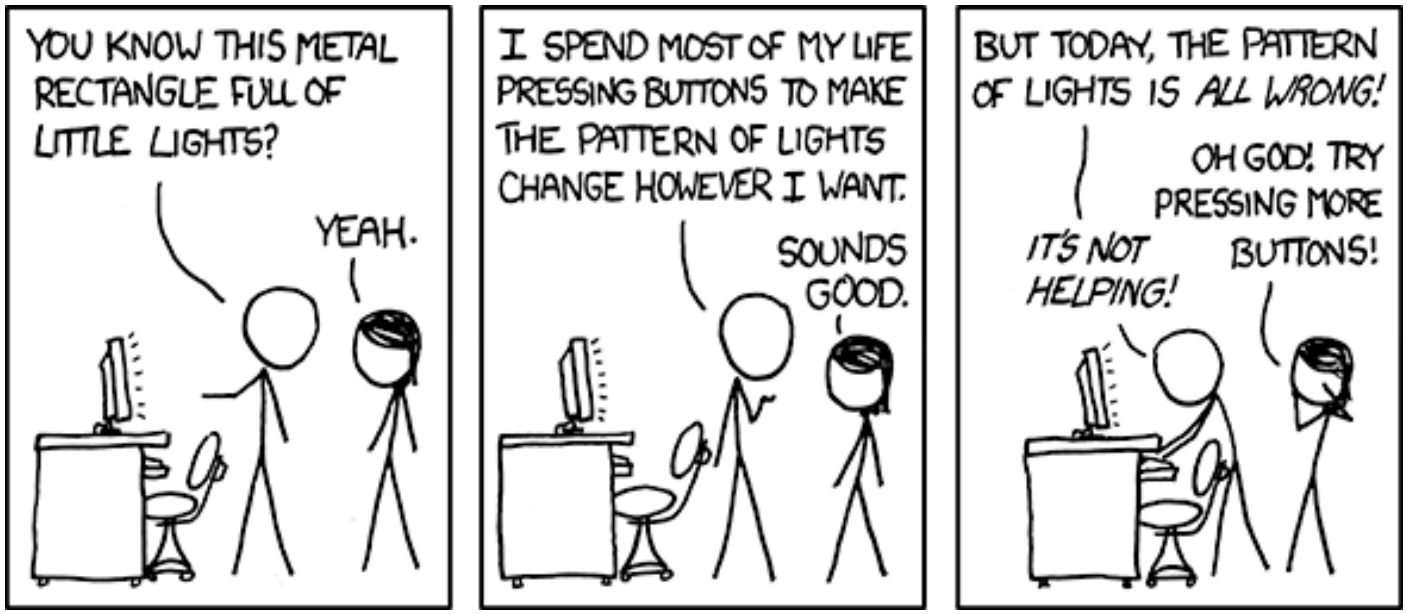
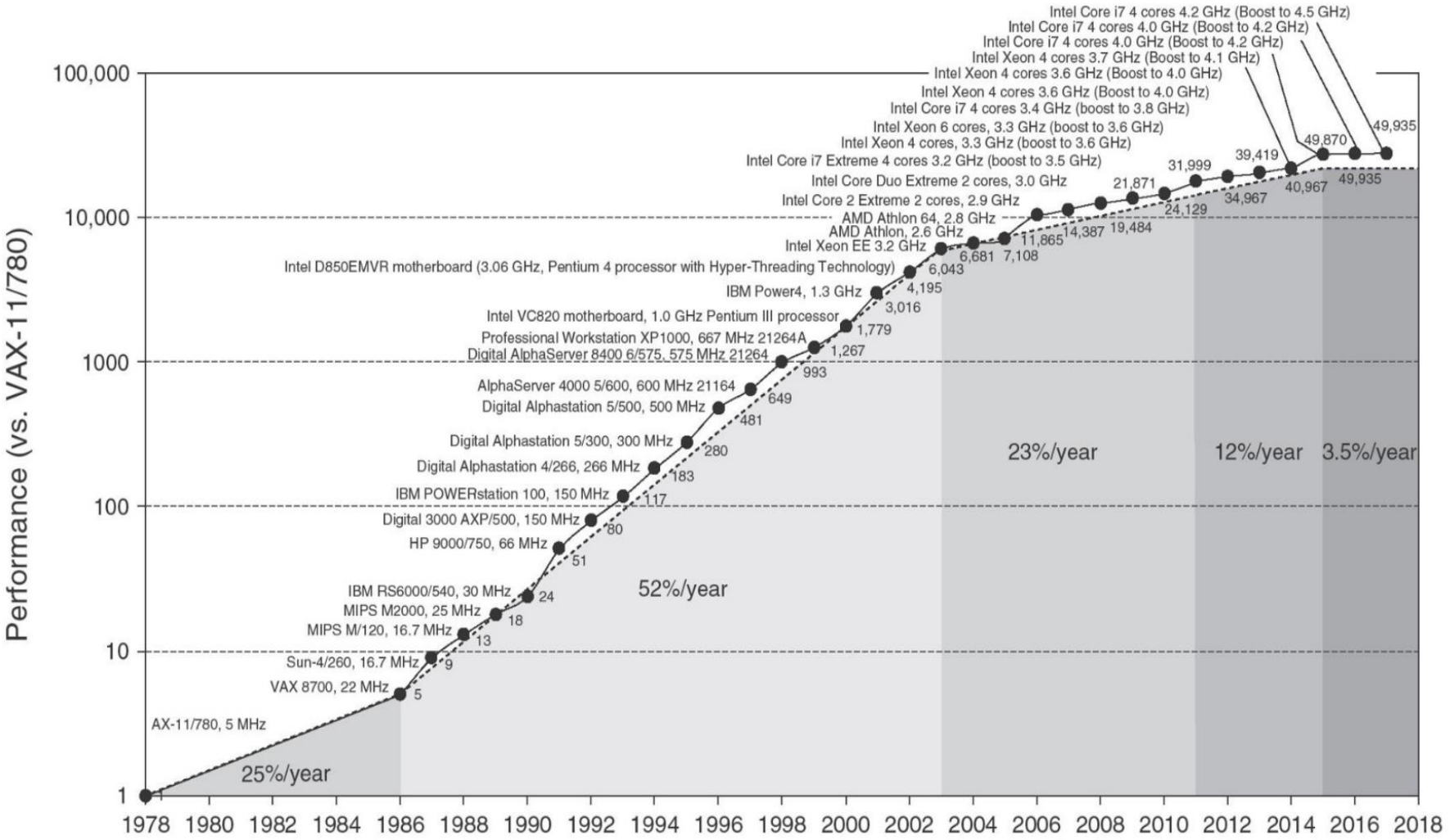
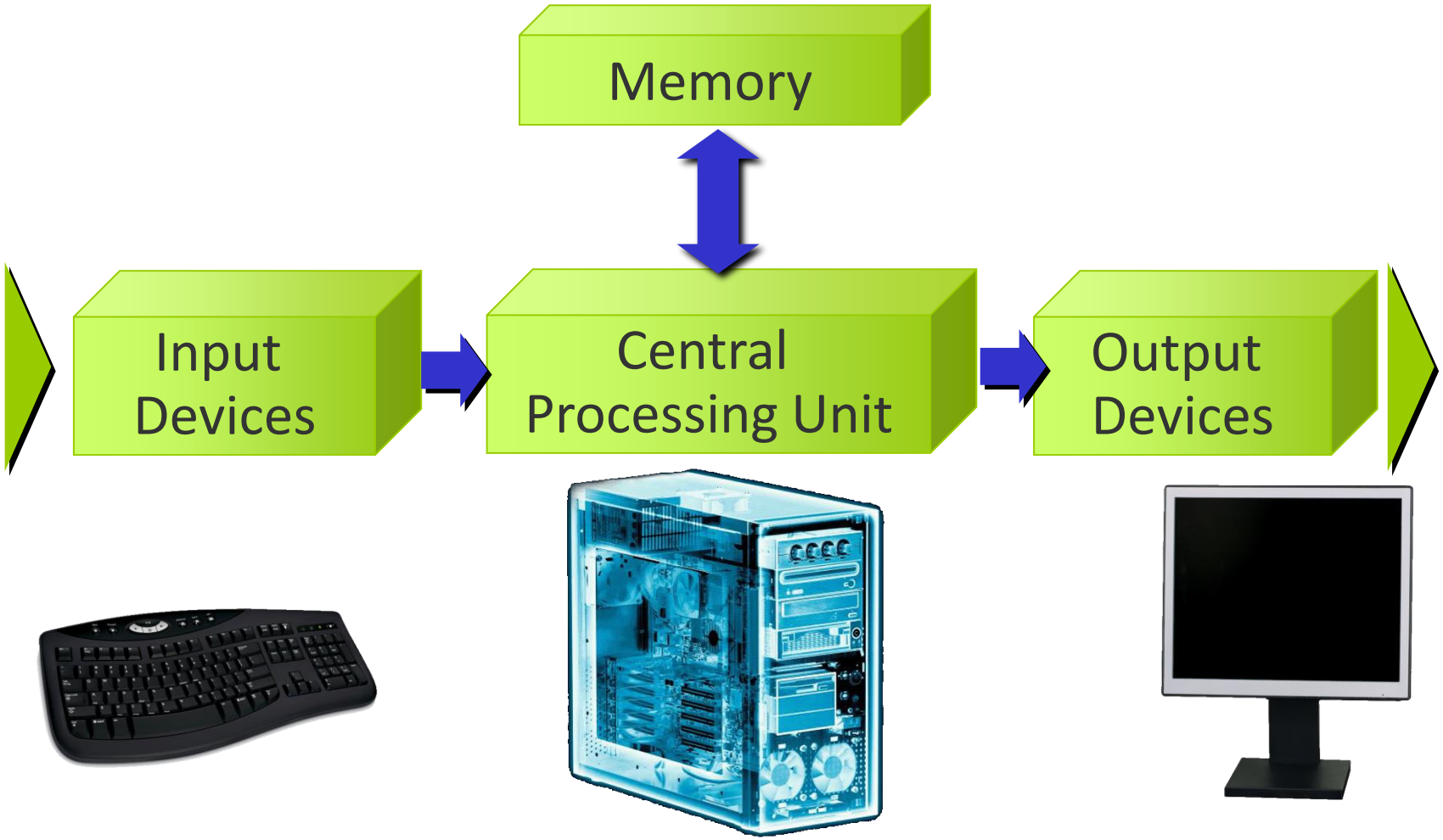
Computer Architecture



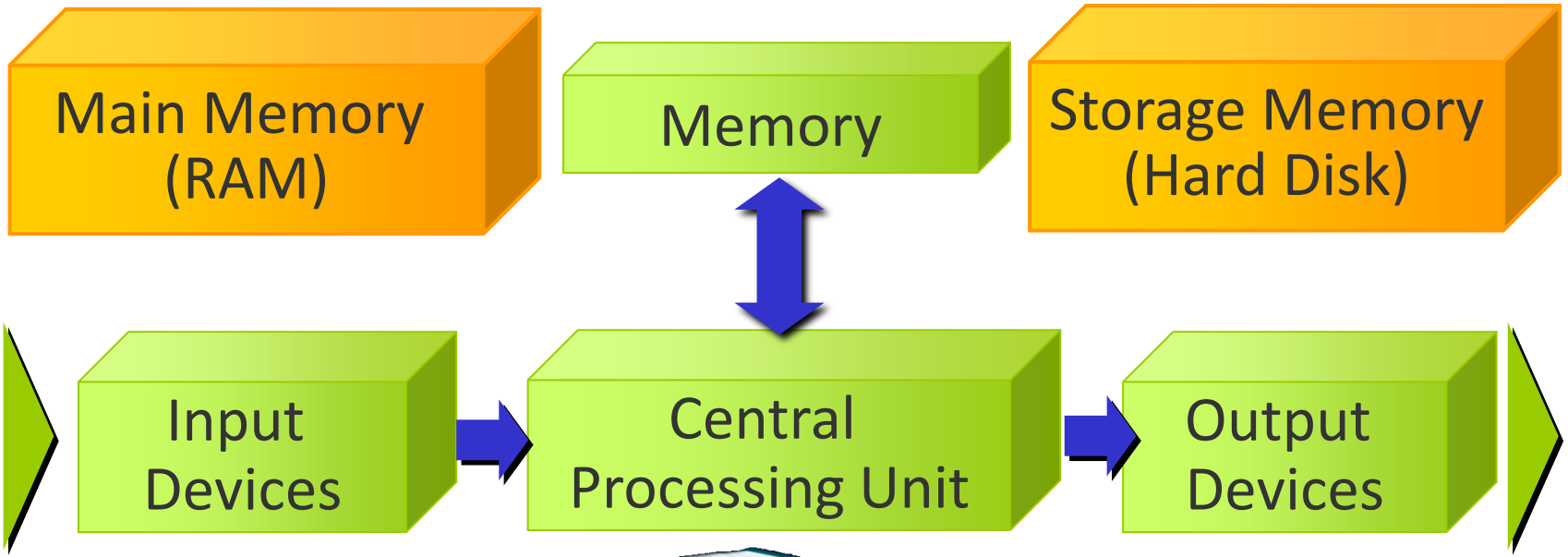
Microprocessor performance growth



Components of a computer system

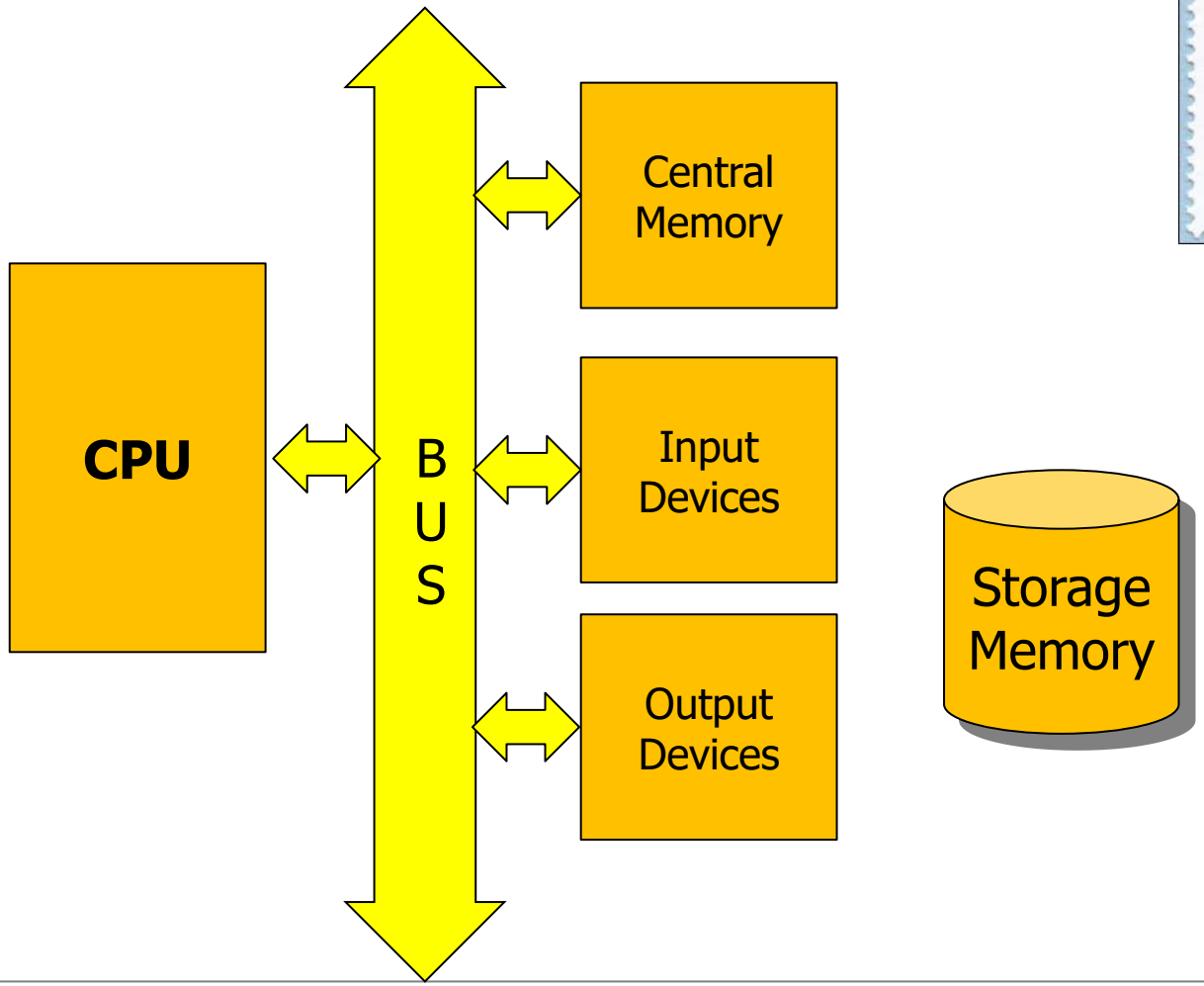


Components of a computer system



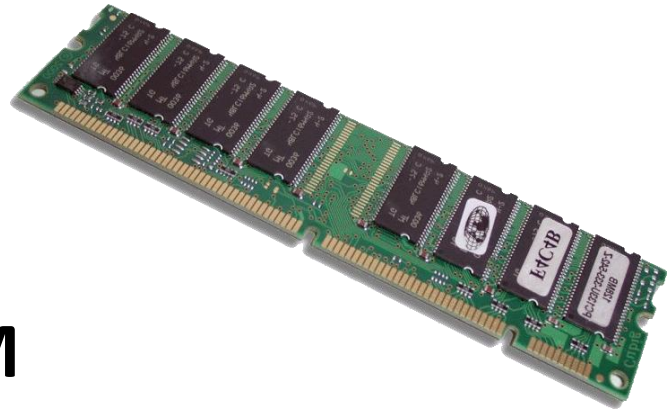
Computer Architecture

- Von Neumann Architeture



Fundamental components

Microprocessor core



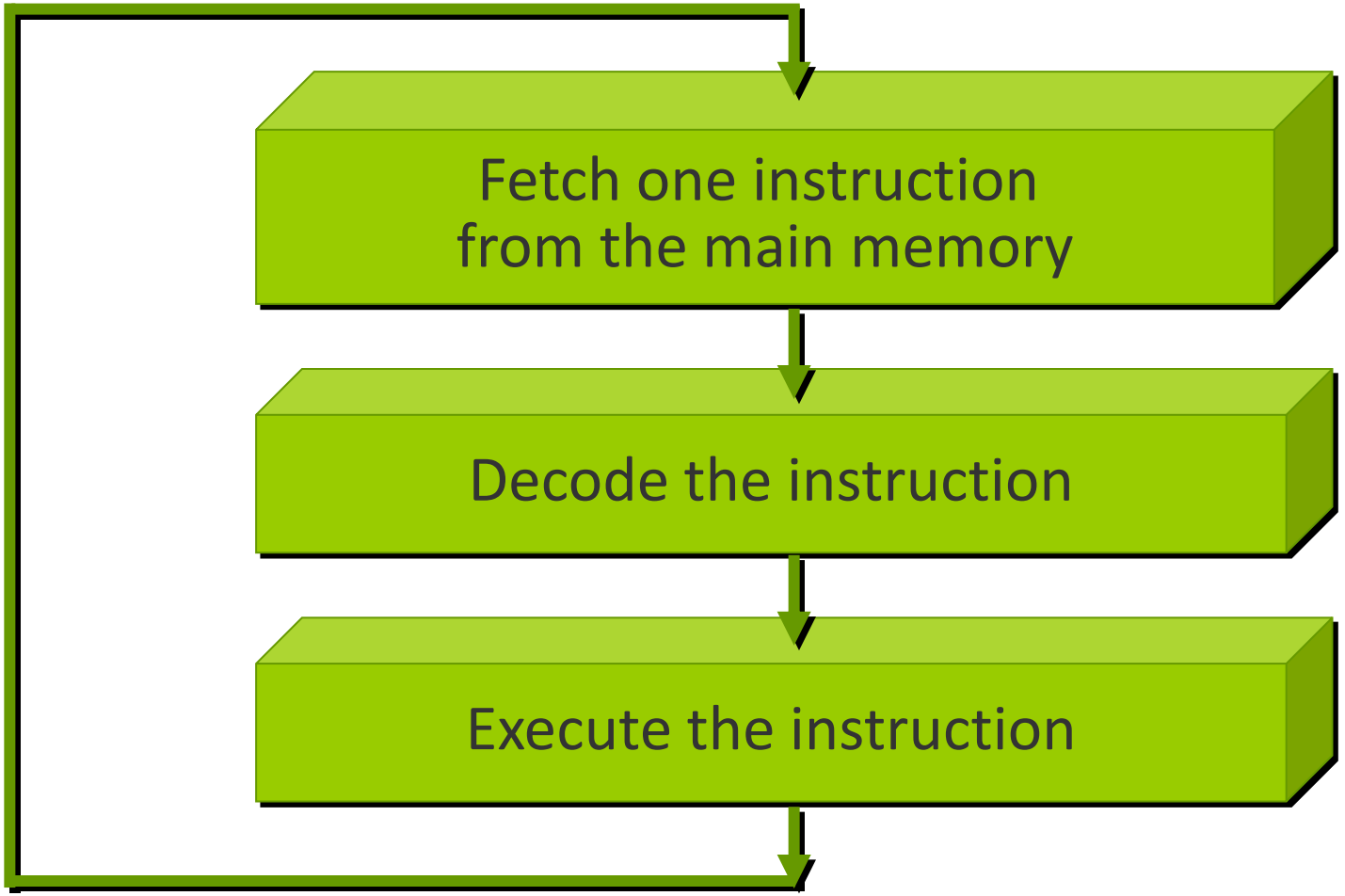
Main Memory - RAM

Microprocessor core

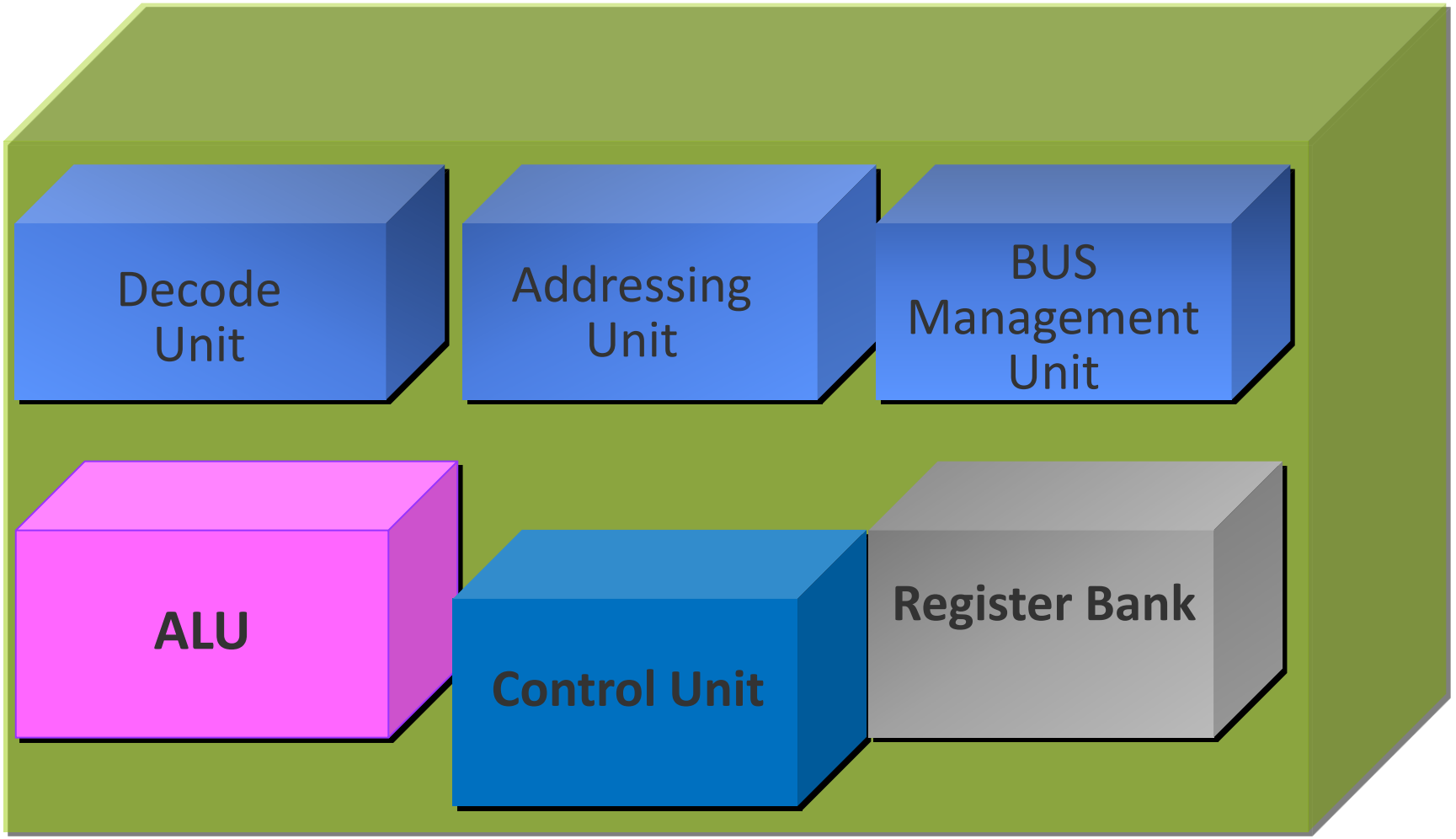
- A microprocessor core (usually called µP) incorporates in a single chip the functions of a computer's "central processing unit (CPU)".

The number of ants in the world is about 1 quadrillion ($1x10^{15}$).
Today one processor core may contain 1,000,000,000 ($1x10^{9}$) transistors.
Every year, more than 1 billion microprocessors are sold in the world.
By 2015 the number of transistors is about 1,200 quintillion ($1x10^{18}$).

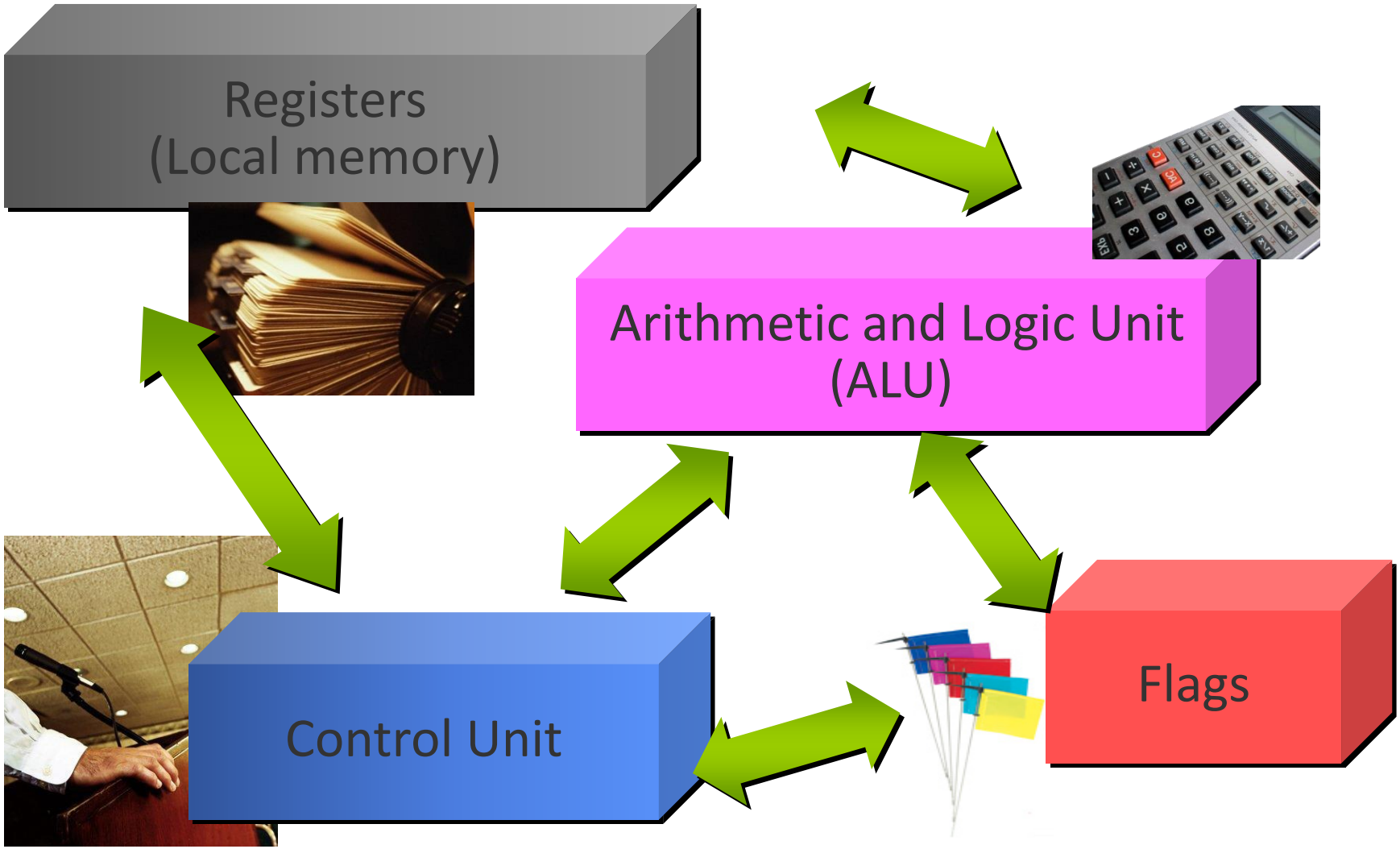
Computer Instruction Cycle



CPU (Central Processing Unit)



CPU (Central Processing Unit) – cont.



Central Processing Unit

- It performs all the required elaborations (arithmetic, logic, graphic, ...).
- It is composed by:
  - Registers
  - ALU
  - Control
  - Flags

Registers

- Local memory elements used for storing data temporally (ex. Partial results).
- Small number (8...128)
- word dimension (8...64 bit)

BIT (BInary digiT)

BYTE = eight bits

WORD = n bytes

ALU (Arithmetic-Logic Unit)

- It performs all the arithmetic and logic computations
  - It is devised to compute Integer values or Real values
  - The set of possible operations depend on the processor architecture
- It is usually composed by combinational circuits.

Control Unit

It is the computer heart:

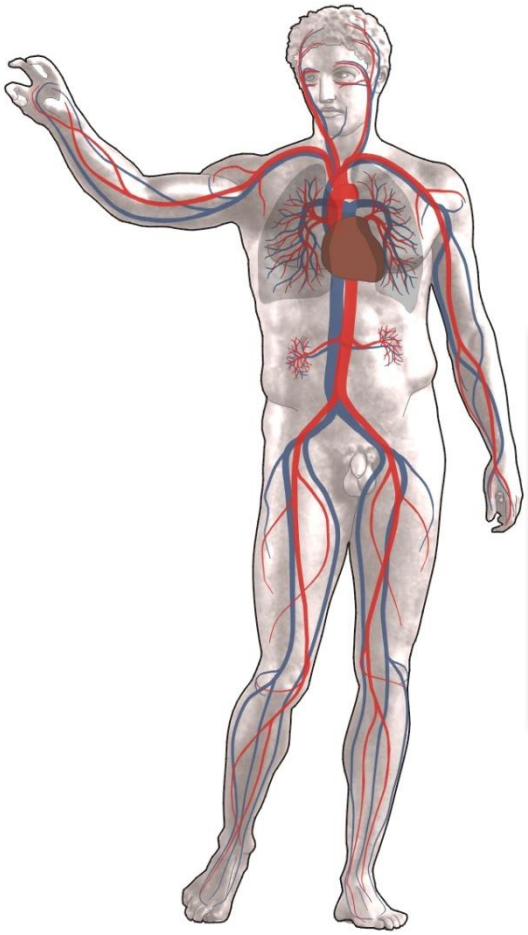
- According to the provided program...
- And the state of all the units...
- Schedules the operations to be executed...
- And issues the corresponding instructions.

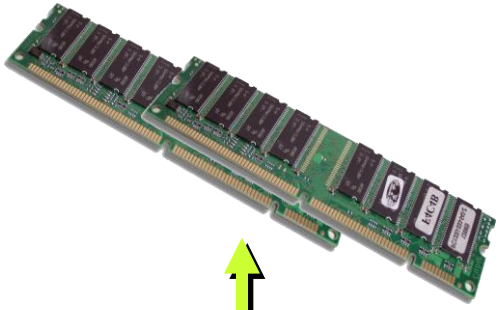
Flag

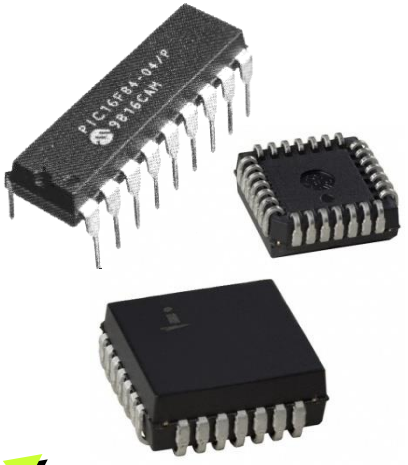
- State indicator of the ALU operation result
- single bit (0=false, 1=true)
- usually grouped into a register
- Most common flags:

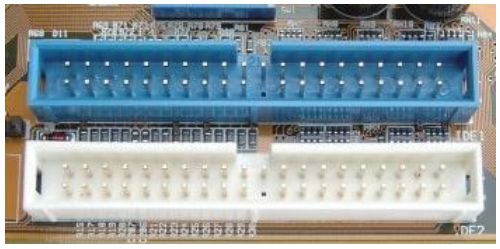
Z (zero)	V (overflow)
CY (carry)	N (negative)

System Bus (PC Circulatory system)







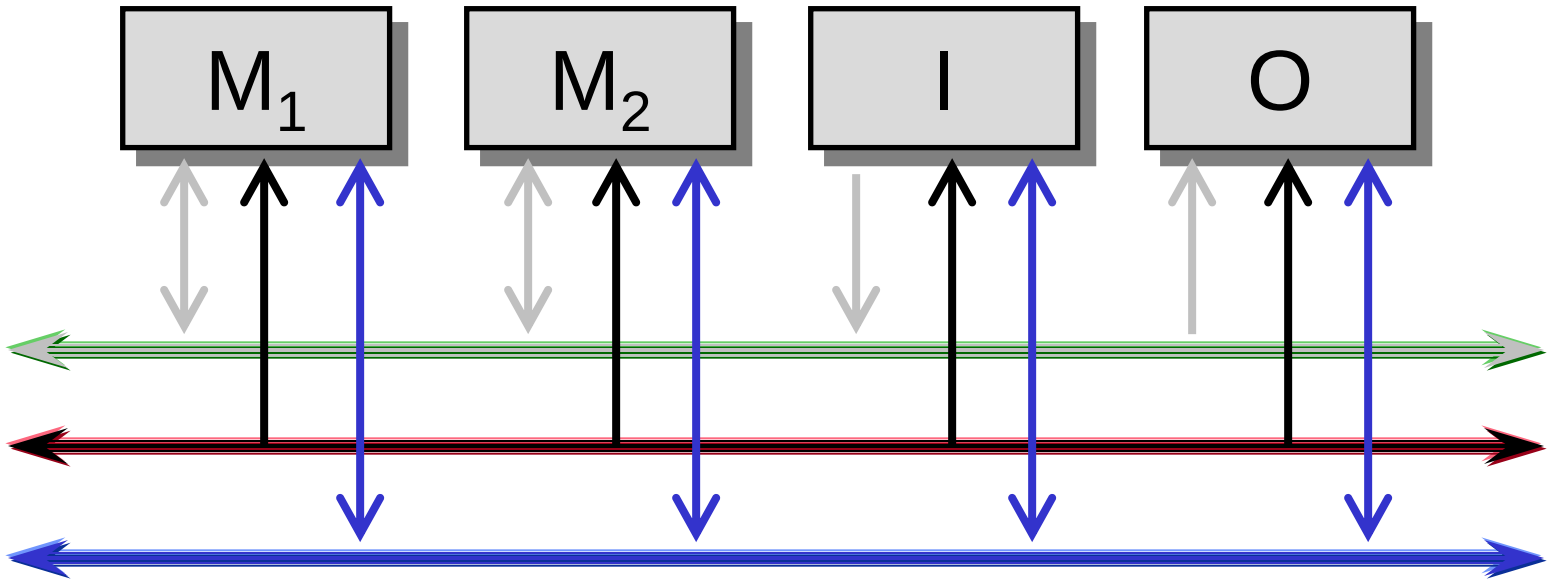


Bus features

- A single data is transported at a time
- frequency = number of data transported in one second
- Width = number of bit composing a single data
- If not properly dimensioned, it could be a bottleneck

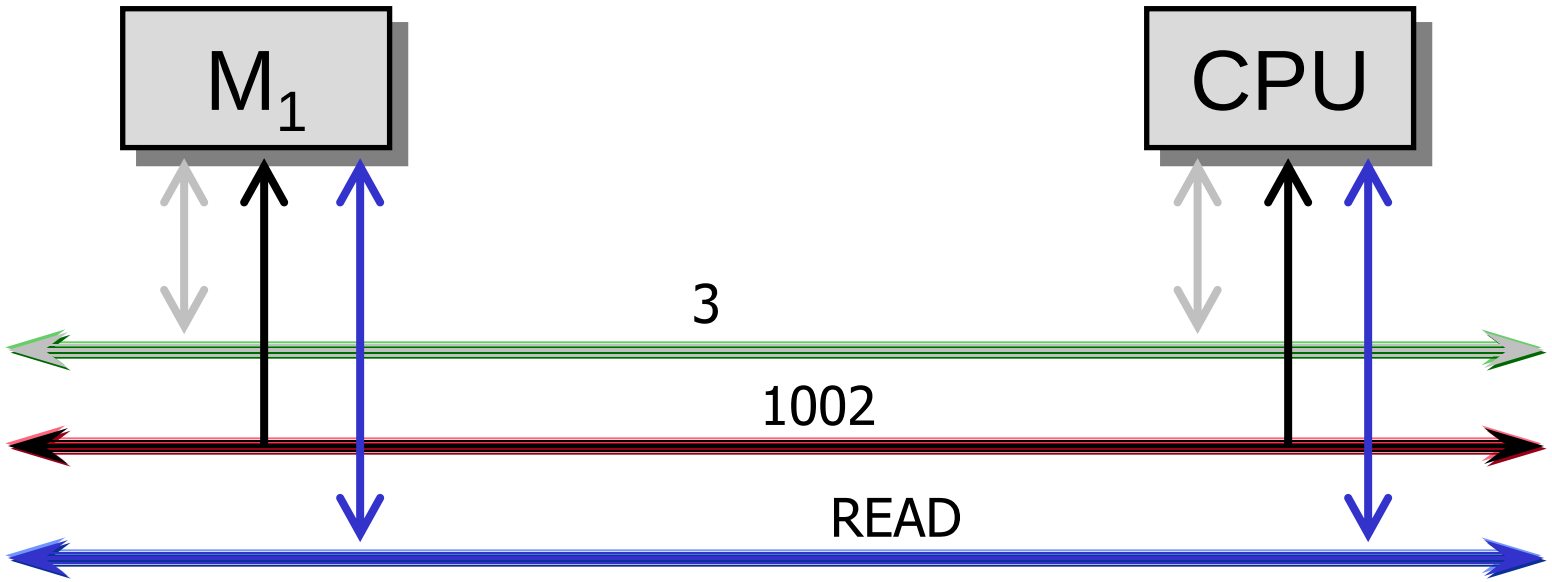
Bus types

- A single bus is composed of the following buses:
  - Data bus (DBus)
  - Address bus (ABus)
  - Control bus (CBus)

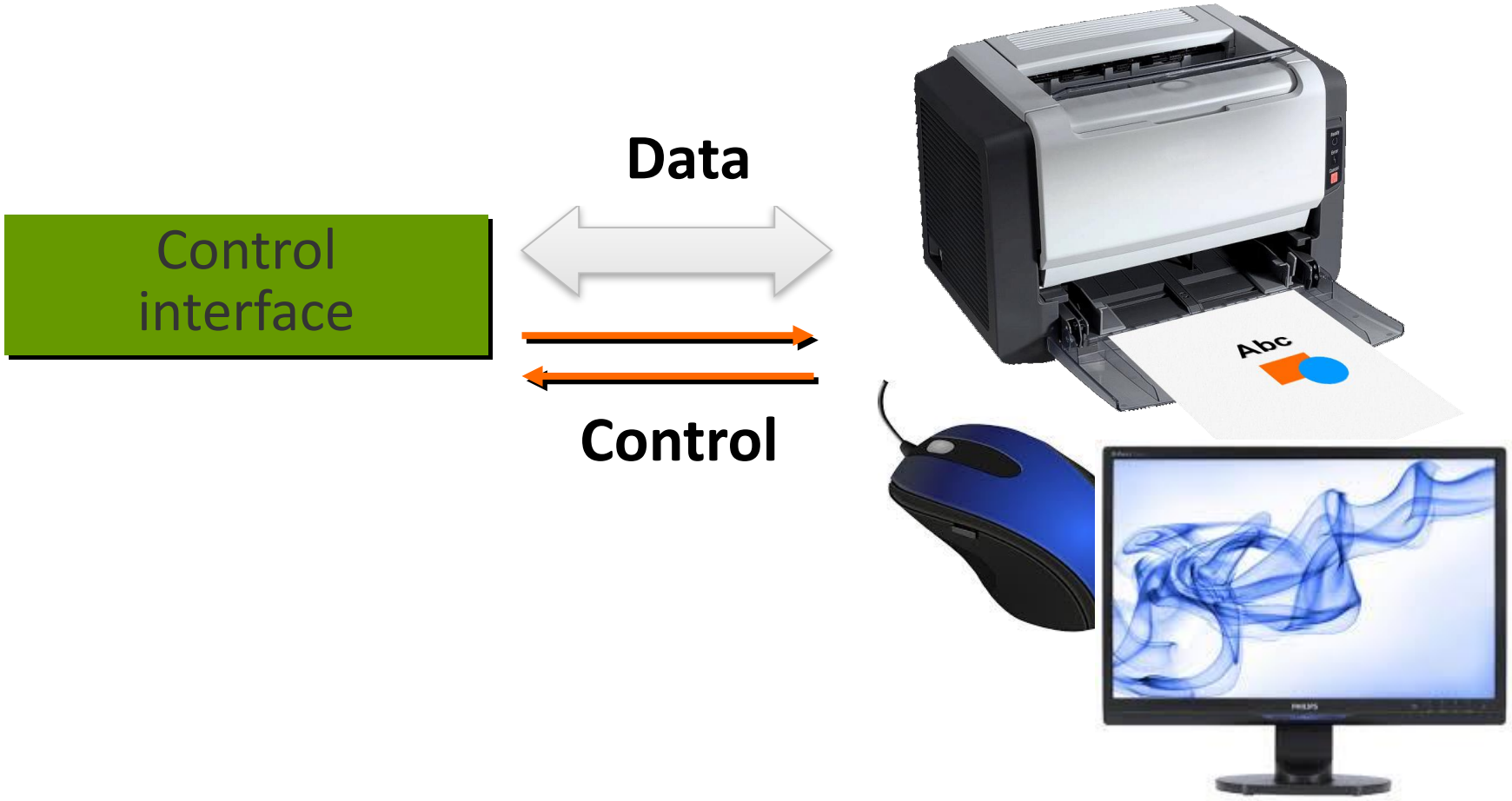


Bus cycle

- It is the time (in clock cycles) required to transfer a single Data from Memory to the CPU or vice versa:
  - CBus (READ)
  - ABus (1002)
  - Dbus ("3")



Peripheral devices



Input/Output (I/O) devices

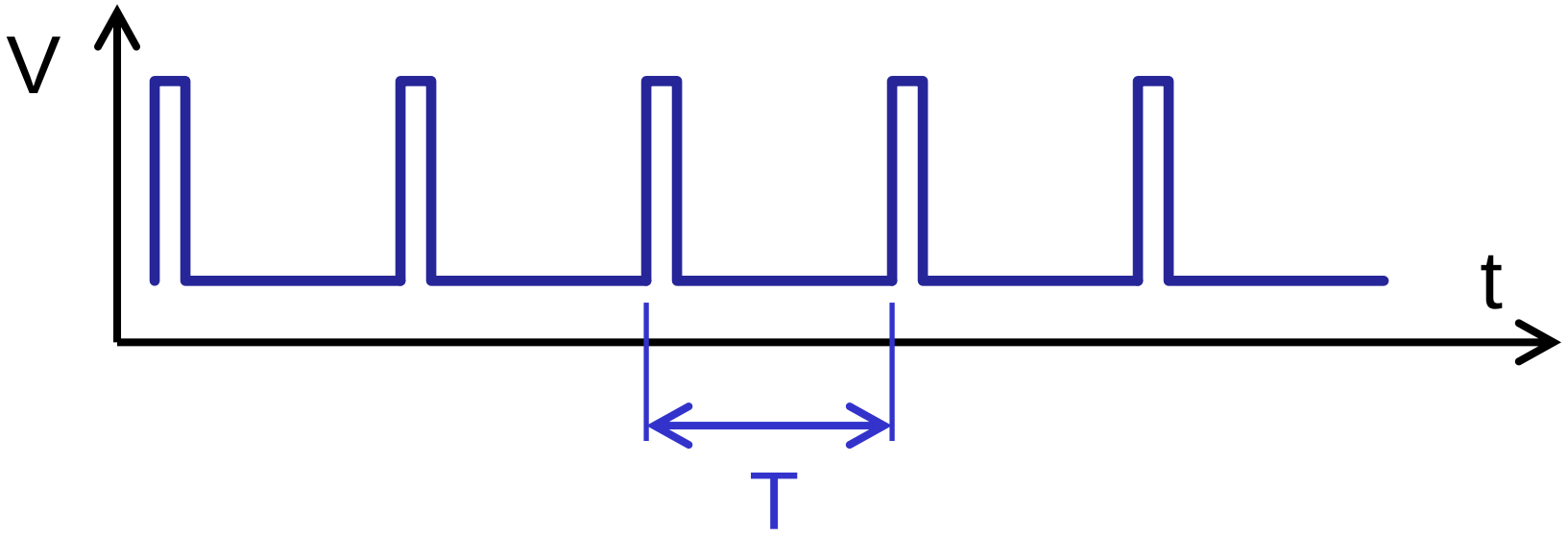
- Enable the interaction of the computer with the external world, by means of synchronized digital signals.
  - Input: From the external world to the system
    - Examples: Keyboard, mouse, microphone, etc.
  - Output: From the system to the external world
    - Examples: Monitor, printer, speakers, etc.

The clock

All the computers have a timing element (namely ***clock***) generating a temporal reference common for all the elements that are part of the elaborating system.

The human body uses asynchronous analog signals.

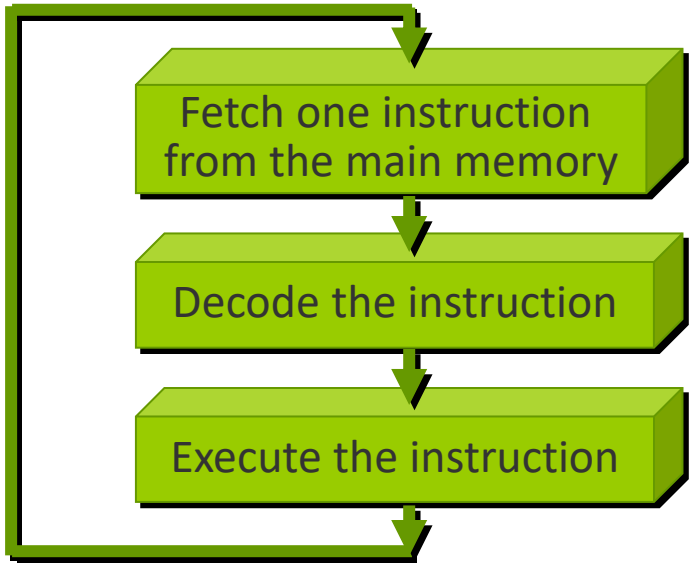
The clock



- T = clock *period*
  - Measure unit = s
- f = clock *frequency* (= 1 / T)
  - Measure unit = s^{-1} = Hz (cycles/s)

Instruction timing

- A *machine-cycle* is the time interval where the basic operation is executed and it is an integer multiple value of the clock period
- The execution requires an integer number of machine cycle variable according to the kind of instruction

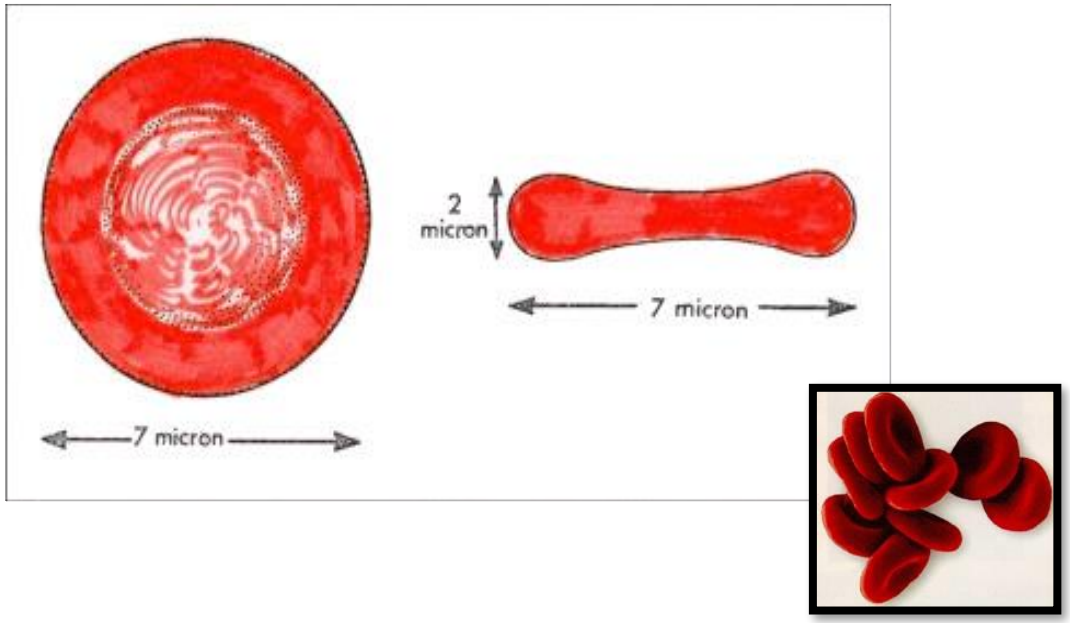


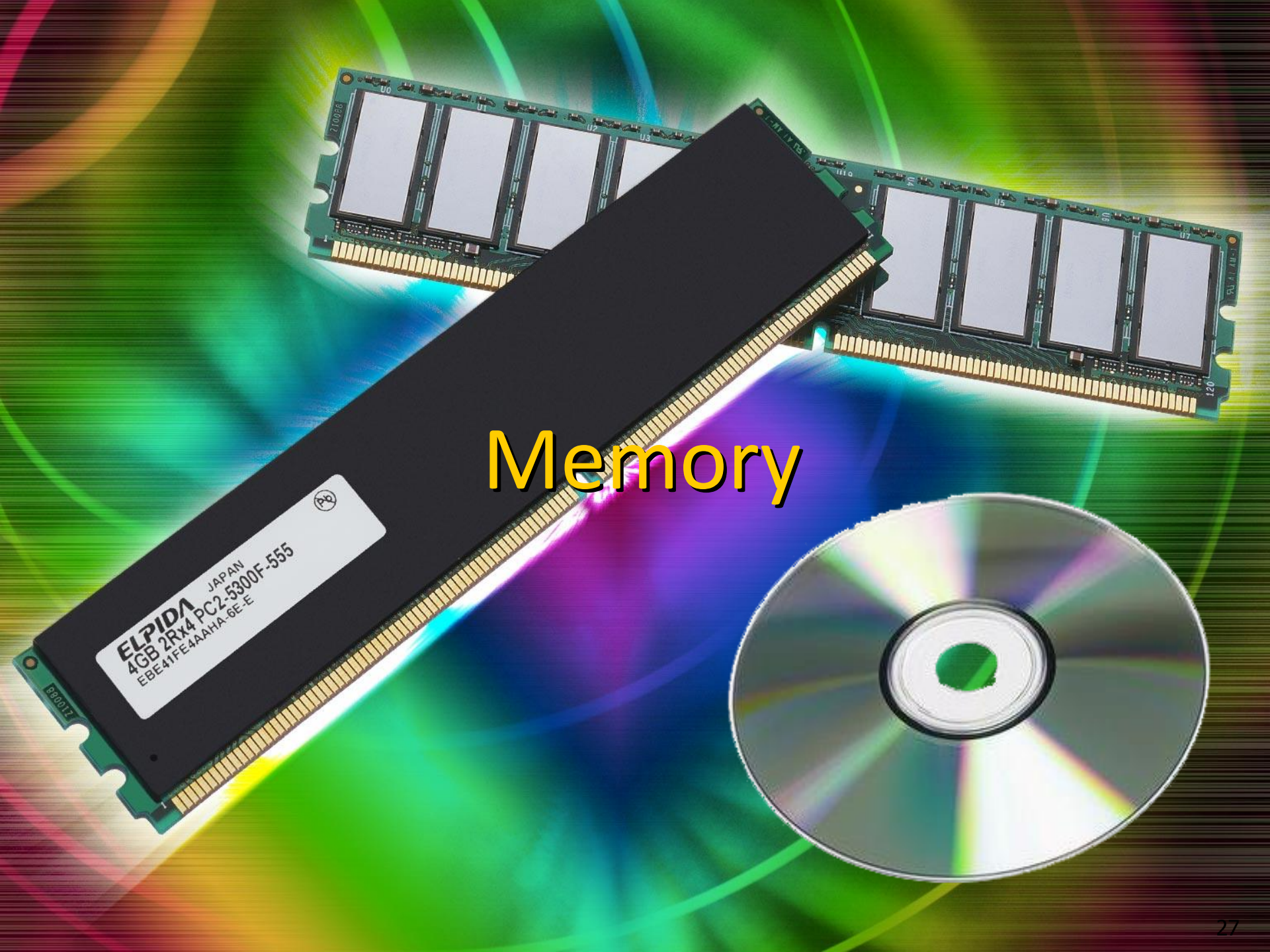
Information facts

- In an Intel Core i7-2700 the clock frequency is 3.5 GHz
  - Note that in 3.5 millionth of a second, light runs about 1 m (104.93 cm)

Information facts

- Some Intel Core i7 and i5 are made using 32 nm technology
  - The cesium atom diameter lengths 0.5 nm
  - A red blood cell is 2.000 nm x 7.000 nm
  - Human hair sizes about 100.000 nm




Memory
ELPIDA
JAPAN
4GB 2Rx4 PC2-5300F-555
EBE41FE4AAHA-6E-E

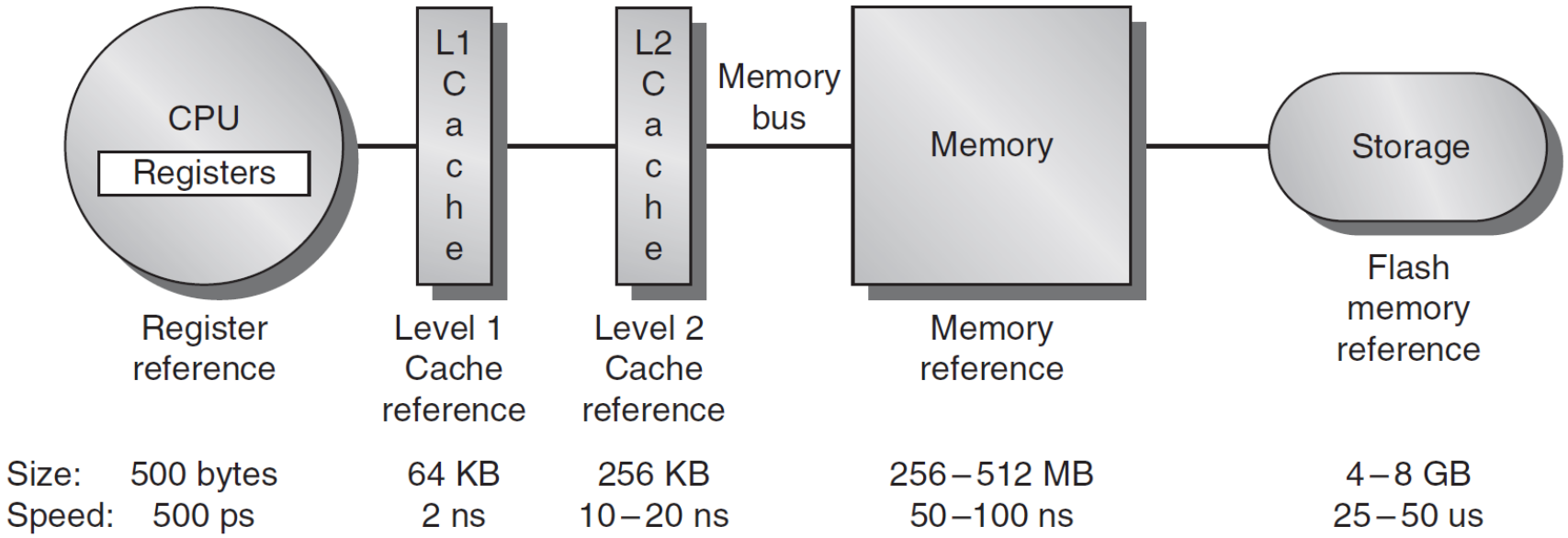
Memory

It stores data and instructions that the computer needs to execute.

Features:

- Addressing
- Parallelism
- Access (sequential or random)

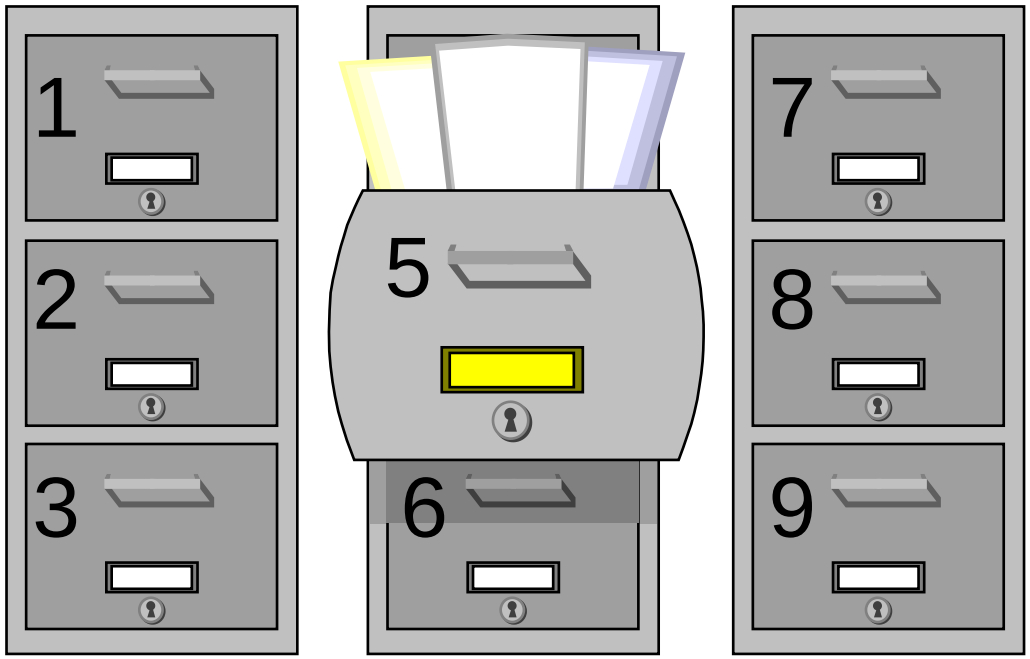
Memory levels in a typical System



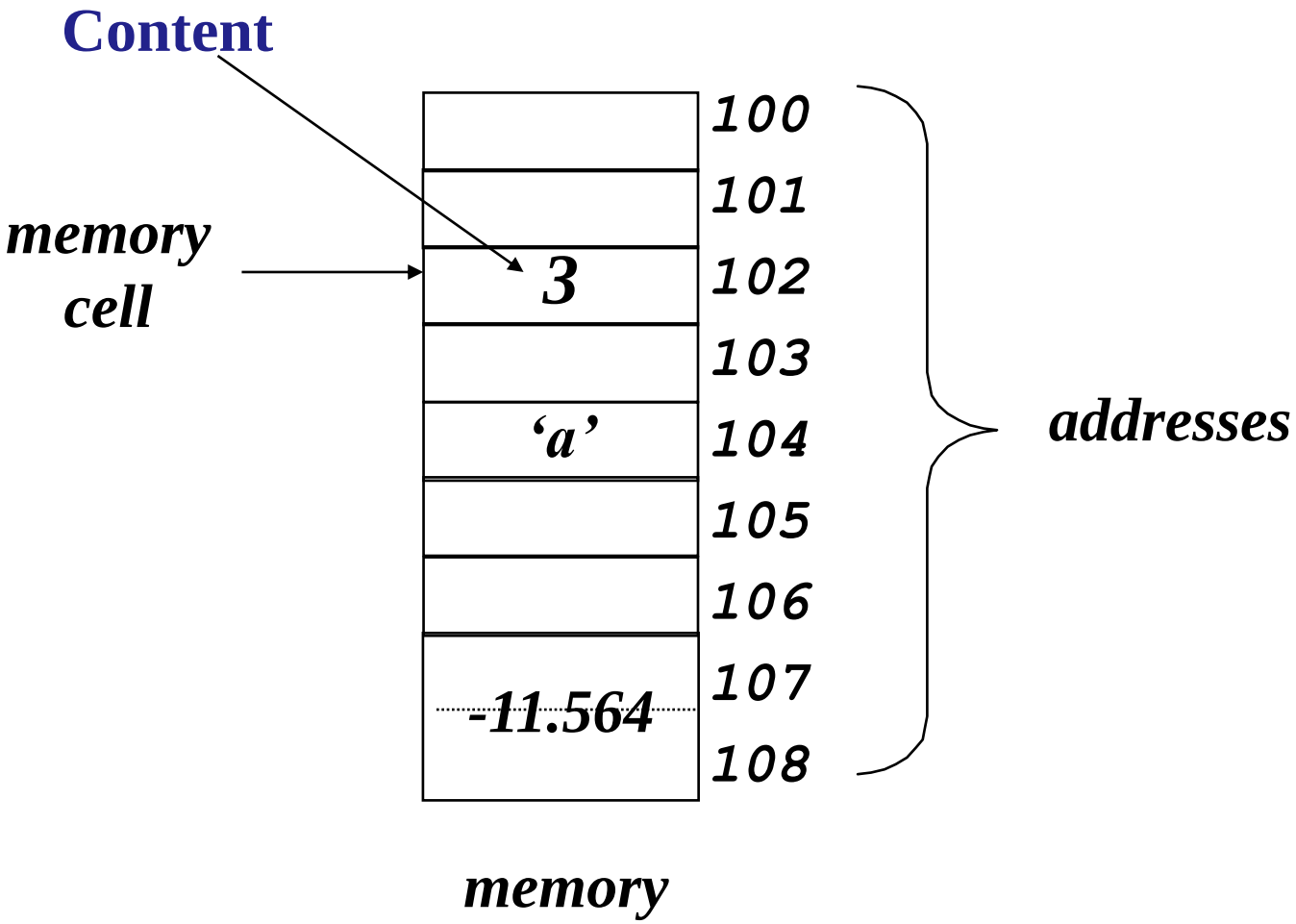
The size and time units change by a factor of 10^9.

Addressing

Memory is organized in *cells* (minimum directly accessible unit). An address (number) is assigned to each cell for uniquely identifying it.



Memory address



Parallelism

Each memory cell contains a fixed quantity of bits:

- Same for all the cells (of a certain memory unit)
- Accessible with a unique Bus Cycle
- It is a multiple of a byte
- At least 1 byte (typically a word for the main memory)

Internal Memory

- Inside the computer
- Solid state (*chip*)
- Usually volatile
- Fast (nanoseconds, 10^{-9}s)
- Limited quantity (some GB)
- Not removable
- Expensive (0.1 € / MB)

External Memory

- External to the computer
- Sometime removable
- Not electronic (e.g., magnetic, optical)
- Permanent
- Slow (milliseconds, 10^{-3} s)
- Large quantity (some TB)
- Cheap (0.1 € / GB)

Maximum internal memory (physically present)

- The Abus dimension determines the max number of addressable memory cells
- The Dbus dimension "suggests" the dimension of a memory cell (bigger cells, requiring two or more data transfer on the Dbus, are also possible)

- max mem = $2^{|Abus|}$ x |Dbus| bits

- example (Abus of 20 bit, Dbus of 16 bits):
  max mem = 2^{20} x 2 bytes = 2 MB
  i.e., 1 M memory cell, each of 2 bytes

Maximum External Memory

- The external memory (ex. disk) does not depends on Abus because it is considered as a peripheral (input and/or output)
- The maximum external memory quantity depends on the I/O bus (where peripherals are connected)