TRIKALESHWAR S

Physical Design Engineer

Mail :trikaleshwarshankar@gmail.com
Phone :+91 91487 60407
LinkedIn: https://www.linkedin.com/in/trikaleshwar-shankar-1185a9246

Physical Design Engineer with hands-on RTL-to-GDSII experience at 28nm and 14nm, specializing in floorplanning, power planning, CTS, timing closure, and sign-off. Proficient with Synopsys (DC, FC, ICC2, PrimeTime, StarRC) and Cadence (Genus, Innovus, Tempus, Quantus) toolchains, with MCMM, multi-voltage, and multi-clock design exposure. Adept at STA and PPA optimization, backed by industry internships and project work in ASIC and FPGA-based digital design.

Experience

VLSIGURU | TRAINEE | Physical Design — *June 2025 - Present*

- Fundamentals of digital design, linux , CMOS working ,and a novice in TCL scripting .
- Implementation of ASIC design flow on a project with 56k cell count, muti-volt and multi-clock design using 28nm node from netlist to sign-off.
- Worked with tools like synopsys [DC-ICC2 and FC] ,cadence[Innovus and genus] and supporting tools like PrimeTime, Tempus, Quantas and StarRC.
- Performed sanity checks and STA with debugging and error fixing to achieve optimal PPA.

Siemens | INTERN — *June 2023 - Sep 2023*

- Implemented PLC logic in a 802D controller .Worked on a project to run PLC logic in a sinumerik S7.

Entuple Technologies Pvt.Ltd | INTERN — *March 2022 - June 2022*

- As an intern I learnt full custom flow from RTL to GDS-II in 14nm.
- Implemented project on 24/12 hour clock circuit using FSM and clock gating to optimize power and extracted the GDS file.

Projects

ASIC flow of Block-level design

- Executed optimal floorplanning and macro placement with (56k cells, 40 macros, 3 master clocks, 3 generated clocks and 2 virtual clocks) on a multi-volt, ensuring robust timing and efficient power grid structure by .
- Performed standard cell placement, clock tree synthesis, and detailed routing to achieve timing closure and DRC-clean connectivity.
- Utilized Synopsys ICC2, PrimeTime, and Cadence Innovus/Genus for design implementation, signoff, and timing analysis.

Implementation and optimisation of AES -256 using FPGA

- Writing a efficient and synthesizable RTL code for AES-256 encryption algorithm.
- Implemented the same on a Altera Deca Max-10 FPGA to test the code using Quartus tool.
- Funded and selected for state level seminar and exhibition by KSCST 46th series of SPP.

Design and verification of RTL code "Alarm clock" in 28nm

- Designed a efficient RTL code for a alarm clock in Verilog using FSM , clock gating and verify the same with test-benches using cadence EDA tools .

Network Jammer Circuit

- Built an analog RC circuit to block incoming 2G Radio signals to the mobile phone working in the range of 800-1200Mhz using RLC network and timer circuits.

Noise Suppressed Photon Fidelity

- LI-FI technology implemented using LASER for transmission of data over a long range with active noise removal by OPAMPS.

Skills

- Pnr flow
- TCL scripting
- STA
- CTS
- Debugging
- Linux
- Verilog
- PPA
- DRC/LVS

Tools

- Fusion Compiler
- DC- ICC2
- PrimeTime ,StarRC
- Innovus
- Genus
- Quantas

Certificate and coursework

- RTL to GDS [NPTEL]
- CTS 1 and 2 [VSD - Udemy]
- STA 1 and 2 [VSD - Udemy]
- TCL beginner to advance [Udemy]
- Soft skills and Ethics [NPTEL]
- Timing ECO [VSD - Udemy]
- Physical Design with timing analysis [NPTEL]

Education

B.E in ECE — *2019-2023*

- Rajarajeswari College Of Engineering .
- CGPA: 8.56