

Performance Analysis of Power Factor Correction in SEPIC Converter Topologies

**Software-Based Solution for Electrical Engineering (19EEE311)
PROJECT REPORT**

Submitted by,

Kenny Gee Oberoi J.M. - BL.EN. U4EEE21017

Kumar Durga Trinadh Myreddy - BL.EN. U4EEE21020

Ram Chaitanya T - BL.EN. U4EEE21033

**BACHELOR OF TECHNOLOGY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING**



**AMRITA
VISHWA VIDYAPEETHAM**

AMRITA SCHOOL OF ENGINEERING, BENGALURU-560035

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Problem Statement:

Conventional rectifiers exhibit drawbacks such as high current pulses and poor power factor, leading to decreased system reliability and increased energy consumption. Power Factor Correction (PFC) converters mitigate these issues by reducing reactive power and harmonics, though they introduce complexity and cost. Efficiency variations among converter topologies pose a challenge, as achieving high efficiency often involves increased complexity, impacting system reliability. Moreover, efficiency and power *factors* directly influence system reliability, emphasizing the need for careful consideration of trade-offs in power conversion system design to optimize performance and longevity.

Objective:

- Analyzing the input and output parameters of the PFC topologies
- Comparing the complexities of the topologies
- Improvement provided in the input power factor by different topologies
- FFT analysis for all the topologies to find the THD of the input parameters.

Theory:

SEPIC converters are versatile in their ability to step up or step-down DC voltage, making them valuable in various applications where voltage conversion is needed. However, increasing the number of power electronics components in a circuit, such as in more complex SEPIC configurations, can lead to a decreased power factor. Power Factor Correction (PFC) circuits become essential in such cases to mitigate input harmonics and improve overall system efficiency.

The advantages of SEPIC topologies include their ability to provide both voltage step-up and step-down capabilities with a single converter, making them suitable for applications requiring flexible voltage regulation. Additionally, SEPIC converters inherently offer isolation between the input and output, enhancing system safety and stability. Moreover, the SEPIC topology allows for continuous input and output currents, reducing stress on components and improving reliability.

However, these benefits come with drawbacks. More complex SEPIC configurations often result in reduced power factors due to increased component count and switching losses. Additionally, the presence of multiple power electronics components can lead to higher manufacturing costs and increased circuit complexity. Furthermore, while SEPIC converters inherently provide some level of voltage regulation, they may not achieve the same efficiency levels as dedicated step-up or step-down converters in certain applications, potentially leading to energy losses. Therefore, careful consideration of the trade-offs between flexibility, efficiency, and complexity is necessary when selecting a SEPIC topology for a particular application.

Design and Parameters:

Parameters	Values
Input AC voltage	100 Vrms
Frequency	50Hz
Duty Cycle	0.5
Output voltage	50 Vdc
Output power	100W
Switching frequency	50KHz
Maximum input current ripple	<25%
Output voltage ripple	<5%
Inductors (L1&L2) (near source)	2.2mH
Inductor (L3) (away from the source)	68uH
Capacitor (C1&C2) (near source)	1uF
Capacitor (Co)	2200uF

MATLAB Circuit Diagram and Waveforms:

i. Conventional SEPIC PFC Rectifier

Conventional SEPIC PFC Circuit

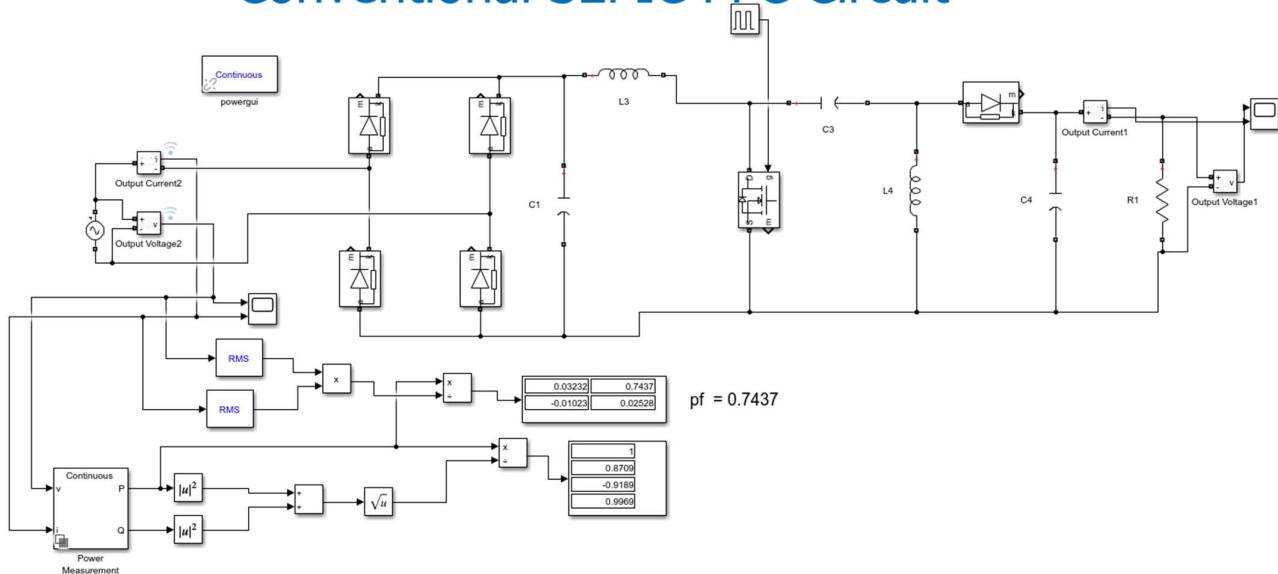
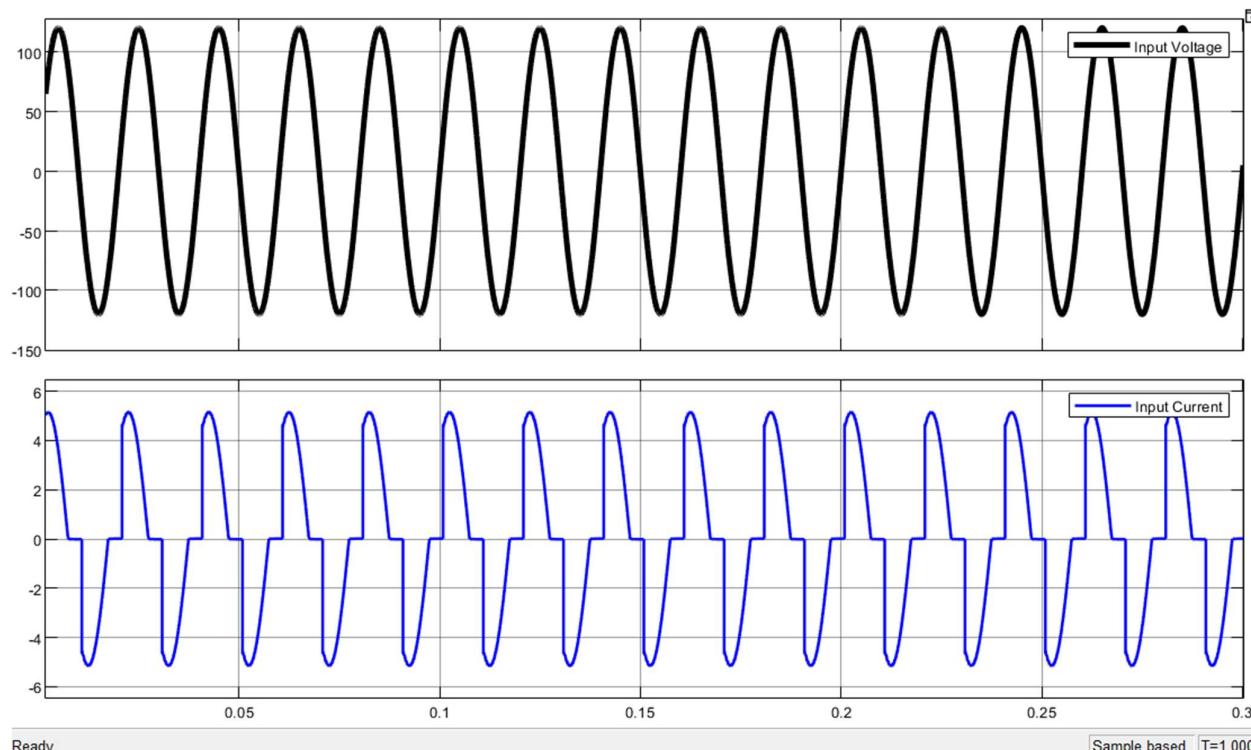


Fig 1. MATLAB Circuit Diagram of Conventional SEPIC Converter

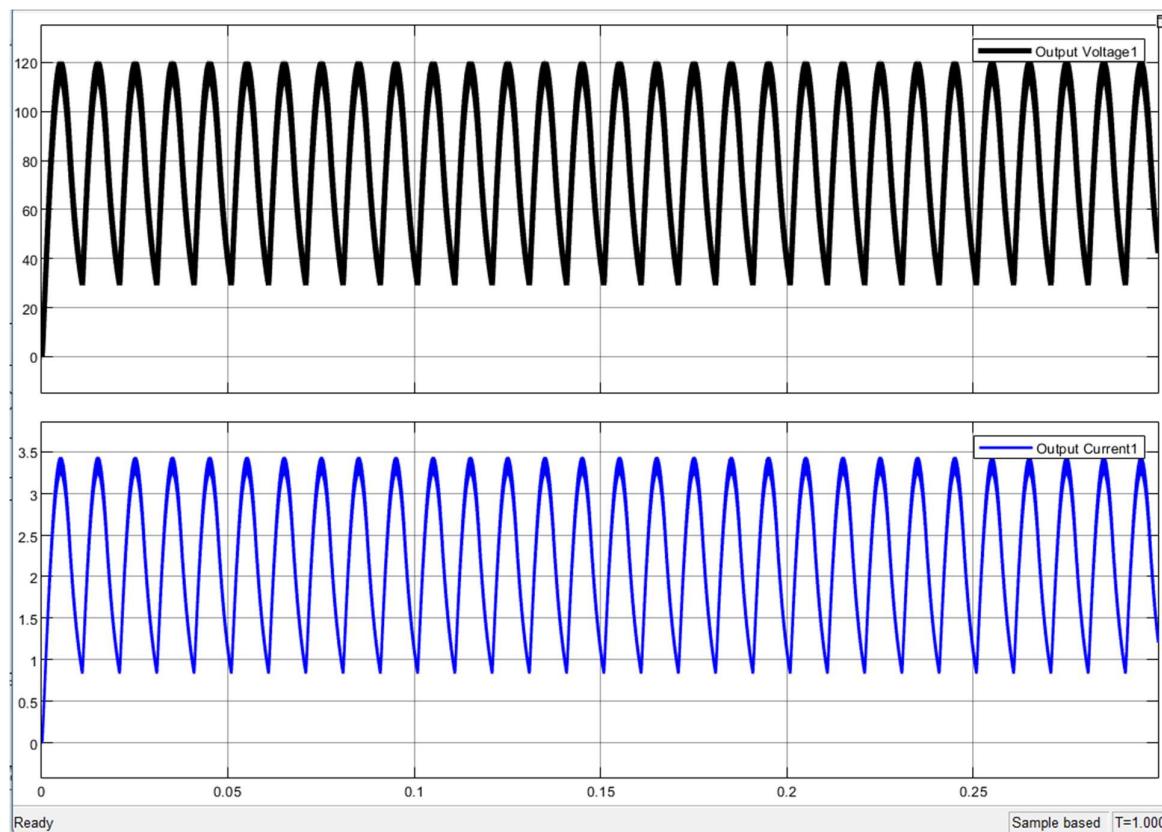
Input Waveforms:



Sample based T=1.000

Input Voltage and Current Waveform of Conventional SEPIC Converter

Output Waveforms:



Sample based T=1.000

Fig 3. Output Voltage and Current Waveform of Conventional SEPIC Converter

FFT Analysis:

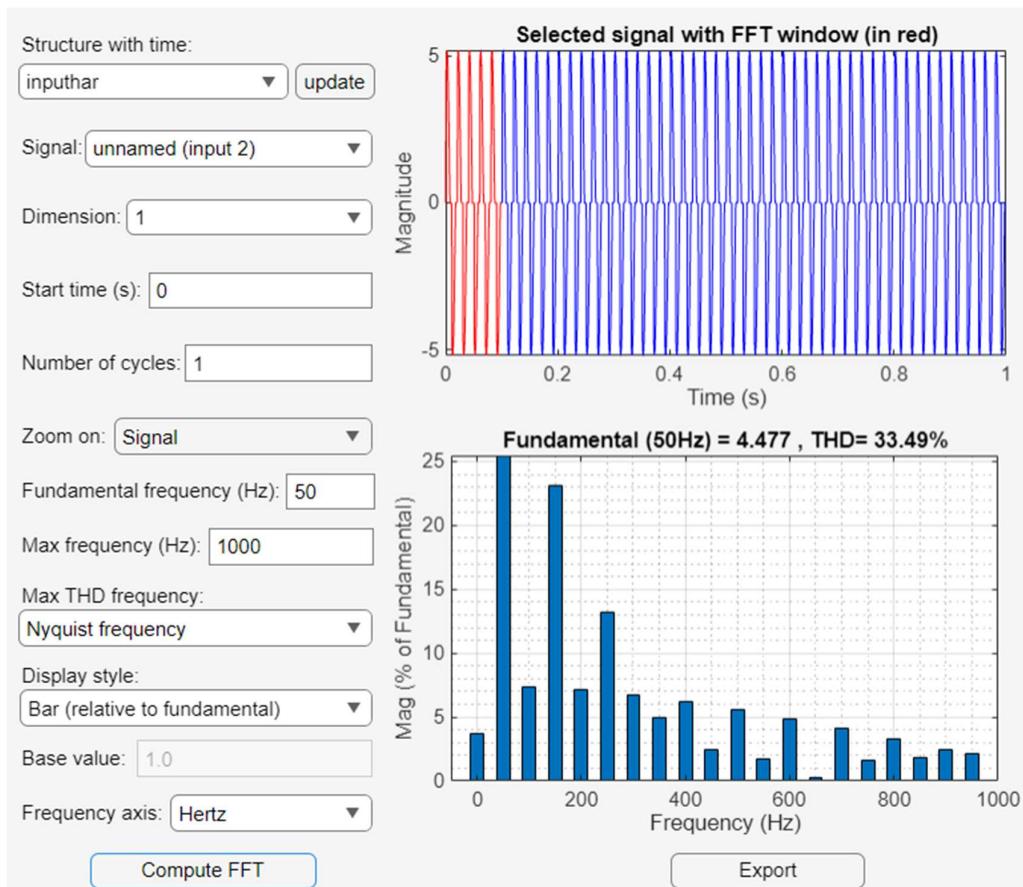


Fig 4. FFT Analysis of Conventional SEPIC Converter

ii. Interleaved SEPIC PFC Rectifier

Interleaved SEPIC PFC Circuit

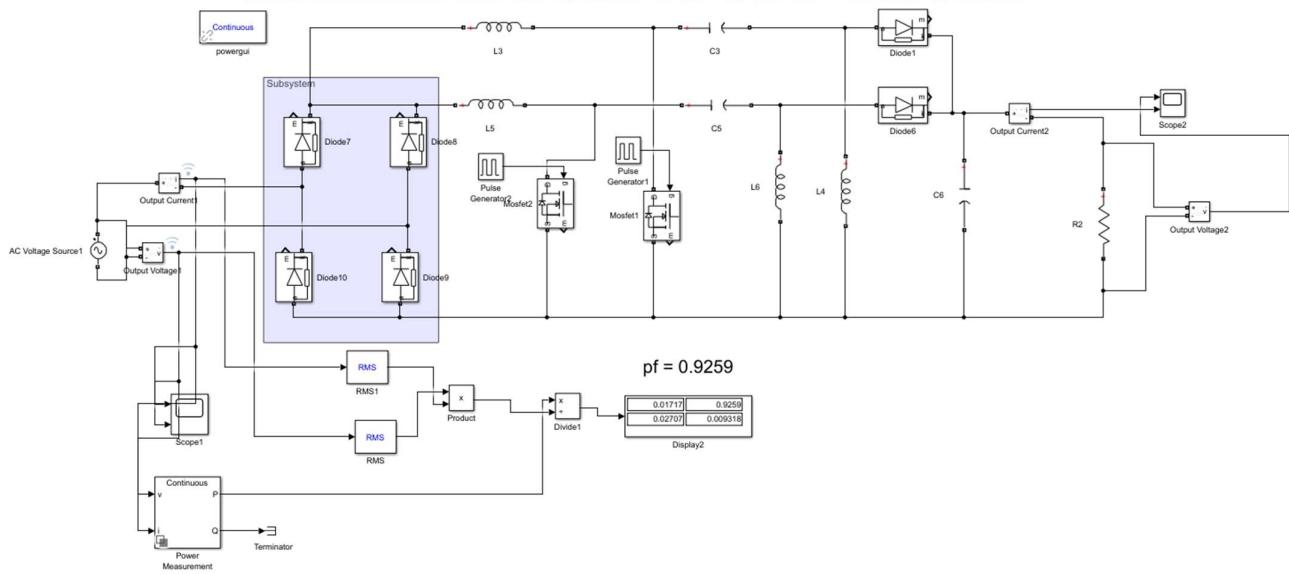


Fig 5. MATLAB Circuit Diagram of Interleaved SEPIC PFC Converter

Input Waveforms:

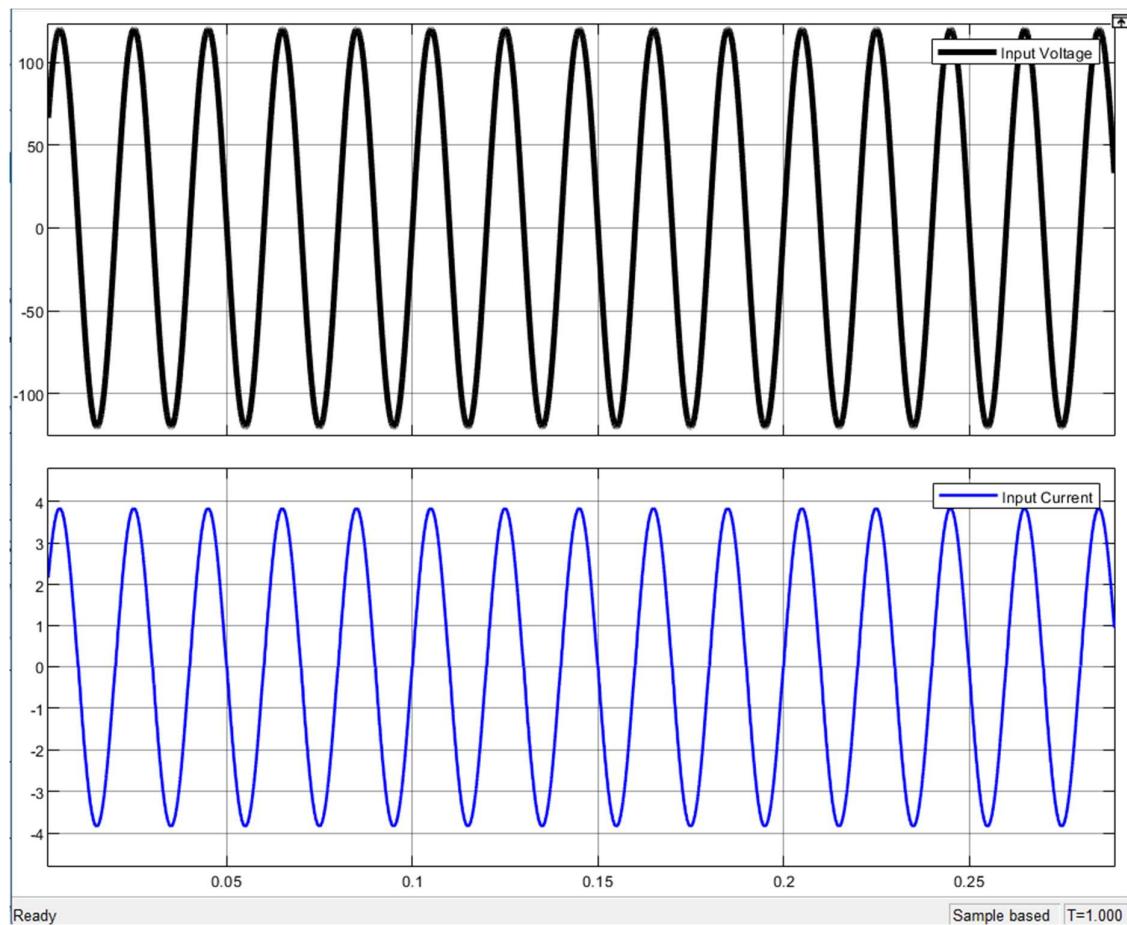


Fig 6. Input Voltage and Current Waveform of Interleaved SEPIC PFC Converter

Output Waveforms:

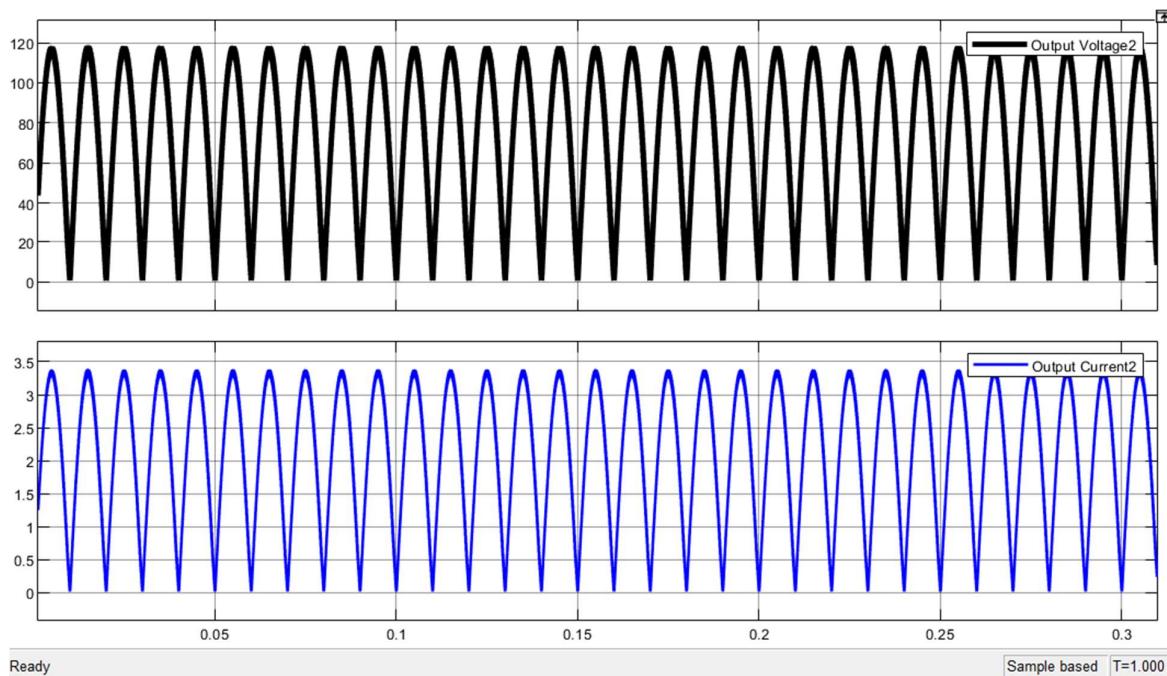


Fig 7. Output Voltage and Current Waveform of Interleaved SEPIC PFC Converter

FFT Analysis:

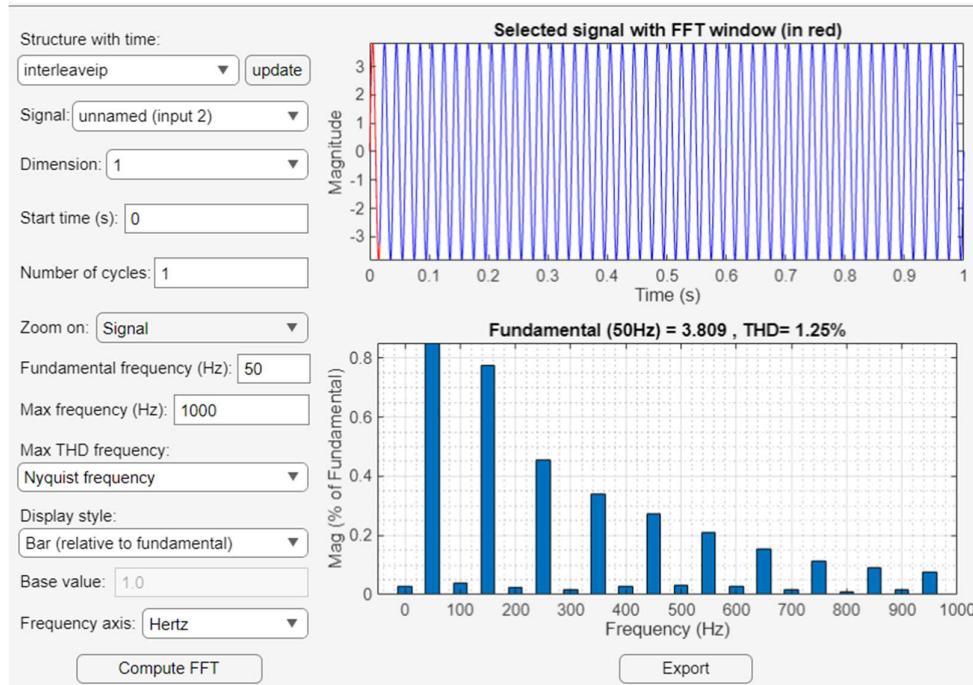


Fig 8. FFT Analysis of Interleaved SEPIC PFC Converter

iii. Totem Pole Bridgeless SEPIC PFC Rectifier

Totem Pole Bridgeless SEPIC PFC Circuit

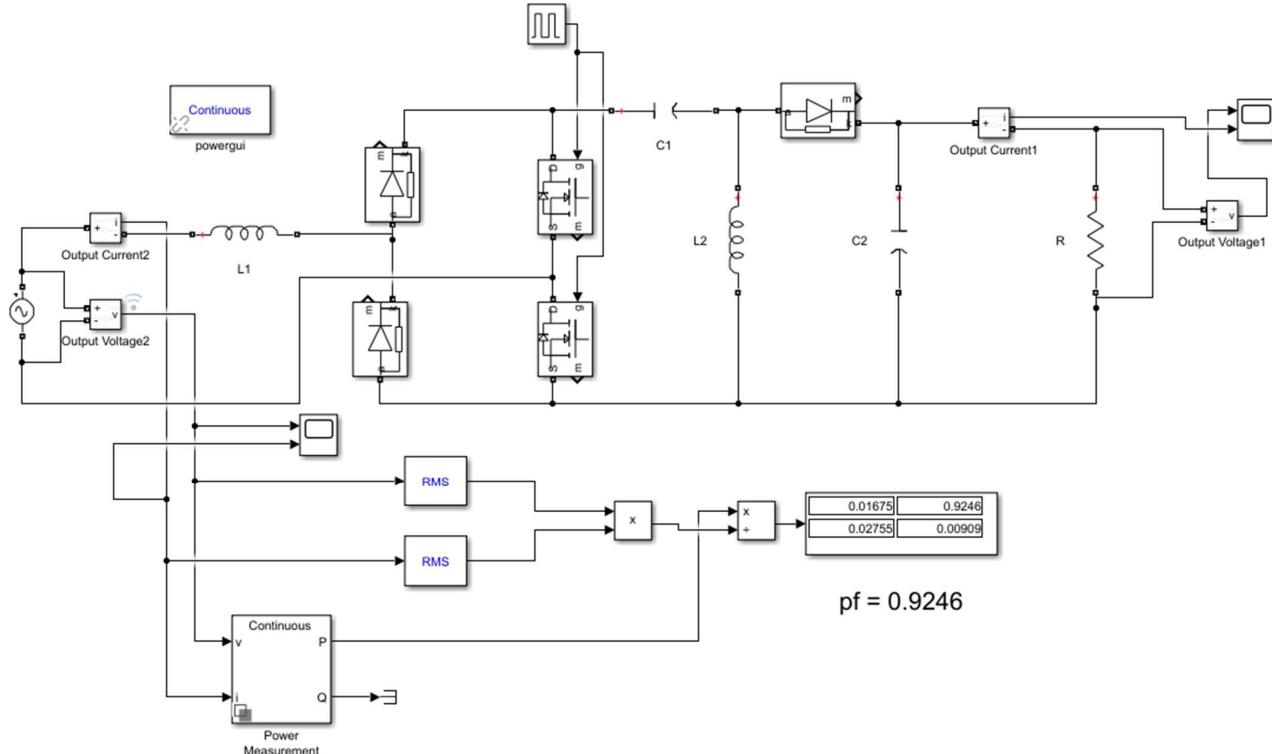
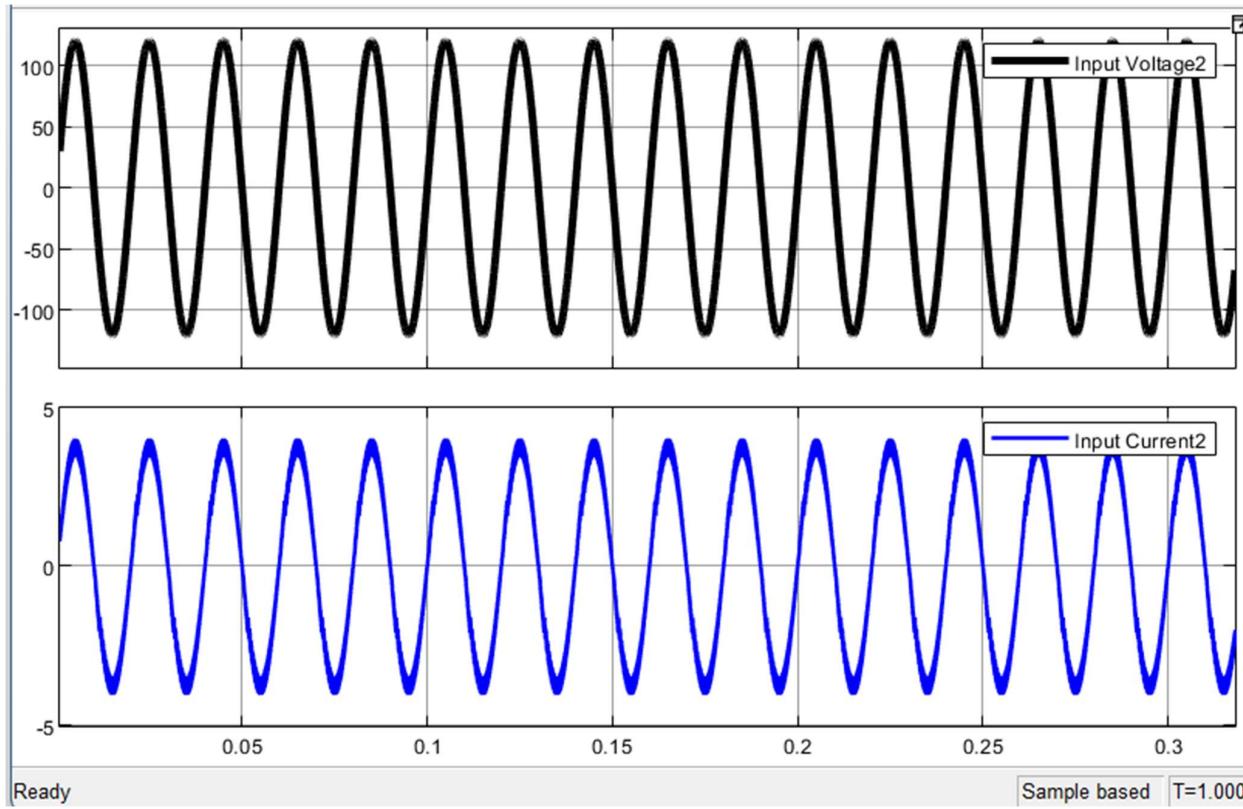


Fig 9. MATLAB Circuit Diagram of Totem Pole SEPIC PFC

Input Waveforms:



10. Input Voltage and Current Waveform of Totem Pole SEPIC PFC

Output Waveforms:

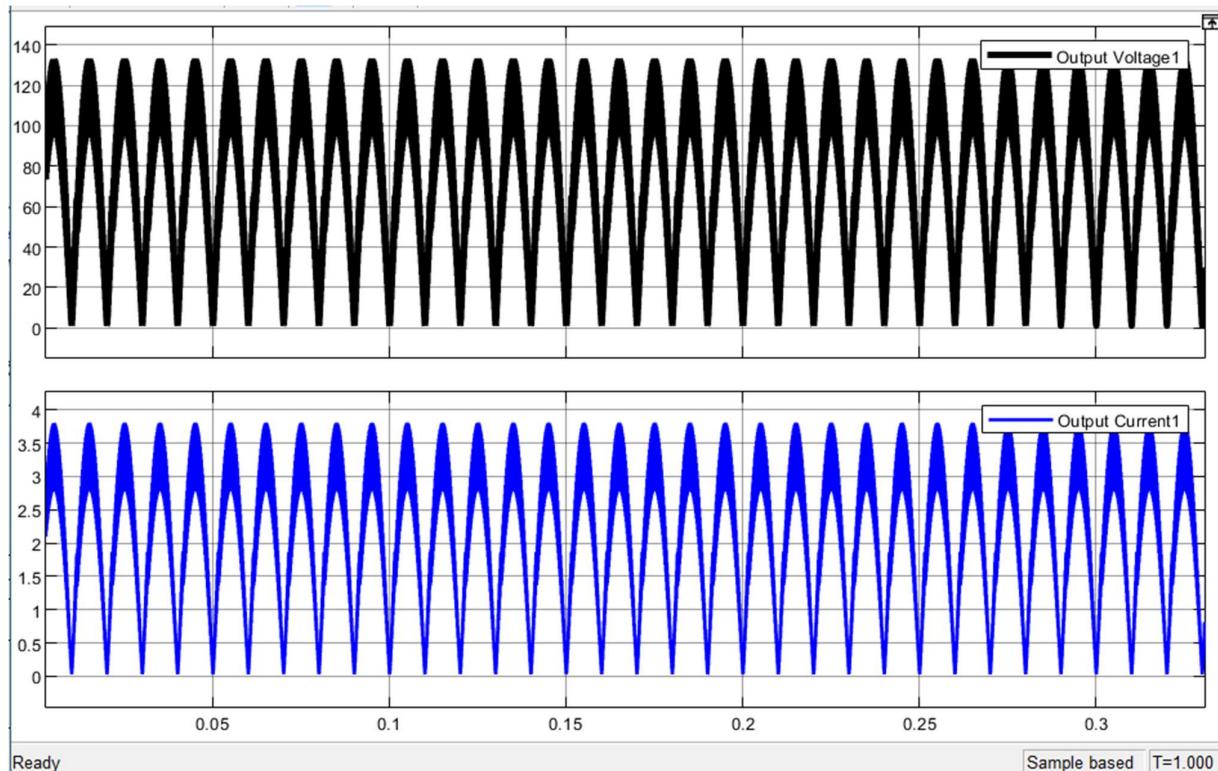


Fig 11. Output Voltage and Current Waveform of Totem Pole SEPIC PFC

FFT Analysis:

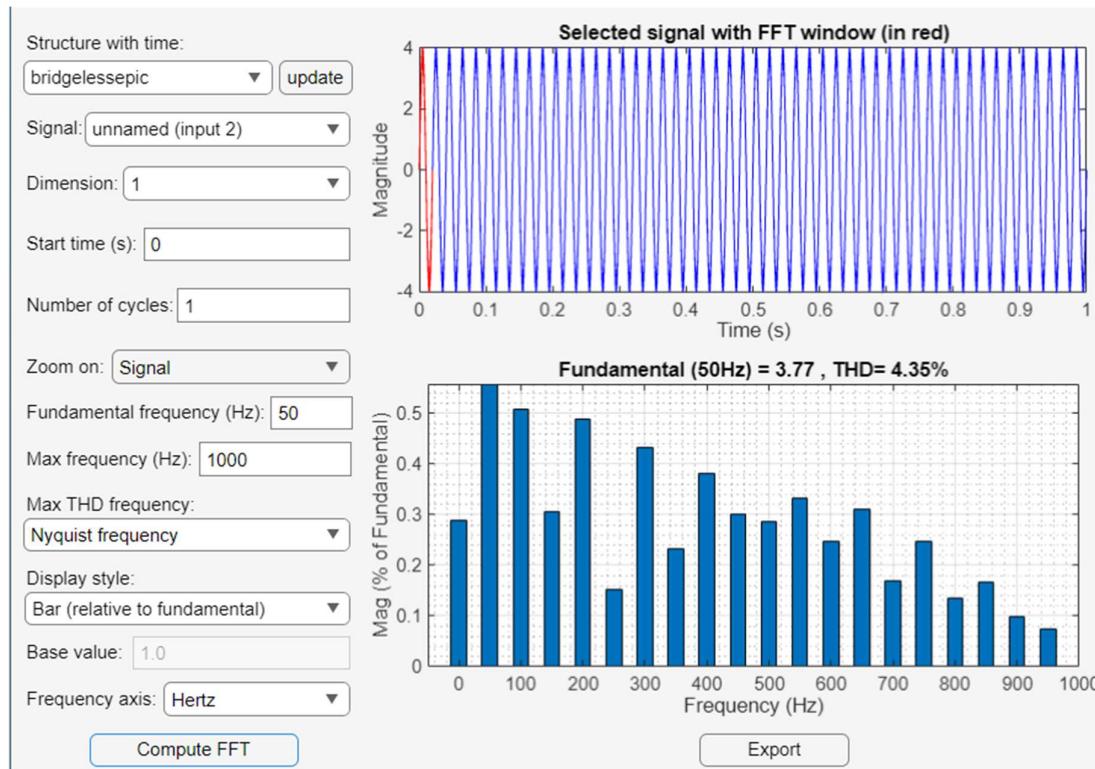


Fig 12. FFT Analysis of Totem Pole SEPIC PFC

iv. Pseudo Totem-pole Bridgeless PFC Rectifier

Pseudo Totem Pole Bridgeless SEPIC PFC

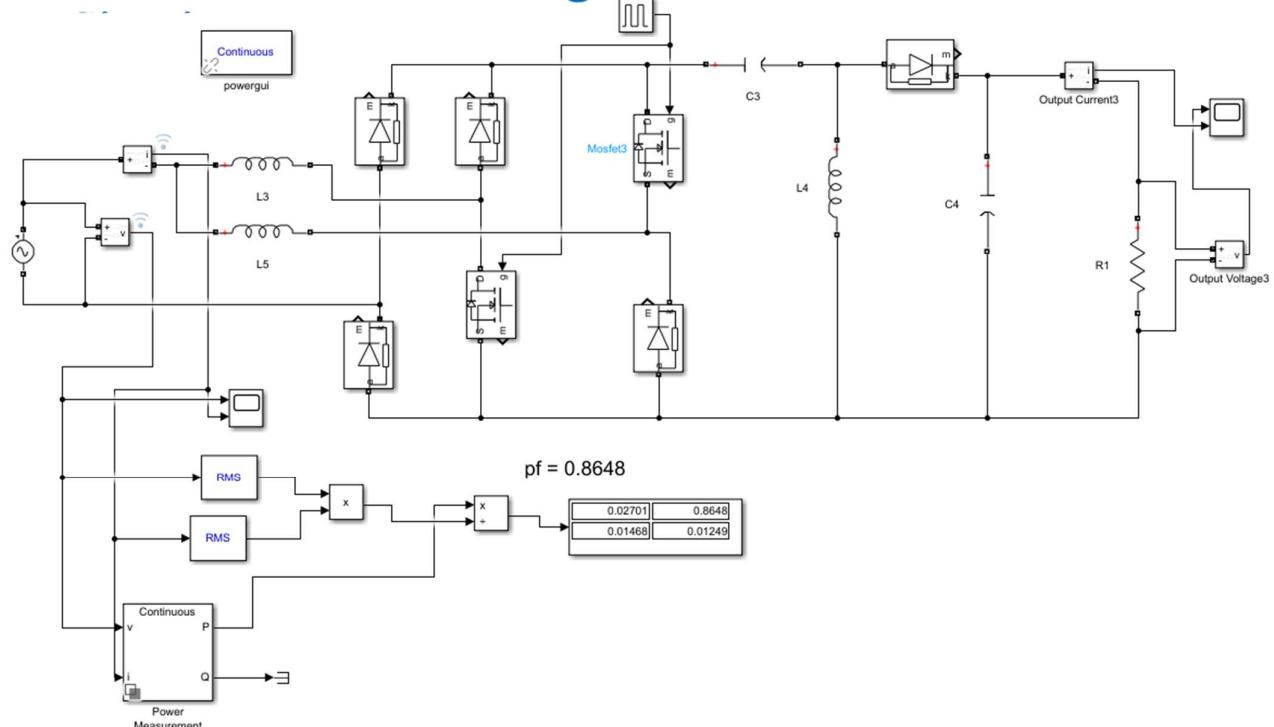


Fig 13. MATLAB Circuit Diagram of Pseudo Totem Pole SEPIC PFC

Input Waveforms:

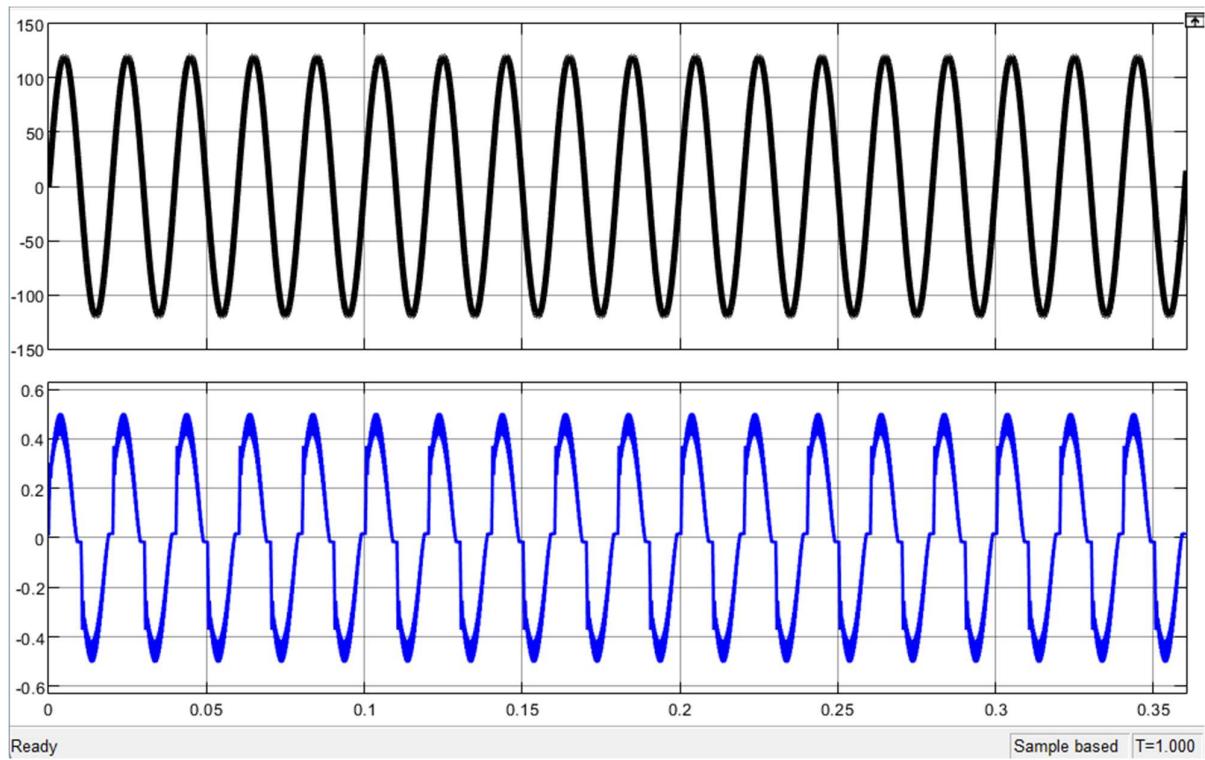


Fig 14. Input Voltage and Current Waveform of Pseudo Totem Pole SEPIC PFC

Output Waveforms:

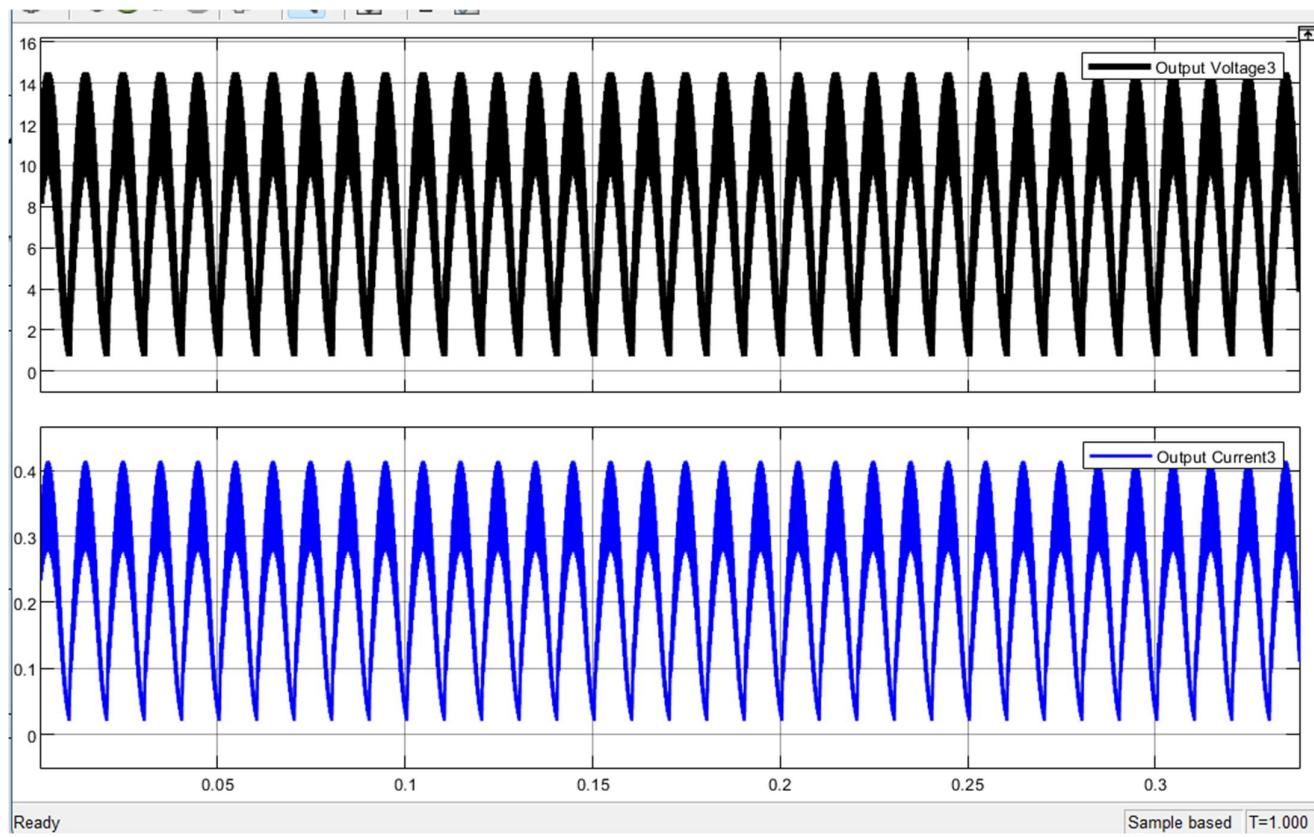


Fig 15. Output Voltage and Current Waveform of Pseudo Totem Pole SEPIC PFC

FFT Analysis:

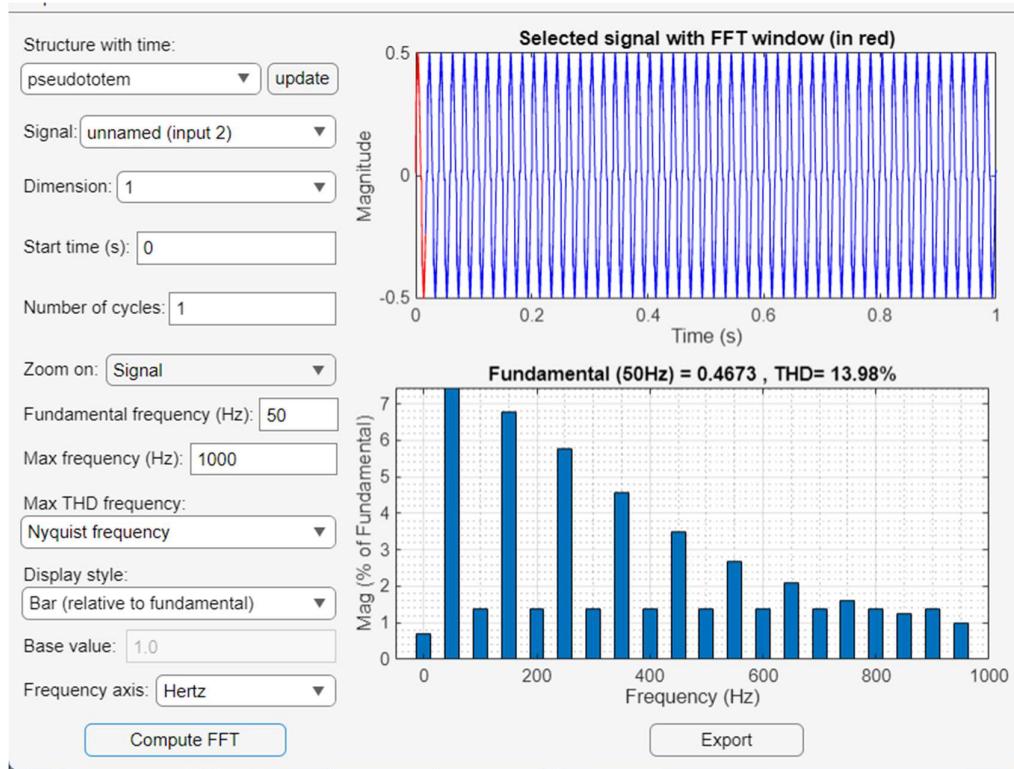


Fig 16. FFT Analysis of Totem Pole SEPIC PFC

v. New Bridgeless SEPIC PFC (taken from conference paper [2])

A New Bridgeless PFC Sepic and Cuk Rectifiers with Low Conduction and Switching Losses

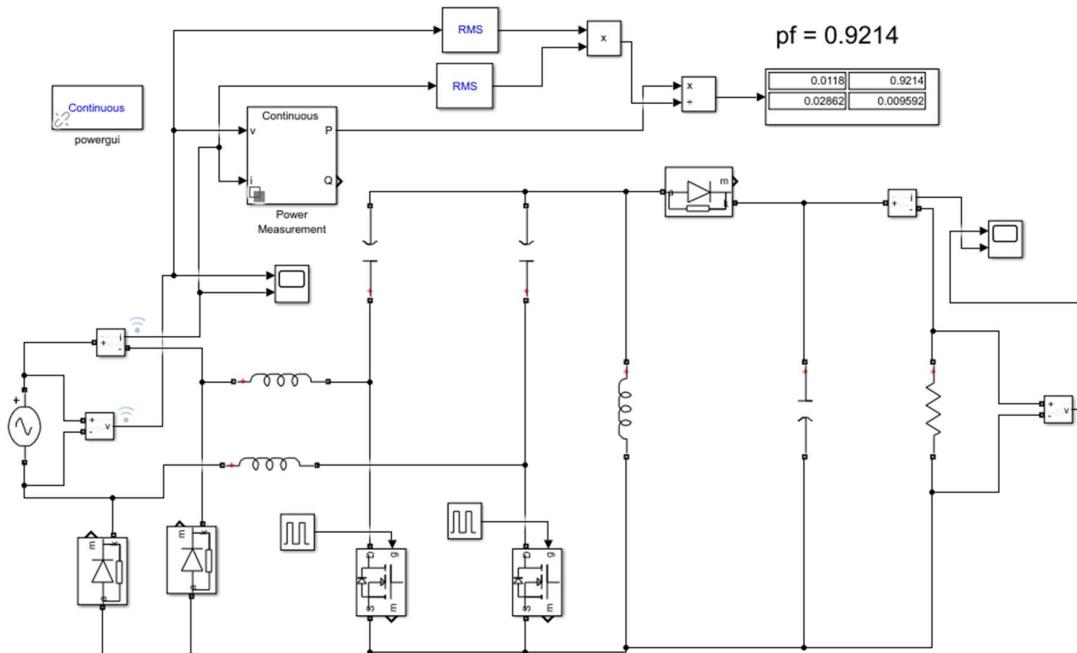


Fig 17. MATLAB Circuit Diagram of Proposed SEPIC PFC Circuit in [2]

Input Waveforms:

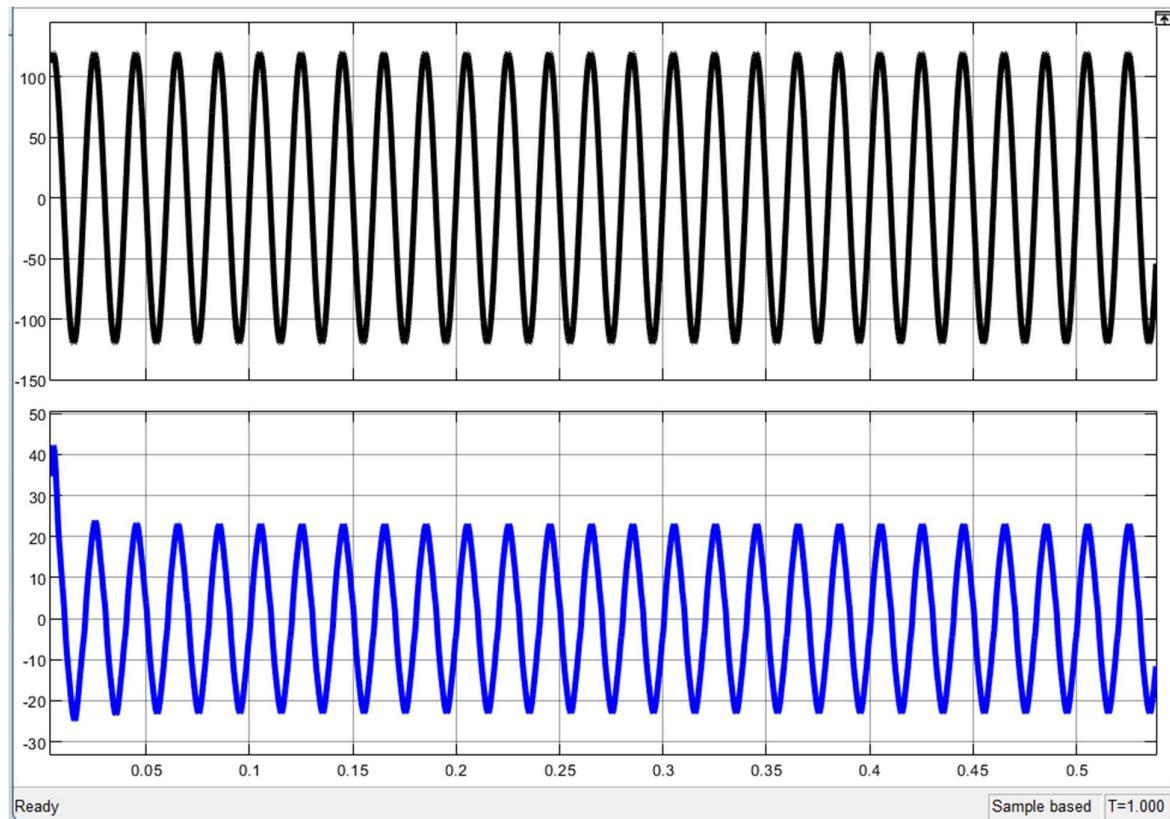


Fig 18. Input Voltage and Current Waveforms of Proposed SEPIC PFC Circuit in [2]

Output Waveforms:

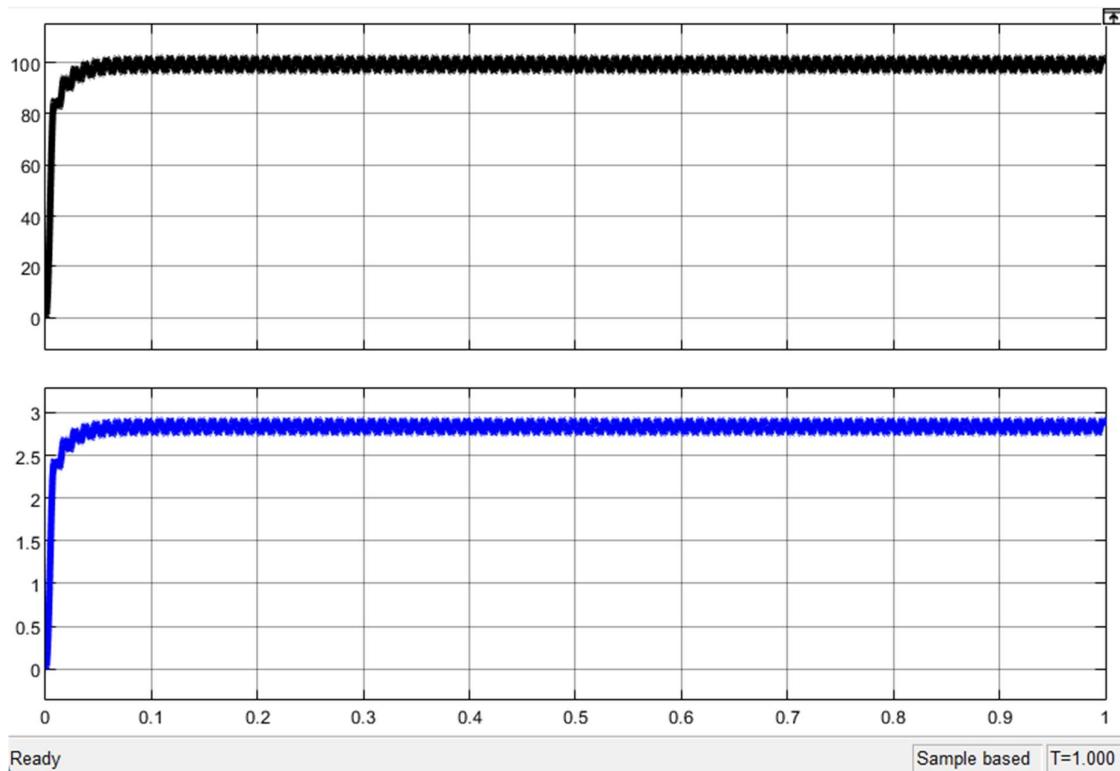


Fig 19. Output Voltage and Current Waveforms of Proposed SEPIC PFC Circuit in [2]

FFT Analysis:

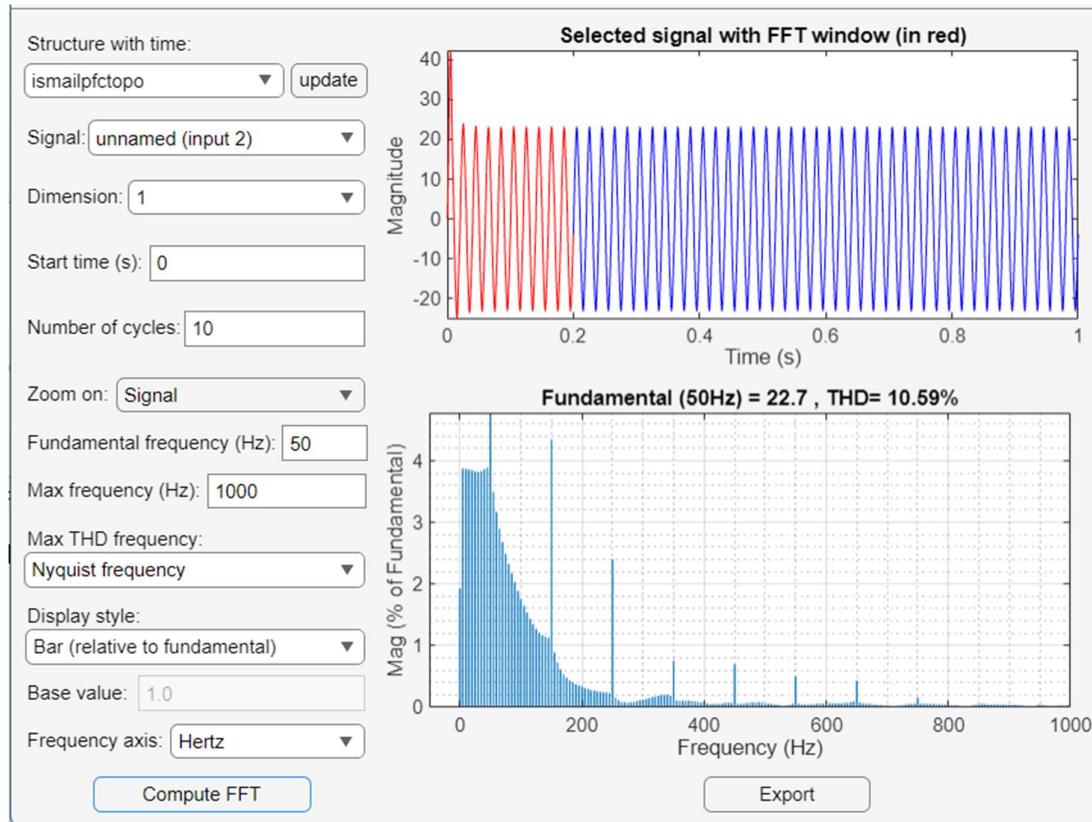


Fig 20. FFT Window of Proposed SEPIC PFC Circuit in [2]

vi. Bridgeless SEPIC Bidirectional Switching PFC Rectifier

Bridgeless PFC SEPIC Rectifier with Bidirectional Switch

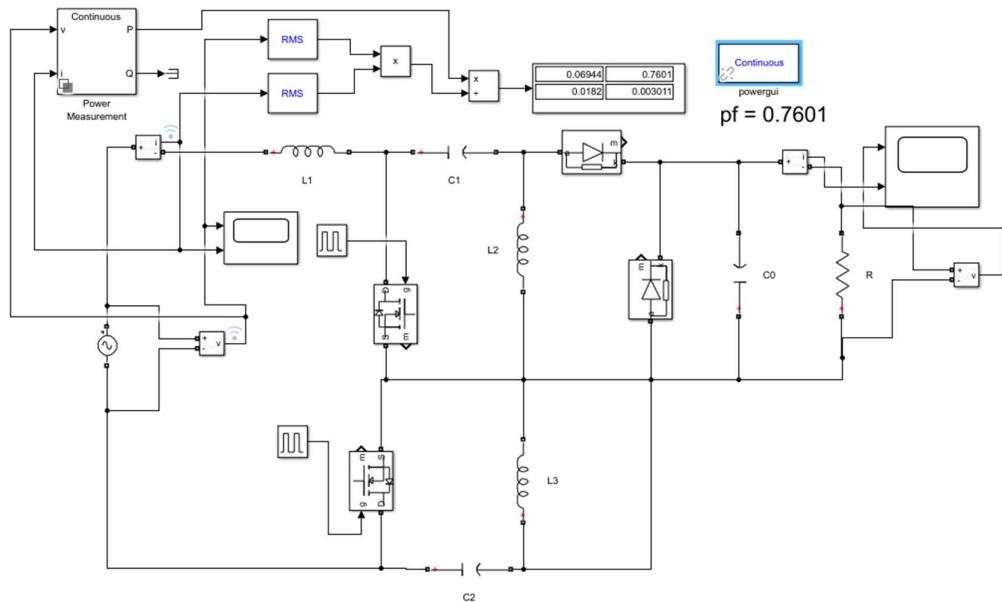


Fig 21. MATLAB Circuit Diagram of Bridgeless SEPIC Bidirectional Switching PFC Rectifier

Input Waveforms:

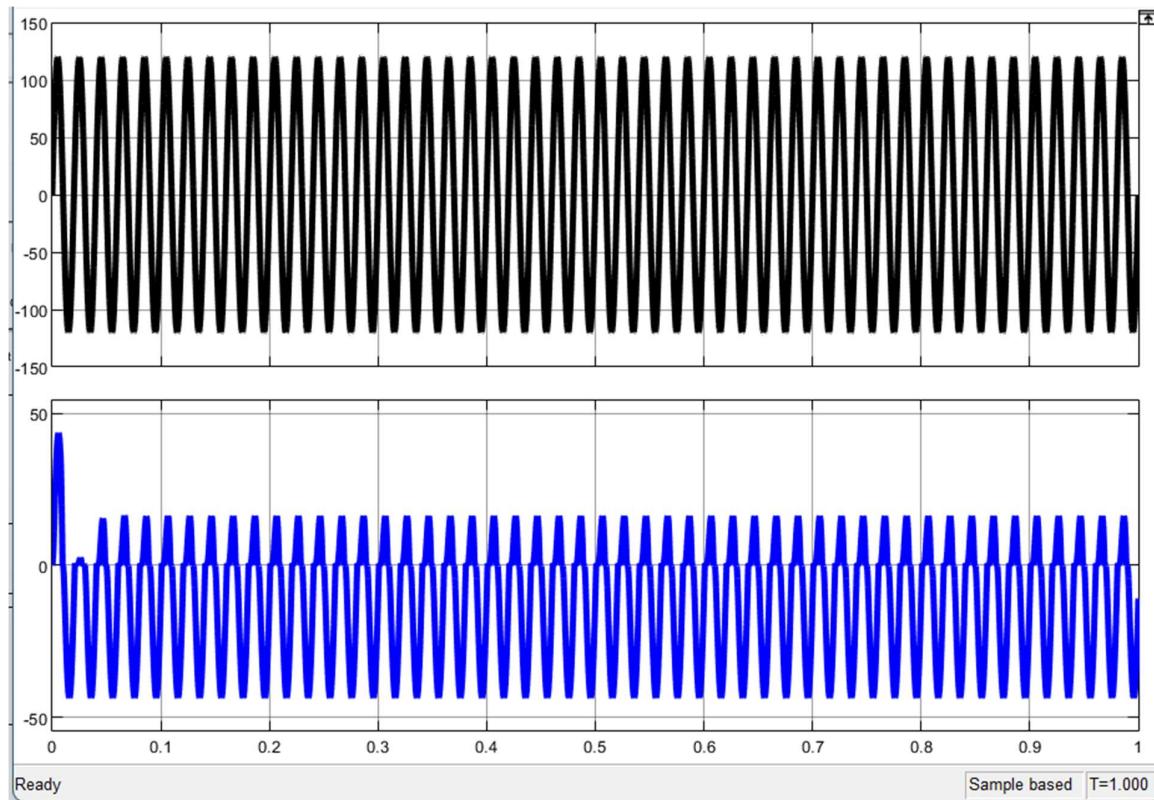


Fig 22. Input Voltage and Current Waveforms of Bridgeless SEPIC Bidirectional Switching PFC Rectifier

Output Waveforms:

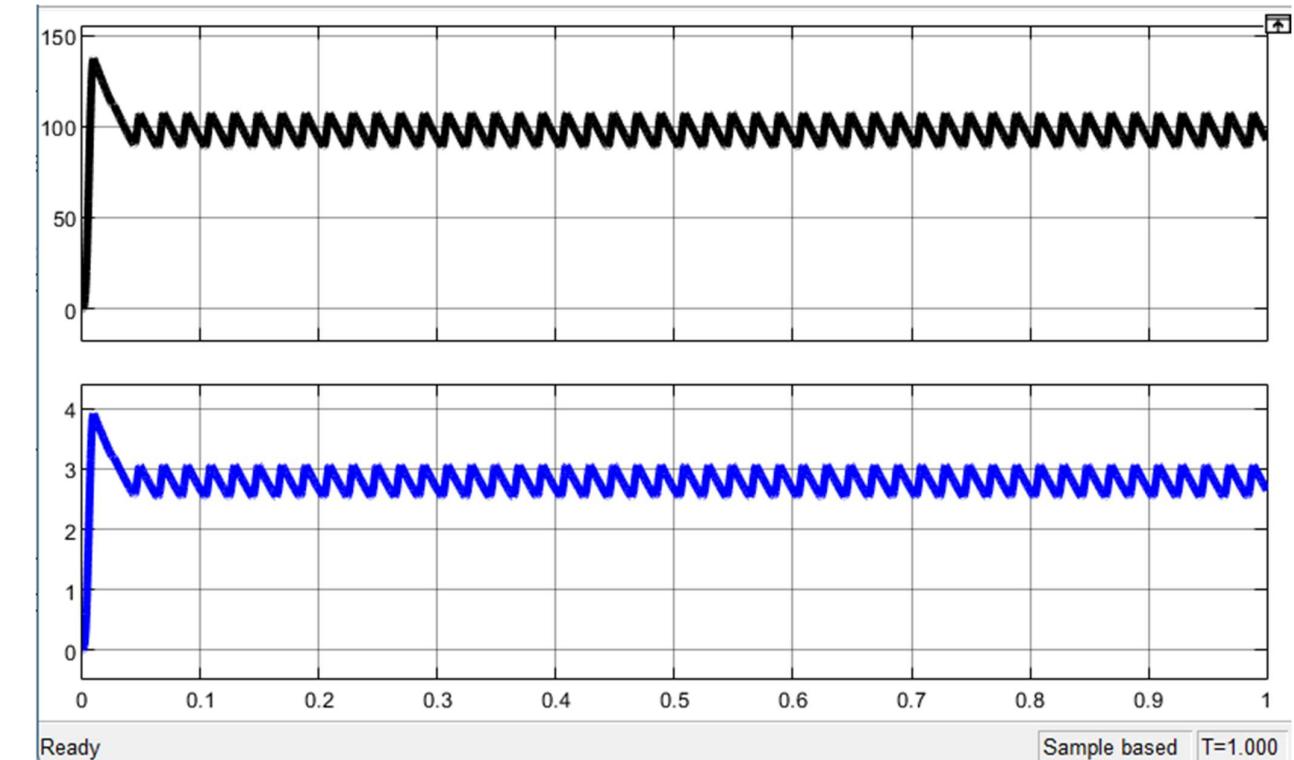


Fig 23. Output Voltage and Current Waveforms of Bridgeless SEPIC Bidirectional Switching PFC Rectifier

FFT Analysis:

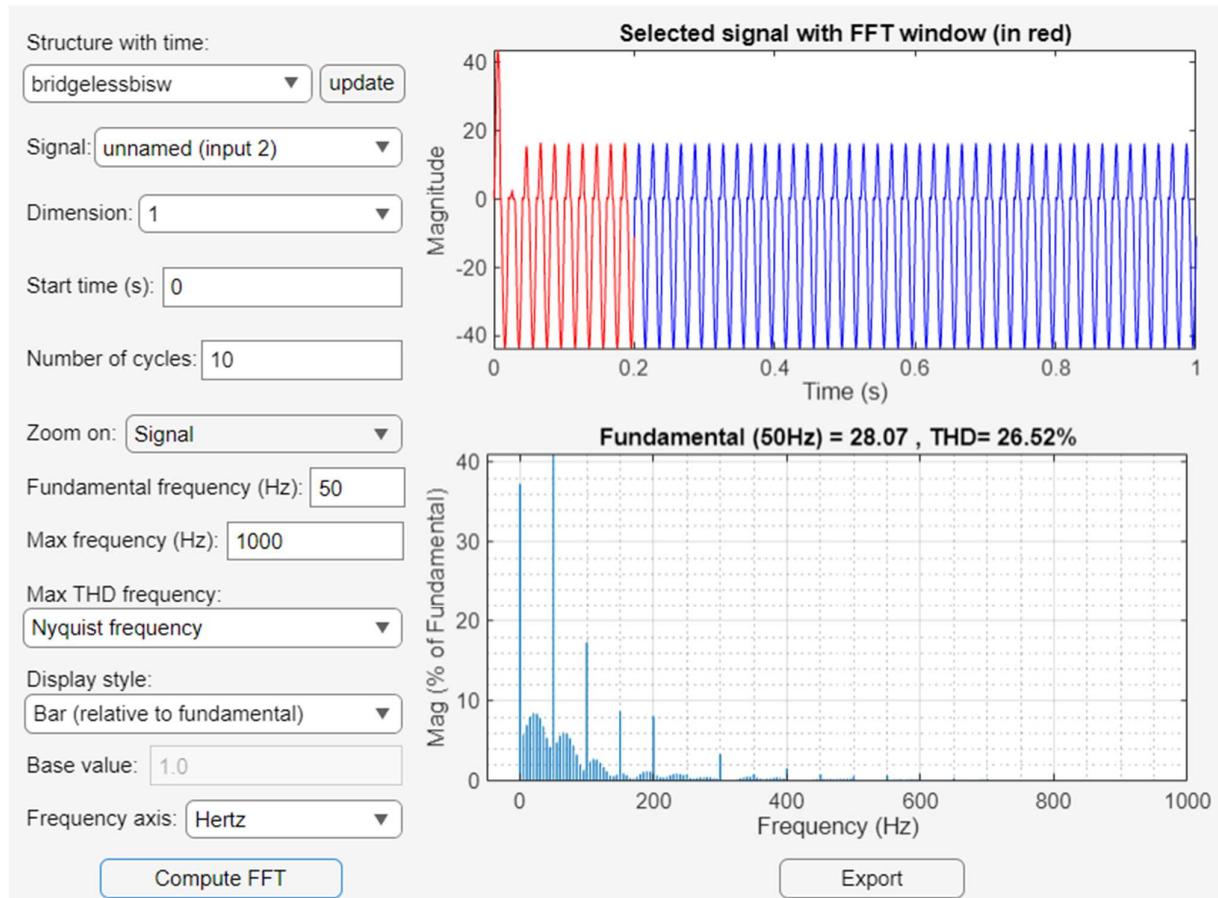


Fig 24. FFT Window of Bridgeless SEPIC Bidirectional Switching PFC Rectifier

Result and Comparisons:

SEPIC topology	Power factor	Input current THD
Conventional	0.7437	33.48%
Interleaved	0.9259	1.25%
Totem pole bridgeless	0.9246	4.26%
Pseudo totem pole bridgeless	0.8648	13.98%
New bridgeless SEPIC	0.9214	10.10%
Bridgeless Bi-directional switching PFC	0.7601	26.51%

The table presents a comparison of various SEPIC (Single Ended Primary Inductance Converter) topologies based on their power factor (PF) and input current Total Harmonic Distortion (THD). Among the configurations examined, the conventional SEPIC exhibits a respectable power factor of 0.7437 but suffers from a high input current THD of 33.48%, indicating significant distortion. In contrast, the interleaved SEPIC demonstrates improvements in both power factor and input current THD, boasting a PF of 0.9259 and a low THD of 1.25%. The totem pole bridgeless SEPIC maintains a high-power factor akin to the interleaved design but with a slightly elevated input current THD. Meanwhile, the pseudo totem pole bridgeless SEPIC achieves a good power factor yet exhibits a relatively high input current THD of 13.98%, hinting at potential inefficiencies. The new bridgeless SEPIC topology shows promise with a strong power factor of 0.9214 and a moderate reduction in input current THD compared to the conventional SEPIC. Finally, the bridgeless bi-

directional switching PFC topology, while featuring a decent power factor, displays a relatively high input current THD of 26.51%, indicating room for enhancement in efficiency and waveform cleanliness.

Overall, the interleaved SEPIC and the new bridgeless SEPIC configurations emerge as particularly noteworthy for their combination of high-power factor and low input current THD, suggesting superior efficiency and cleaner power conversion compared to the other topologies evaluated.

Conclusion:

- From this work it can be concluded that the input current is affected significantly because of the inductor and capacitor present in the SEPIC converter.
- Different topologies can be used to reduce the THD in the input current.
- The best topology for the given parameter is interleaved.
- Other topologies can also be used depending on the application

REFERENCES

- [1] A. V. J. S. Praneeth and S. S. Williamson, "A Review of Front End AC-DC Topologies in Universal Battery Charger for Electric Transportation," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, USA, 2018, pp. 293-298, doi: 10.1109/ITEC.2018.8450186.
- [2] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," in *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 873-881, March-April 2011, doi: 10.1109/TIA.2010.2102996.
- [3] K. Akter, G. Sarowar, M. A. Hoque and S. F. B. Ahmed, "Modeling and Simulation of Input Switched AC-DC SEPIC Converter with PFC Control for optimized Operation," *2018 4th International Conference on Electrical Engineering and Information & Communication Technology (iCEEICT)*, Dhaka, Bangladesh, 2018, pp. 240-245, doi: 10.1109/CEEICT.2018.8628168.
- [4] https://www.researchgate.net/figure/Positive-half-cycle-of-the-input-voltage-when-switch-S-is-off-Mode-2_fig2_336016915 (SEPIC open loop AC_DC)
- [5] [https://toshiba.semicon-storage.com/info/docget.jsp?did=68570#:~:text=A%20power%20factor%20correction%20\(PFC\)%20circuit%20reduces%20the%20harmonic%20distortion,factor%20to%20unity%20\(1\)](https://toshiba.semicon-storage.com/info/docget.jsp?did=68570#:~:text=A%20power%20factor%20correction%20(PFC)%20circuit%20reduces%20the%20harmonic%20distortion,factor%20to%20unity%20(1)).