**VLSI LAB REPORT: LAB 1**

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**LAB 1: INVERTER SCHEMATIC DESIGN & TRANSIENT SIMULATION**

**1. Introduction**

In this first lab, the main goal was to get familiar with the **Cadence Virtuoso** environment. I focused on designing the schematic for a standard CMOS Inverter using the gpdk090 technology node. After drawing the circuit, I performed a transient simulation using ADE L to verify if the logic works correctly and to measure key performance metrics like propagation delay and power consumption.

**2. Design Procedure**

Library Setup

I started by creating a new working library named mylib. To make sure I had access to the correct devices, I attached this library to the technology file gpdk090 1.

Schematic Entry

For the inverter design, I used two transistors from the library: nmos1v and pmos1v.

* **Sizing:** I set the **NMOS width to 240 nm** and the **PMOS width to 480 nm**, keeping the length at 100 nm for both. I chose the PMOS to be twice as wide as the NMOS to balance the rise and fall times, compensating for the lower mobility of holes compared to electrons.
* **Connections:** I connected the gates together to form the input (in) and the drains to form the output (out). The body terminals were connected properly to the supply rails (NMOS to gnd, PMOS to vdd) 2.

A computer screen shot of a computer

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**3. Simulation & Results**

Setup in ADE L

To run the simulation, I launched the Analog Design Environment (ADE L).

* **Model:** I selected the gpdk090.scs model file and chose the **TT\_s1v** (Typical-Typical) section to simulate standard operating conditions 3.
* **Stimuli:** I set up a global DC voltage source (vdd!) at **1.2 V**. For the input pin, I configured a Pulse source with a period of 40 ns and rise/fall times of 3 ns4.
* **Analysis:** I ran a **Transient analysis** for a duration of **100 ns**5.

Transient Response

The simulation ran successfully. As shown in the waveform below, the output (out) clearly inverts the input signal (in), confirming the correct logic behavior of the NOT gate.

Measurements

Using the Waveform Calculator, I extracted the following data:

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* **Propagation Delay (Tp):** I measured the delay at the 50% voltage threshold (0.6V).
  + Measured value: 109.2 ps
* **Average Power:** By averaging the power signal (:pwr) over the simulation time, I found the power consumption.
  + Measured value: 1.838 uW.