Concepts in VLSI Design Laboratory

EE121IU

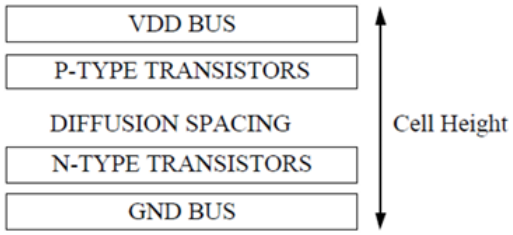
Instructor: Nguyen Binh Duong

A. Introduction to Layout, DRC and LVS

- Layout is representation of a circuit in terms of planar geometric shapes (e.g. rectangles, polygons) showing the patterns of metal, polysilicon, oxide, or diffusion layers that make up the components (resistors, inductors, capacitors, transistors) of the integrated circuit.

- When using a standard process (e.g. 45nm, 90nm or 180nm process available in our lab), the behaviour of the final integrated circuit depends significantly on the positions and interconnections of the geometric shapes due to parasitic resistances and capacitances contributed by them. While designing a layout, designer must keep in mind performance (e.g. power-delay product) and size (area occupied by the chip) criterion.

- While designing digital circuits, one usually follows an ASIC design flow, where, the height of standard cells that are used is the same throughout the cell library, but their widths must vary according to their logical functions and drive strengths. The following figure shows a generalized standard cell height concept:



Although we will follow a full-custom IC design flow, we will maintain same cell height throughout our cell library.

The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are:

- Design Rule Checking (DRC)
- Layout Versus Schematic (LVS) checking
- Parasitic extraction and post-layout simulation

Design Rule Check (DRC):

Design Rule Checking (DRC) is the process that determines whether the designed layout of a circuit satisfies a rules specified by the process being used.

Design Rules are a series of rules (e.g. area, width, overlap, enclosure, extension, spacing) provided by semiconductor manufacturers which are specific to a particular semiconductor manufacturing process. Design rules specify certain geometric and connectivity restrictions to ensure that the process can fabricate the device properly.

Layout versus Schematic (LVS) Check:

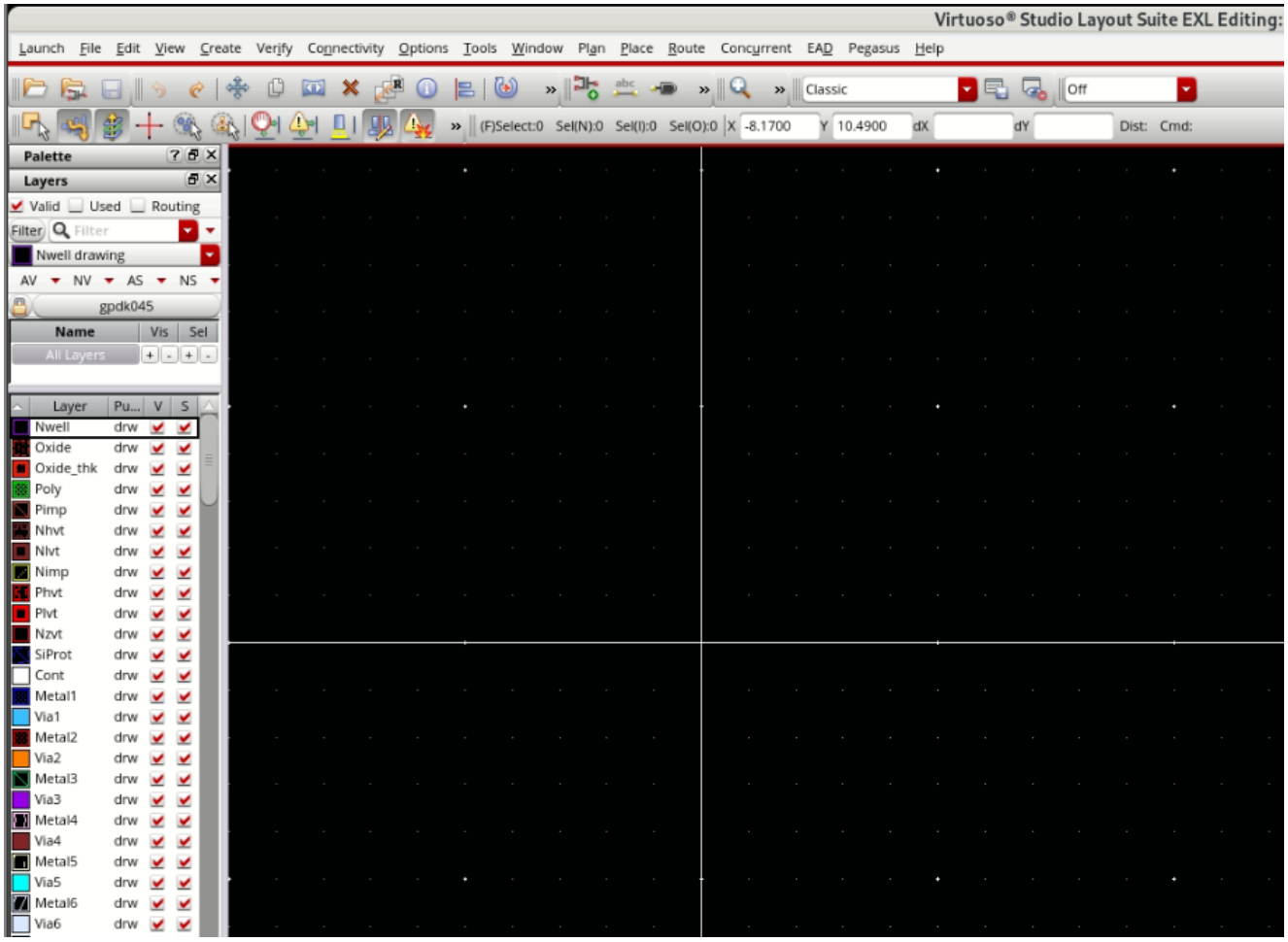
The Layout Versus Schematic (LVS) is the verification step to determine whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. A successful Design rule check (DRC) ensures that the layout conforms to the rules designed/required for faultless fabrication. However, it does not guarantee if it really represents the circuit we desire to fabricate. This is why an LVS check is used.

B. Layout design using Virtuoso Layout Suite EXL Editor

Invoke **Virtuoso Layout Suite EXL Editor** from the **CIW** by executing ***File*** -> ***New*** -> ***Cellview***. The '**New File**' form appears. Fill it in as shown in the figure below:

Cell: <*your_inverter_schematic _name*>, **View:** *layout,* **Open with:** *Layout EXL*. Click **OK**.

The following window of **Virtuoso Layout Suite L Editor** will appear.

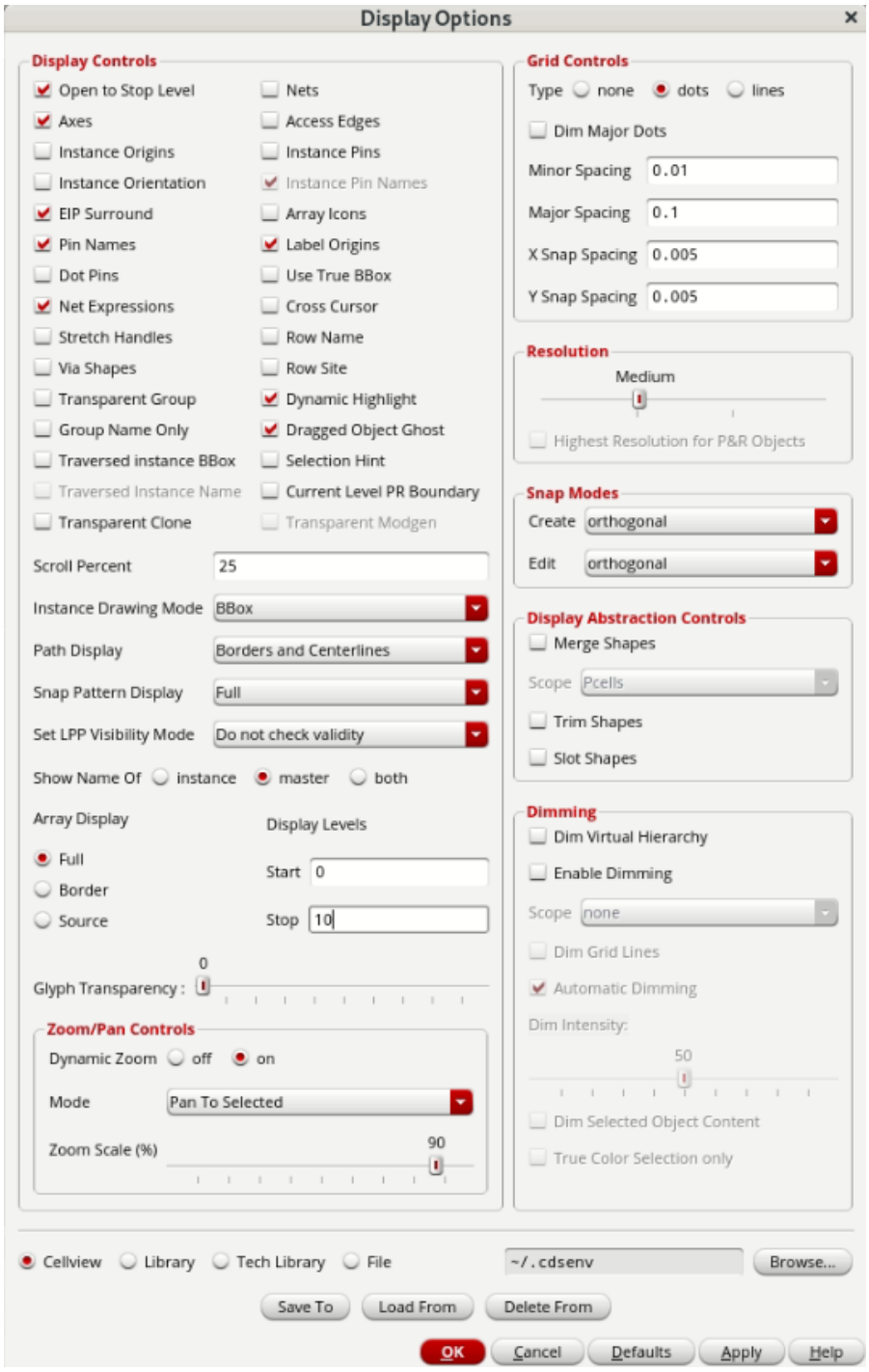


On the left side of the window, you will find a panel called 'Layers'. This panel is divided in three main categories which are: layer color, layer name and layer purpose. The details are described in the table below:

Color	Matches the color in the Editing window. Each layer has its own color and pattern. Each layer has two colors associated with it: a fill color and an outline color. These colors can be changed to fit your taste by editing the technology file.
Name	The type of layer (Nwell, Oxide, Poly, Metal1, etc)
Purpose	In gpdk045 the only purpose classifications are: drw = drawing, slot = slot Drawing is used in layout, slot is used to create a hole for metal stress relief

Verify that the layers display corresponds to the gpdk045 layers shown in the GPDK 45 nm Mixed Signal Process Specification manual (gpdk045_drc.pdf).

1. Before starting to design layout, you need to set the layout display configuration. Execute the following in the Virtuoso Layout Editor: ***Options -> Display*** or press '**e**' on keyboard. Configure the form as shown in the figure below: You have to set the following parameters only:



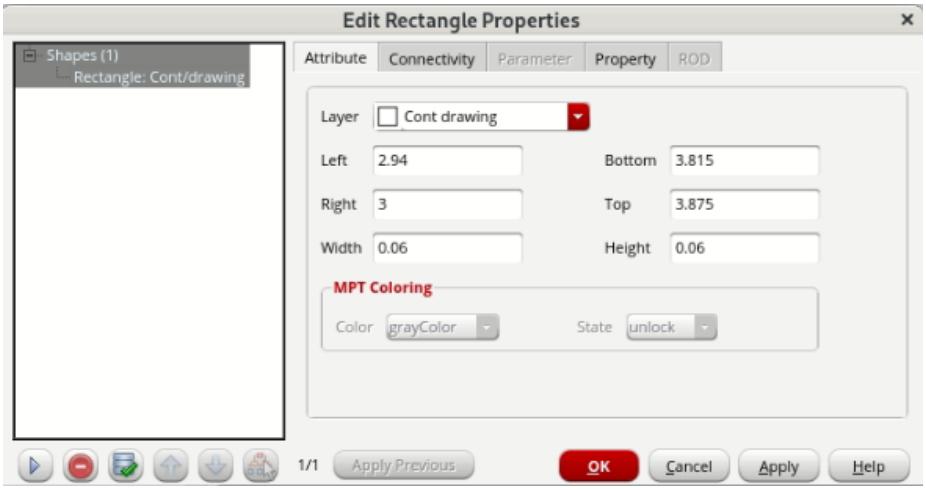
2. Now we are going to build the layout of the inverter. An inverter has an NMOS and a PMOS transistor. First we will build an NMOS transistor.
   Layout of NMOS inverter consists of oxide, Nimp, Cont and Poly layers. Study the rules of these layers and calculate the minimum size of the Poly, Cont, Oxide and Nimp layer to create an NMOS transistor. The rules related to the NMOS transistor can be summarised as follows:

Contact size	0.06 µm x 0.06 µm (Fixed)
Poly width (Minimum)	0.045 µm (Fixed MOS gate length)
Contact to poly spacing (Minimum)	0.05 µm
Contact to oxide enclosure (Minimum)	0.03 µm
Poly/Nimp extending from oxide (Minimum)	0.07 µm
Nimpenclosing oxide (Minimum)	0.14 µm
Minimum Metal 1 width	0.06 µm
Maximum Metal 1 width	6.0 µm

Now we start building the NMOS and PMOS transistor layout. Look at the LSW and find the current drawing layer.

3. Click on the following icon in **Virtuoso Layout Suite EXL Editor** window so that it notifies you anytime you make a violation of any design rule. When clicked, it will show '**DRD Notify ON**'. DRD stands for Design Rule Driven.

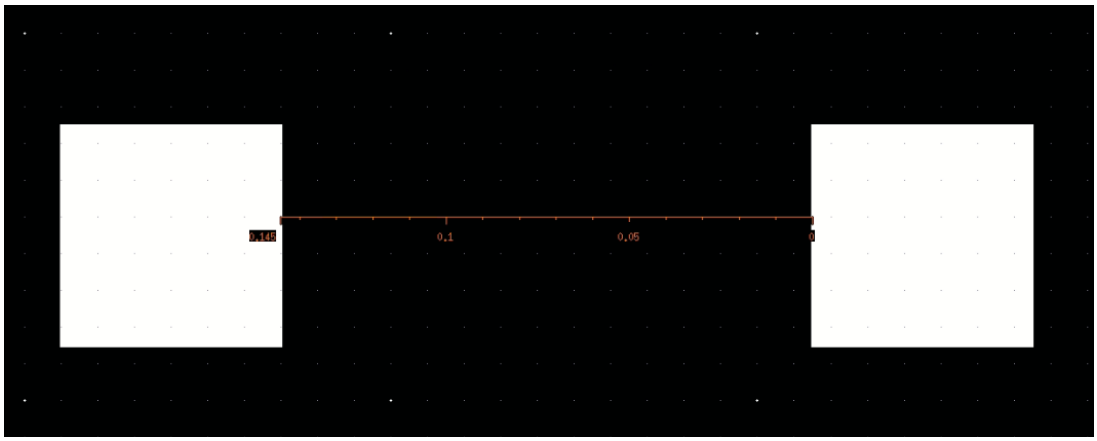
4. Select '**Cont (drw)**' (contact) layer from the '**Layers**' panel and draw a rectangle of '**Cont (drw)**' layer using Create -> Shape -> Rectangle or simple pressing '**r**'. Press '**Esc**' to stop '**create rectangle**' tool. In gpdk045 technology, Cont layers must be of dimension **0.06 µm x 0.06 µm**. So, if your rectangle is not of that dimension, click on the rectangle, press '**q**'. In the following window, check if the criterion has been met and change '**Width/Height**' if required.



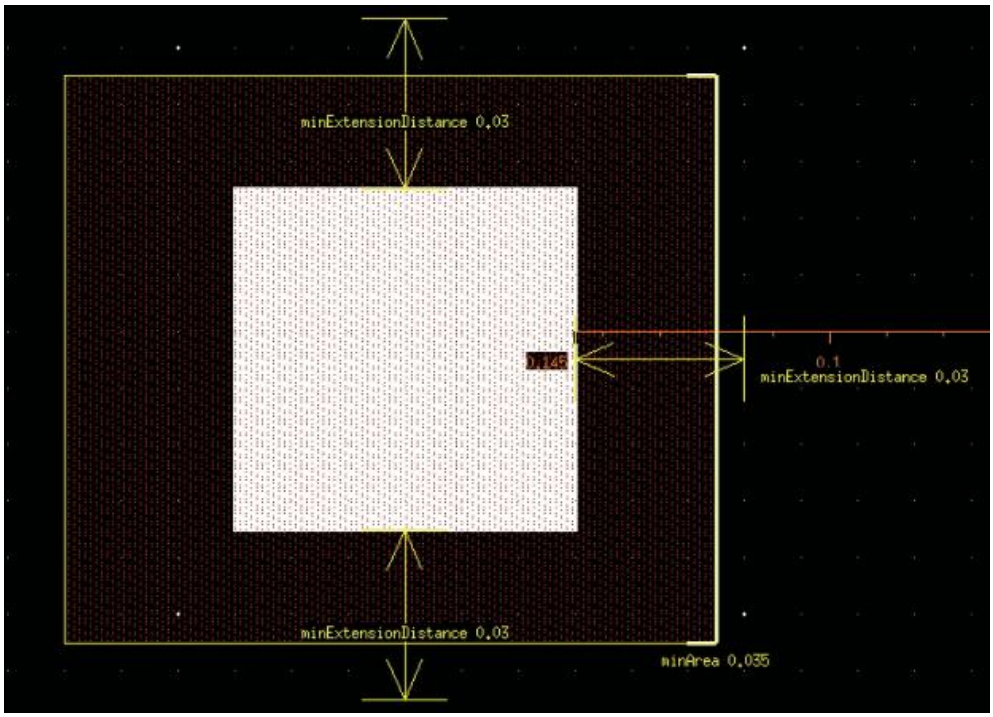
Now we start building the NMOS and PMOS transistor layout. Look at the **LSW** and find the current drawing layer.

Contact to poly spacing must be **0.05 µm** in this technology and the **channel length** of NMOS/PMOS in our design is **0.045 µm**. So, we need a minimum space of **0.145 µm** between the contacts at source and drain.

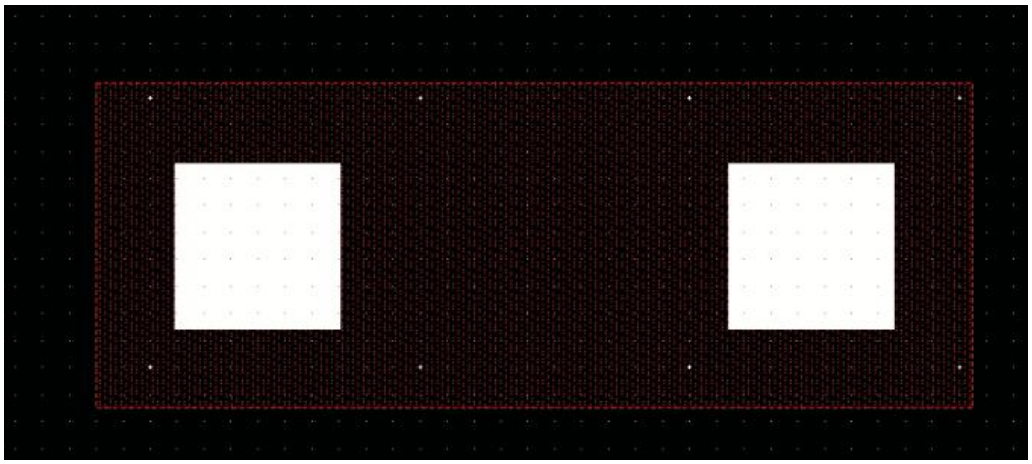
5. Press '**k**' to invoke the '**ruler**' tool. Use it to measure lengths whenever needed. To copy, press '**c**'. After placing two contacts, the layout looks like this:



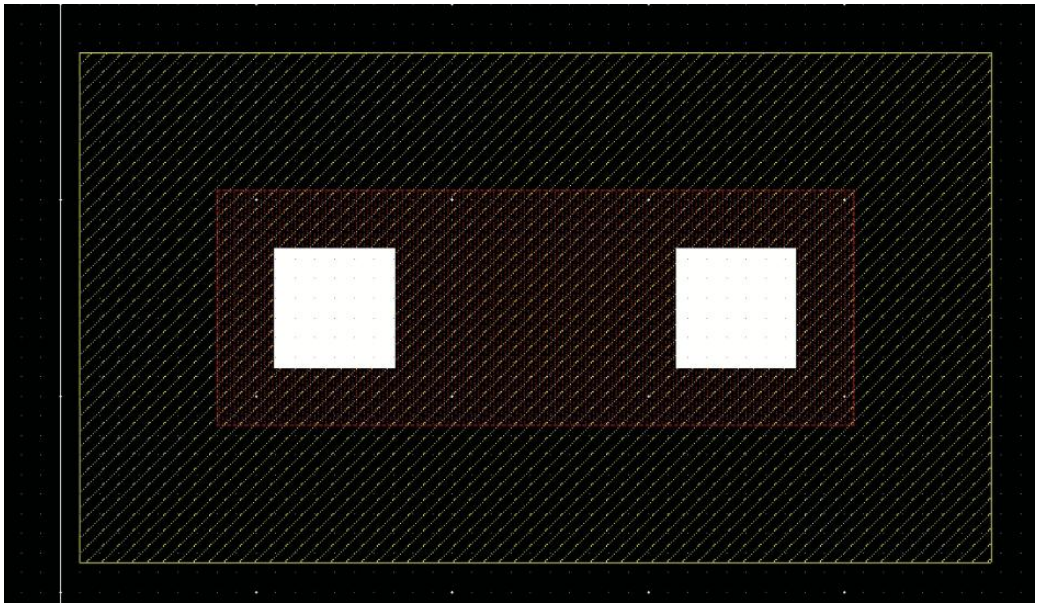
6. Now, **contact to oxide spacing** is minimum **0.03 µm**. So, draw a rectangle of 'Oxide (drw)' layer so that it covers both the contacts and extends from each side by **0.03 µm**. While drawing this, you will see Design rule violations when they are committed.



7. After drawing oxide layer, the layout should look like this:

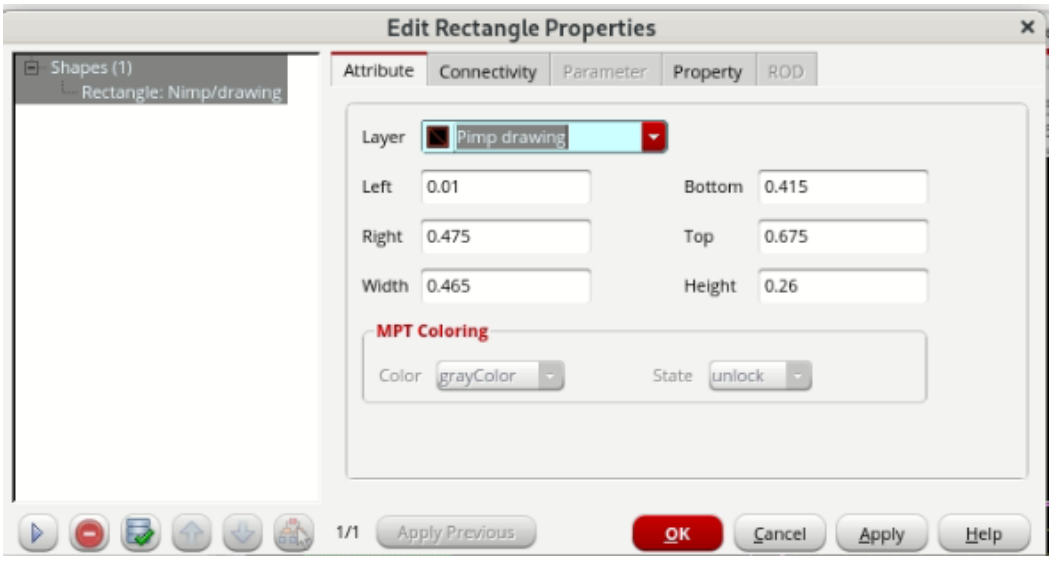


8. Now we will draw '**Nimp (drw)**' layer, which must extend from the oxide layer by a minimum of 0.07 µm. First, draw a rectangle and then extend it to meet design rules. Use stretch tool by pressing '**s**'. Layout will look like the following:

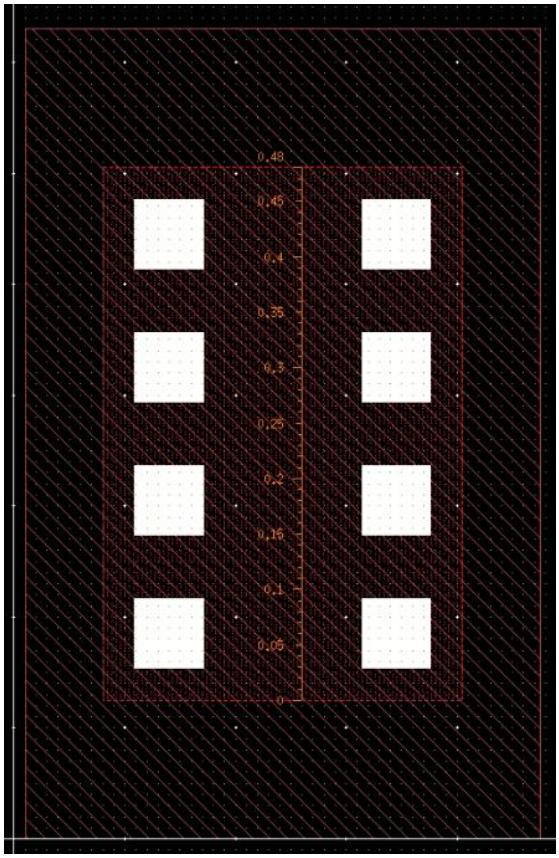


9. Now, copy it and create another copy of all these layers by selecting all and pressing '**c**'.

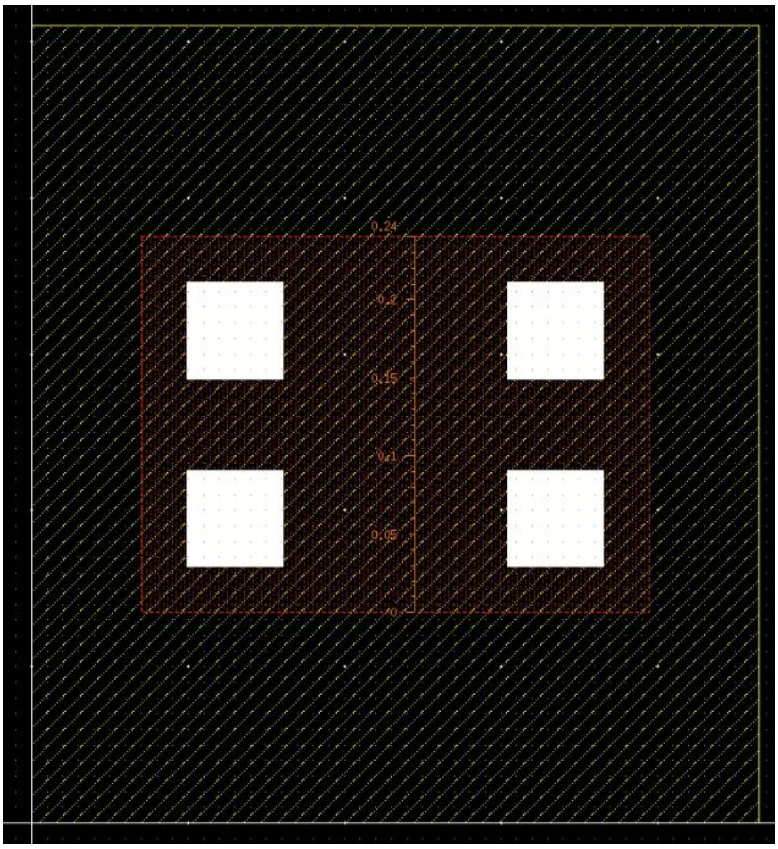
10. Click on the '**Nimp (drw)**' layer of the copy in the upper portion of the layout and press '**q**' to edit properties. From '**Edit Rectangle Properties**' window, select '**Pimp (drw)**' layer under '**Layer**' option. Click **OK**.



11. Above is basic steps to create a simple NMOS/PMOS. However, this process is incomplete as it omits the critical **physical design parameters**: the transistor's **Length (L)** and **Width (W).** Failing to define these dimensions correctly will inevitably lead to Design Rule Violations (DRC), as the layout will not comply with the technology's manufacturing constraints. You should design your NMOS/PMOS like this to cover this issue.
    Below is the 480n width PMOS:

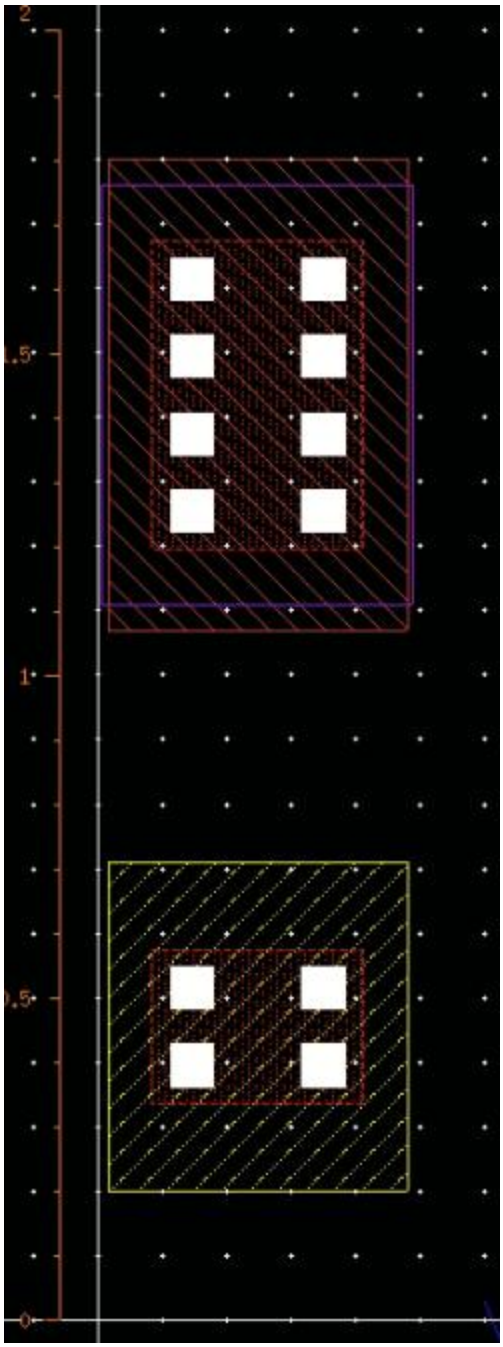


Do the same with NMOS (width = 240):

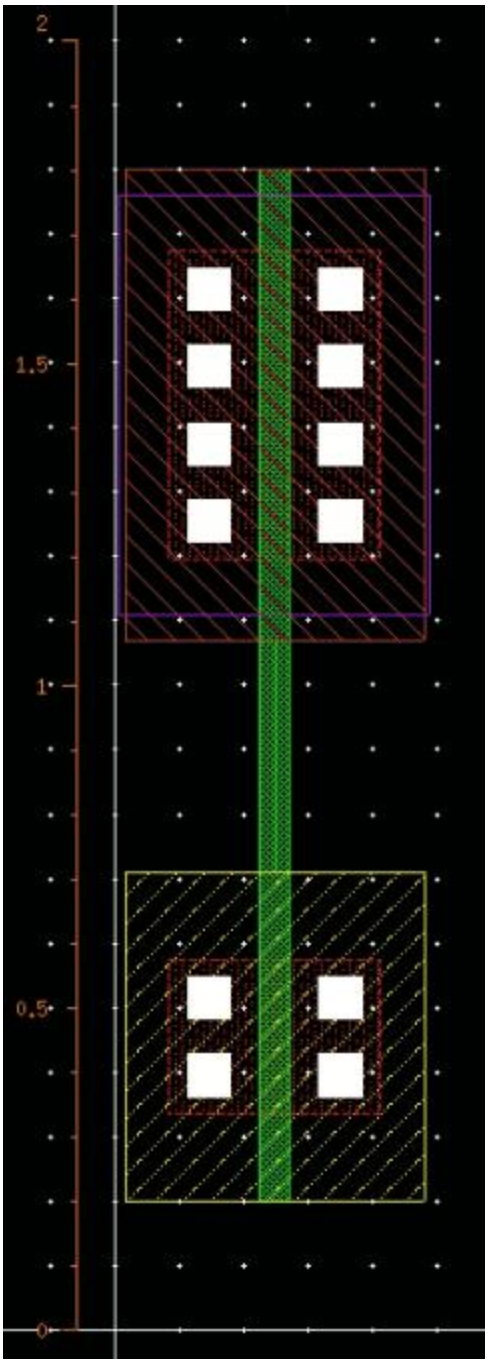


12. With more metal layers available in today's silicon processes, using the routing approach, such as first metal traverse vertically and second metal traverse horizontally, would be advantageous in standar cell physical design. Using this method, the second layer (e.g. Metal2) can be used for power and ground routing over internal standard cell transistors. In standard cell layout, it is preferable to use firt conducting layer, such as Metal1, as much as possible to make internal connections of NMOS and PMOS transitors within the cell. If there is a nedd to use other conducting layers, such as, Metal2, use of such layers must be kept to a minimum. It is desired to use first routing (e.g. Metal1) layer for standard cell ports.

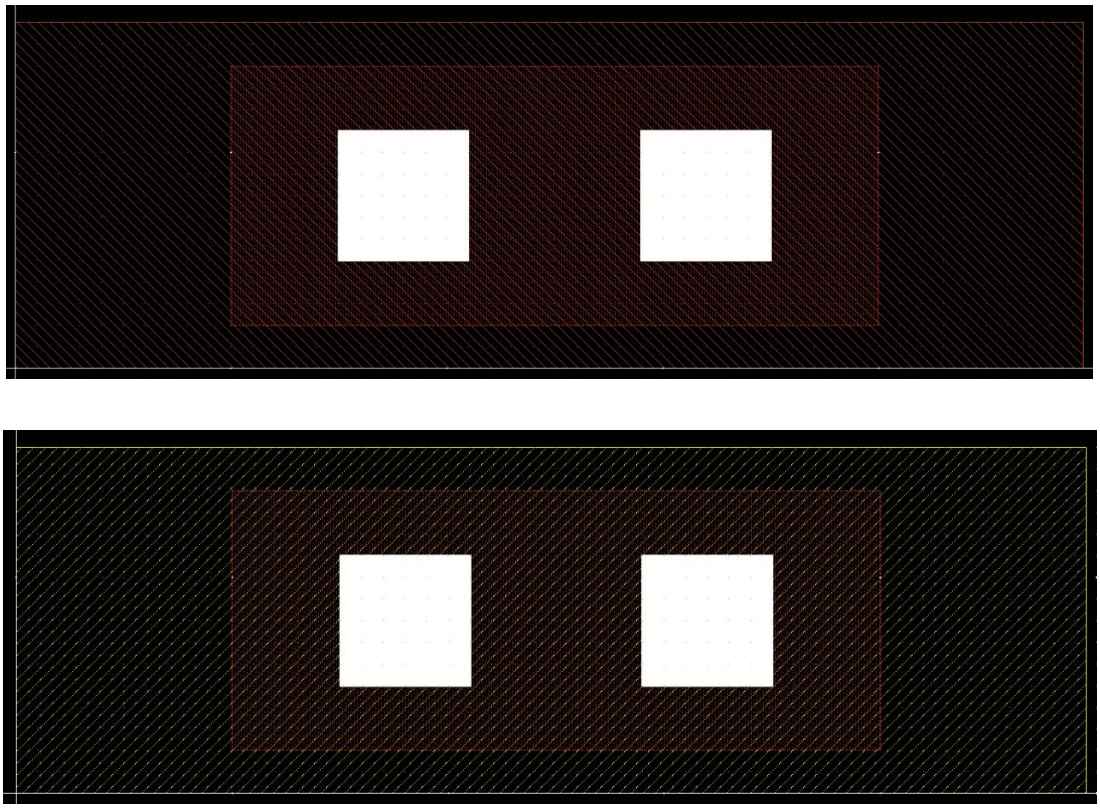
13. Our cells will have a height of 2 µm. Place the two parts (NMOS and PMOS) and create a ruler so that the cell height can be checked whenever needed and the separation between the NMOS and PMOS can be maintained properly. Now, the layout will look like the following:



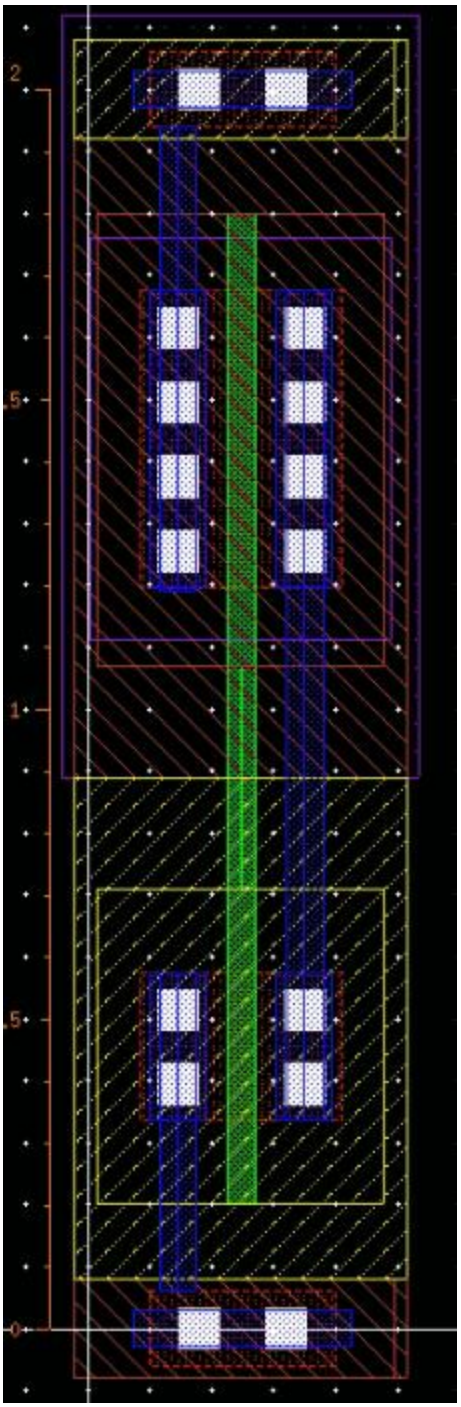
14. Next, draw a '**Poly (drw)**' path by selecting '**Poly**' layer from the '**Layers**' panel and pressing '**p**' to invoke '**create path**' tool. This layer must be of **0.045 µm** in width and in between the two contacts, extending from the oxide layer by 0.07 µm (at least, on both sides). After placing the 'poly' gate, the layout will look like the following one:



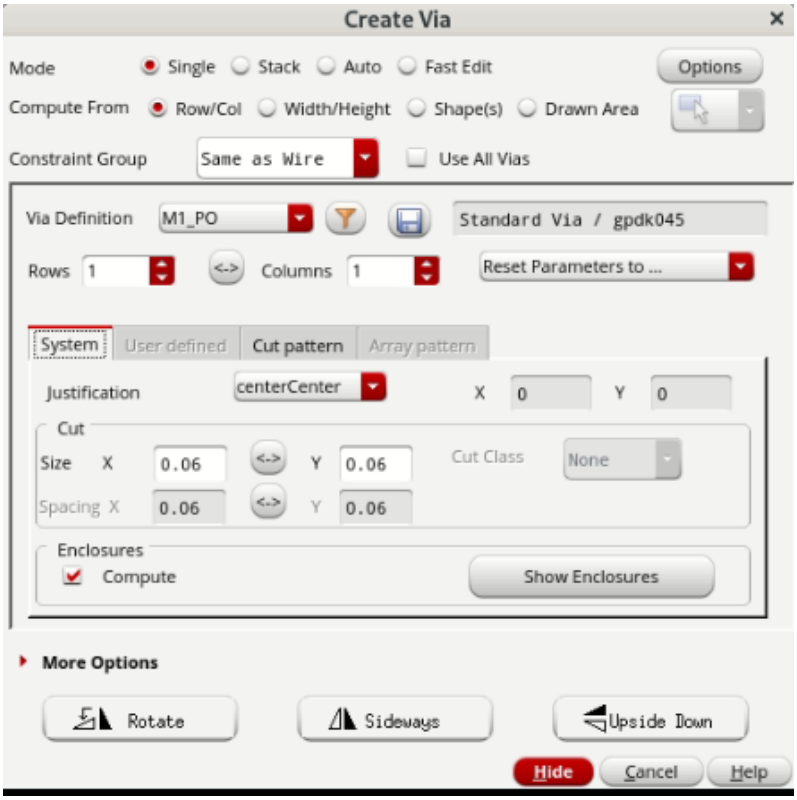
15. Now that you know most of the shortcuts and layers, draw contact for body terminals for NMOS and PMOS. These portions should consist of Cont, Oxide and Nimp (for body of PMOS) or Pimp (for body of NMOS). Check DRD notifications for design rule violations. The following figure shows a Psubstrate and an Nwell contact. The measurement dimensions are shown only on the left one, as they are same for both contacts. Note that, more vias -> more stable signal at the output



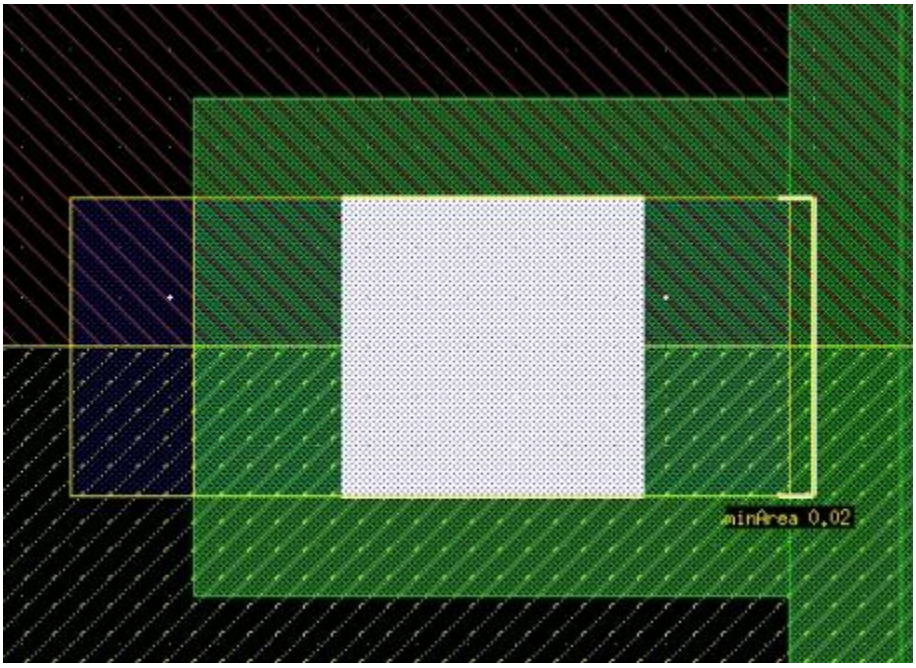
16. Connect the Drain regions of the NMOS and PMOS. Also connect the source of both MOS's to respective body terminals using '**Metal1 (drw)**' layer. Connect the drains of the MOS's using '**Metal1 (drw)**' layer.
17. PMOS should be in '**Nwell (drw)**'. So draw an '**Nwell (drw)**' rectangle surrounding both the PMOS and the body contact for PMOS. You should divide the area of NIMP and PIMP almost equally. The layout will look like the following:



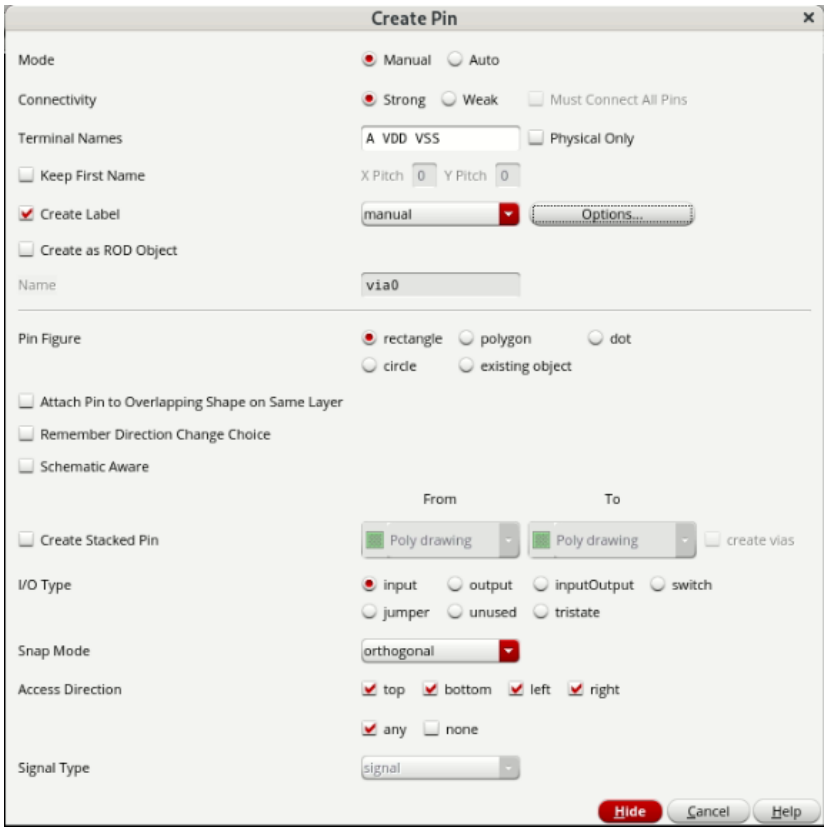
18. Now, we have to place pins. The gate is in '**poly (drw)**' layer. Let's bring it to '**Metal1(drw)**' layer by extending the '**Poly (drw)**' layer, creating a contact between '**Poly**' and '**Metal1**' layer by pressing '**o**' to '**create via**' and selecting '**M1_POv**' under '**via definition**' and placing it on layout.



19. Also draw a 'Metal1 (drw)' rectangle on the via, because the default Metal1 rectangle area is less than the required minimum. However in real design, you can skip this since input and output will connect with other circuit and it will solve this issue.

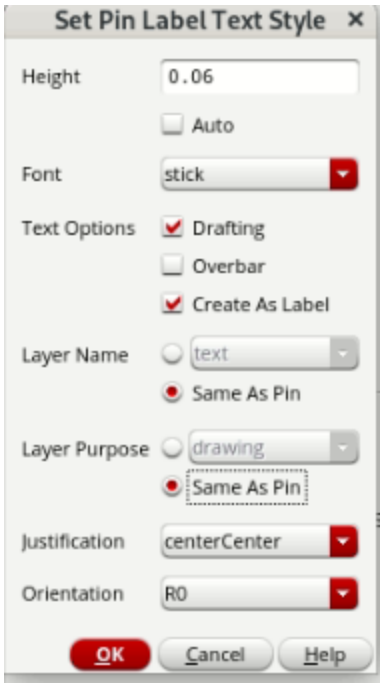


20. Now, Execute **Create-> Pin** to create pins for **VDD**, **VSS**, **A** and **Y**
    For **A**, **VDD** and **VSS** select '**input**' as '**I/O type**' and for **Y** select '**output**' as '**I/O type'**. Now, draw rectangles on the **Poly-Metal1** via for '**A**' pin, PMOS source-to-body '**Metal1**' connection for '**VDD**' pin and NMOS source to-body connection for '**VSS**' pin. For '**Y**' pin, draw the rectangle on the **Metal1** layer connecting the two drains of MOS's.

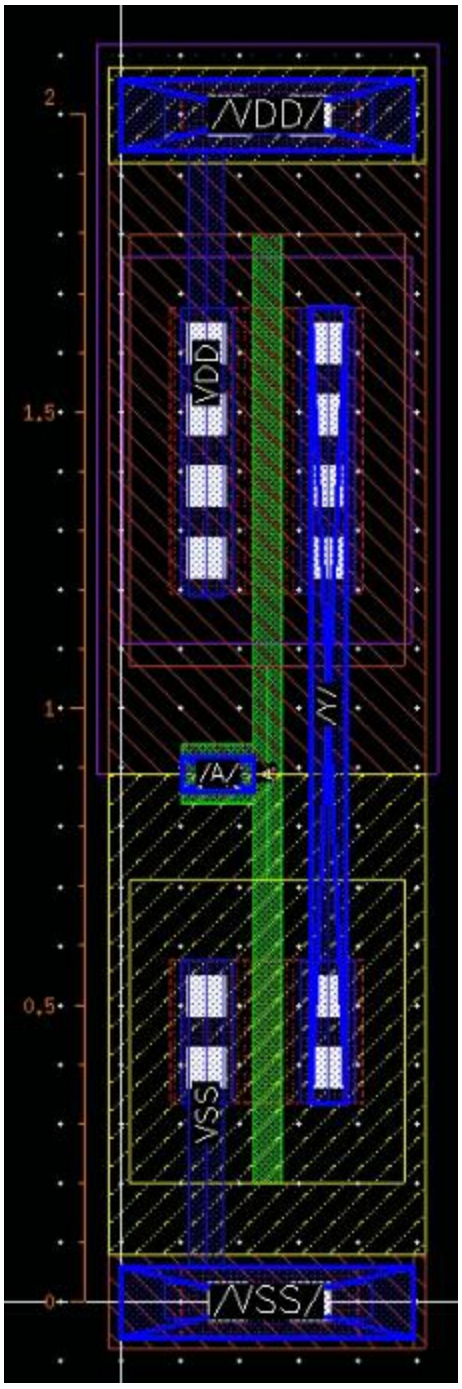


Remember to change the layer of the pin you just create to pin by right click on the pin -> press '**q**' then change the layer of the pin from '**metal 1 drawing**' to '**metal 1 pin**'

Check the **Create Label** box and choose **options**, then you can set up the label for the design

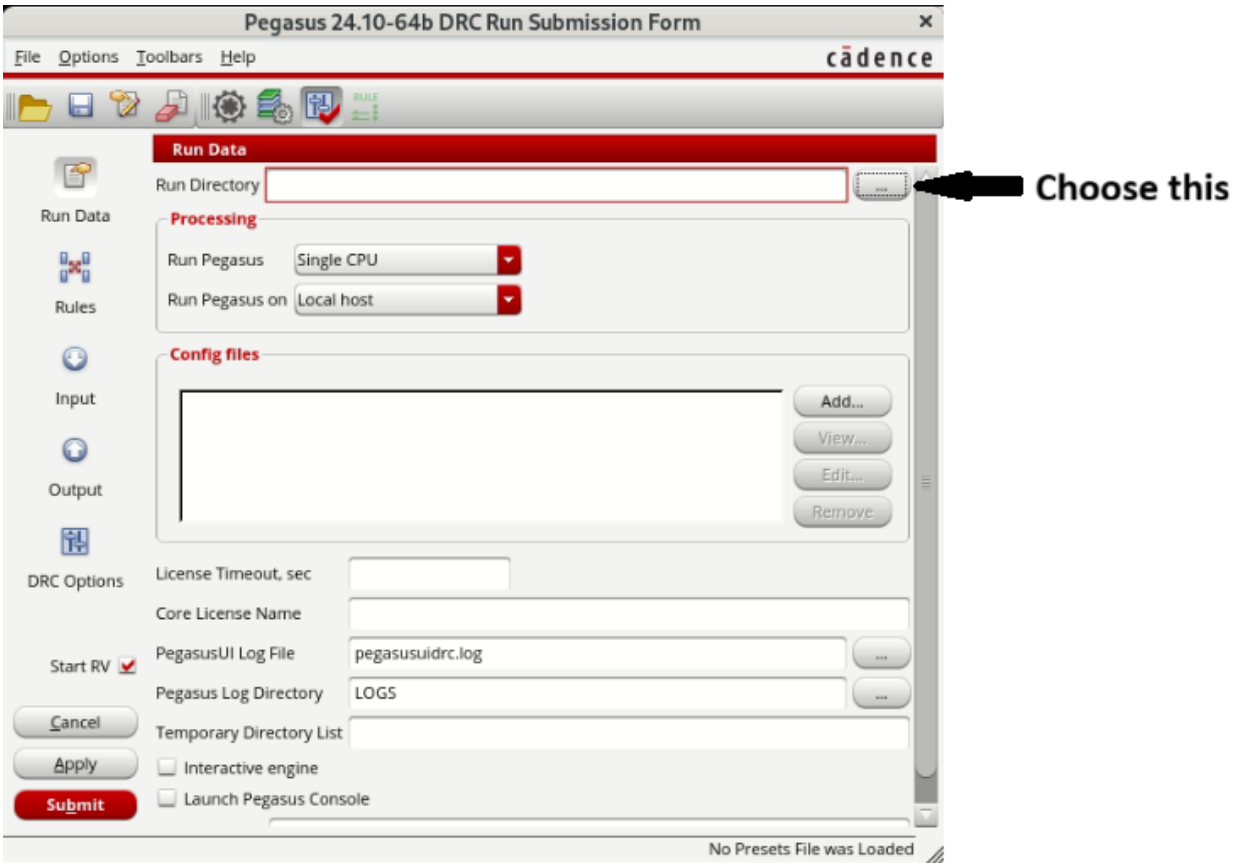


21. The final layout should look like this:

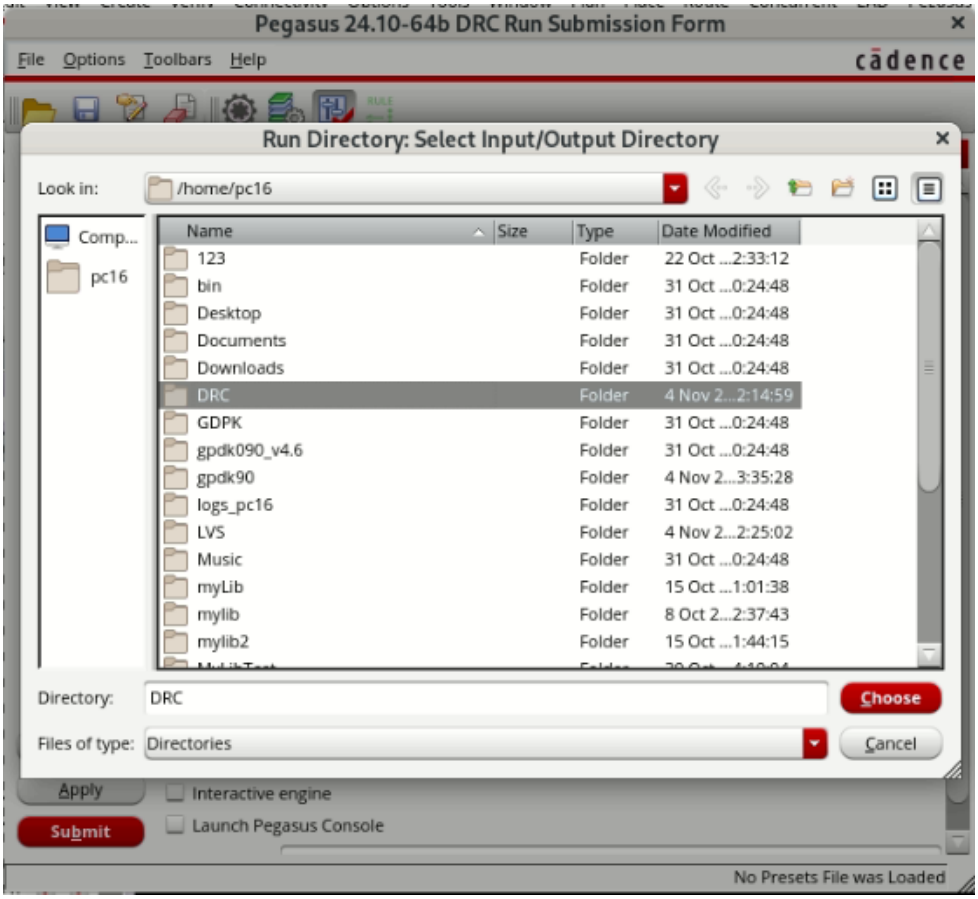

2
1.5
1
0.5
0
VDD
VDD
A
VSS
VSS

C. DRC Rules check by Cadence's PEGASUS

1. Now we would like to check the DRC rules by PEGASUS. Execute Pegasus → Run DRC. In the Following window, choose Run Data and set up your run directory.

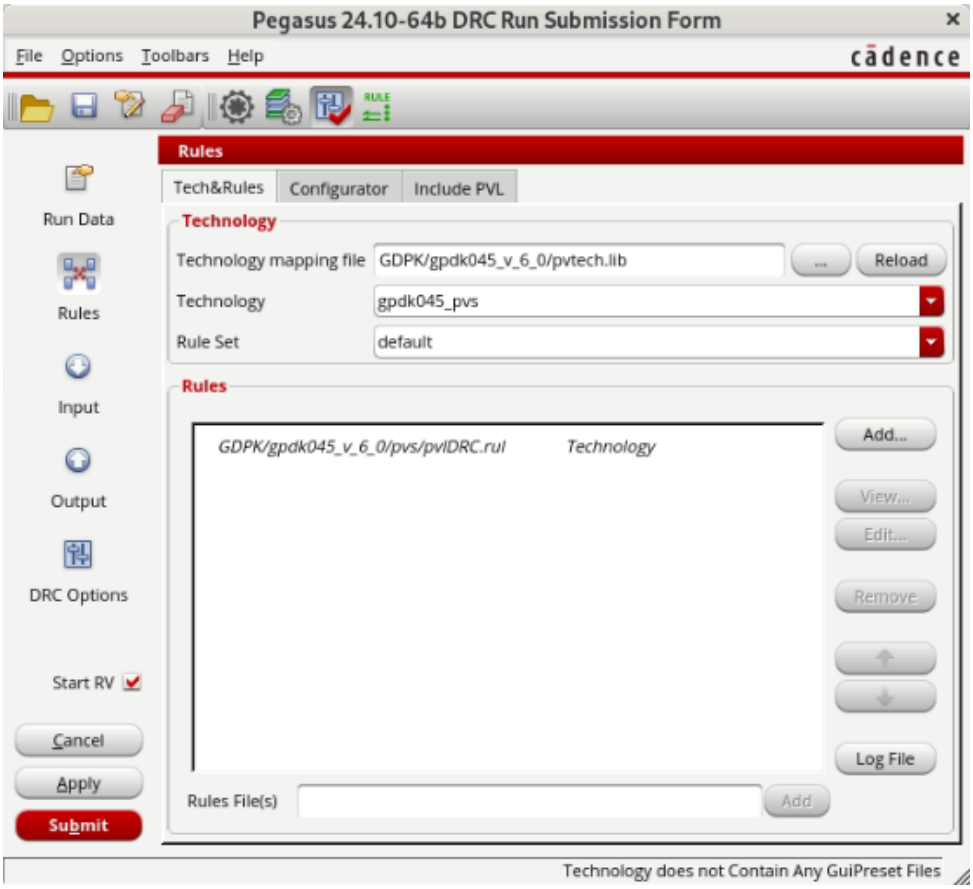


You can create a new folder and name it yourself (DRC, DRC_check…)

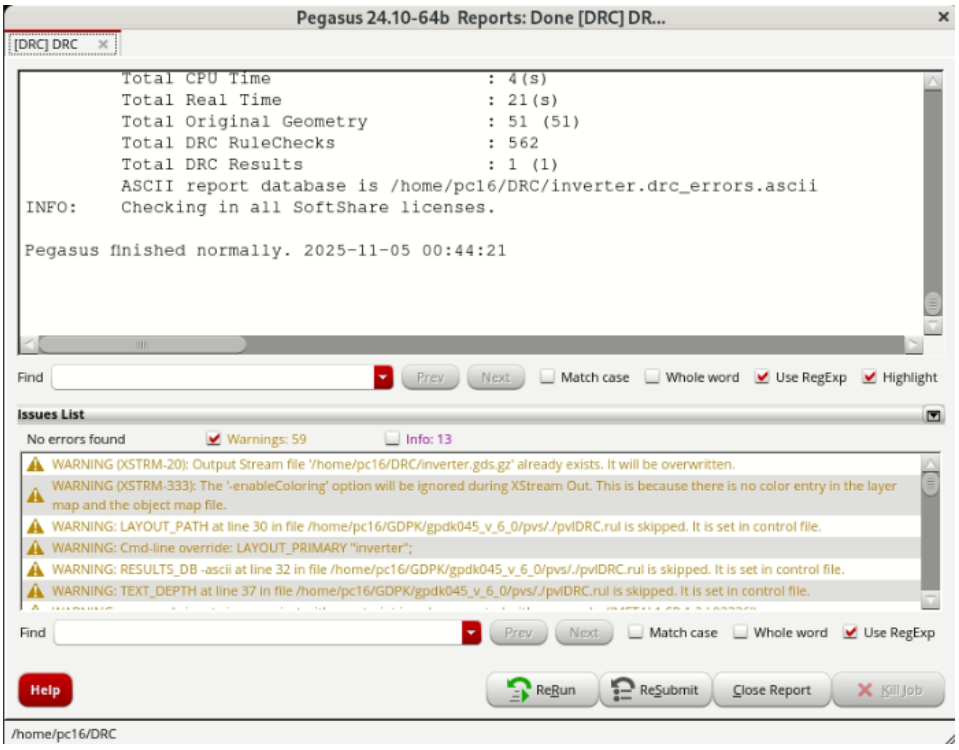


Press Choose and your result now will be stored in that directory.

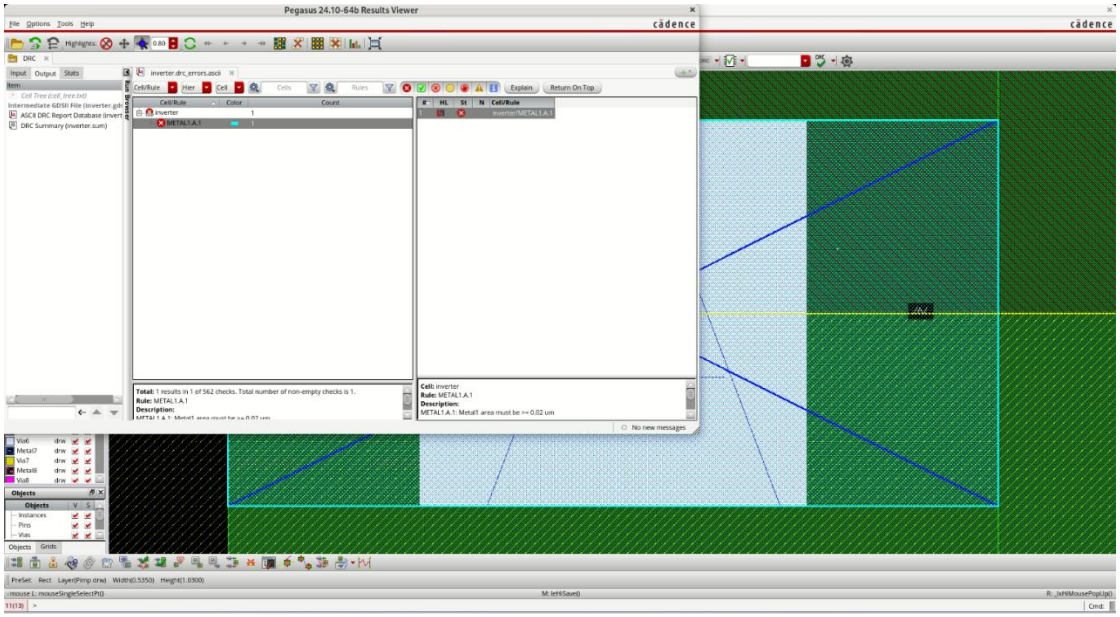
2. Navigate to Rules and set up as indicated in the picture below. Then click **submit**



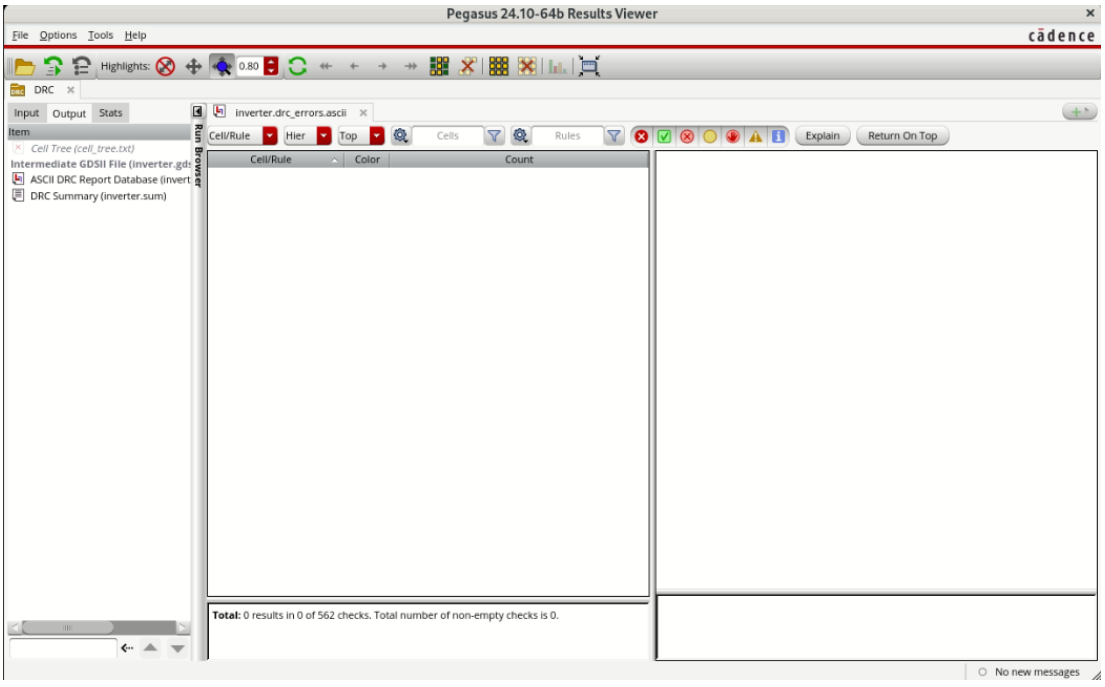
3. DRC window will look like this after completion of DRC run.



Then Result Viewer window will now appear, and you can choose the error to locate the error



After fixing the error, you can click **ReRun** on DRC window to run the DRC check again. If your design is error free, your Results Viewer will look empty like this



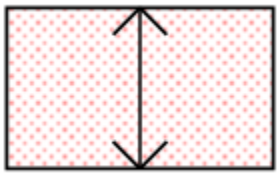
NOTE: You can open the list of DRC error code by reading gdpk045_drc.pdf which is located at ..\gpdk045_v_6_0\docs

Appendix A (Shortcut keys for Cadence Virtuoso ® Layout Editor L)

Shortcut Key	Tasks performed
f	Fit display to window
r	Draw rectangle
q	Edit property of an object
p	Makes a min width path of the layer selected in LSW
Ctrl+a	Select all
Ctrl+d	Deselect all
c	Copy
m	Move
s	Stretch side of a rectangle
k	Invoke ruler tool
Shift+k	Delete all rulers
i	Add an instance
u	Undo
Shift+u	Redo
e	Display options
o	Add via between layers
l	Create a label

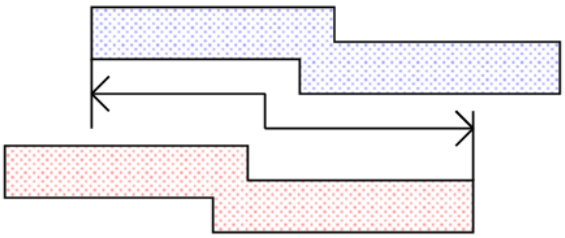
Appendix B (gpdk090 Design Rules Guide (Abridged Version for VLSI-I Lab)) Terminology Definitions

Width - shortest distance from the inside of the edge of a shape to the inside of the edge of the same shape.

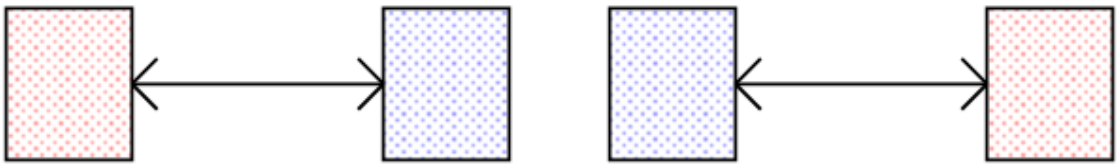


Length - opposite of Width - the measurement of the longest edge of a shape.

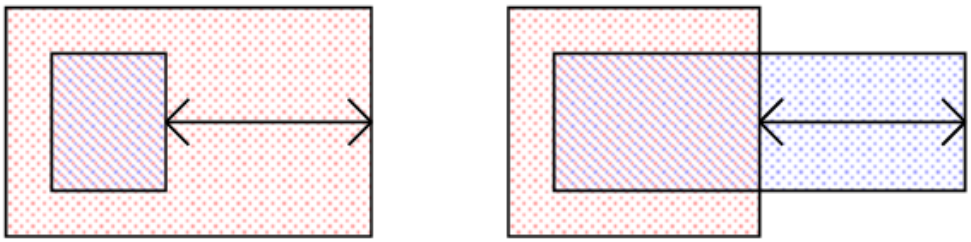
Parallel Run Length - the distance two shapes maintain a spacing less than the check value.



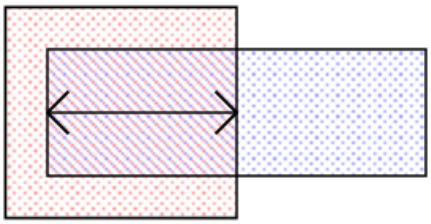
Spacing - distance from the outside of the edge of a shape to the outside of the edge of another shape.



Enclosure - distance from the inside of the edge of a shape to the outside of the edge of another shape.



Overlap - distance from the inside of the edge of a shape to the inside of the edge of another shape.



Butting - outside of the edge of a shape touching the outside of the edge of another shape.