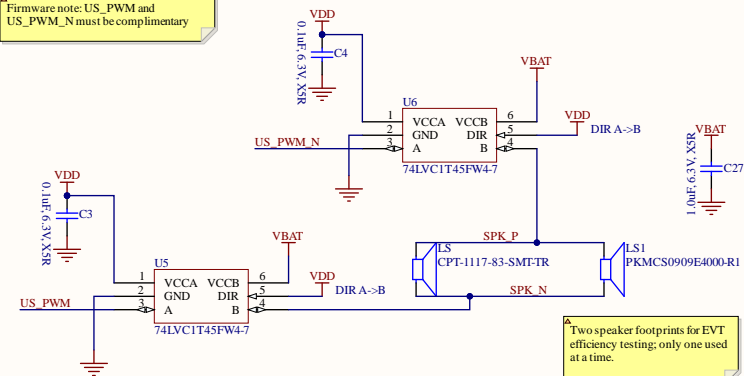
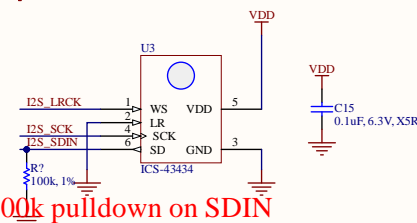


[illegible]

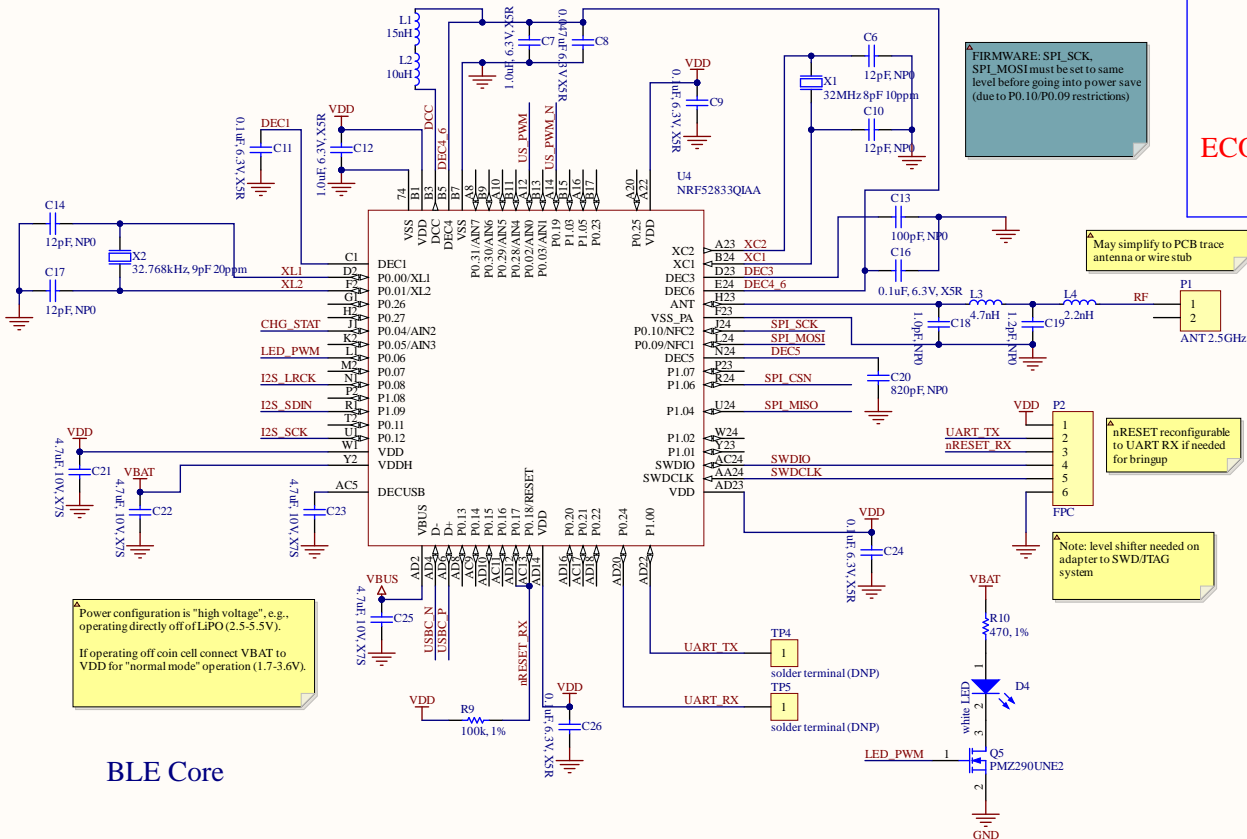
Firmware note: US_PWM and US_PWM_N must be complimentary




ECO: 100k pulldown on SDIN



FIRMWARE: SPI_SCK, SPI_MOSI must be set to same level before going into power save (due to P0.10/P0.09 restrictions)



 nRESET reconfigurable to UART RX if needed for bringup

Note: level shifter needed on adapter to SWD/JTAG system

Power configuration is "high voltage", e.g., operating directly off of LiPO (2.5-5.5V).

If operating off coin cell connect VBAT to VDD for "normal mode" operation (1.7-3.6V).

[illegible]

Configured as legacy USB device only support.

USB-A with PCB-as-connector option also being considered.



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Title Simmel		
Size A3	Number	Revision
Date: 4/17/2020	Sheet of	
File: F:\largework\...\core.SchDoc	Drawn By:	

A

B

C

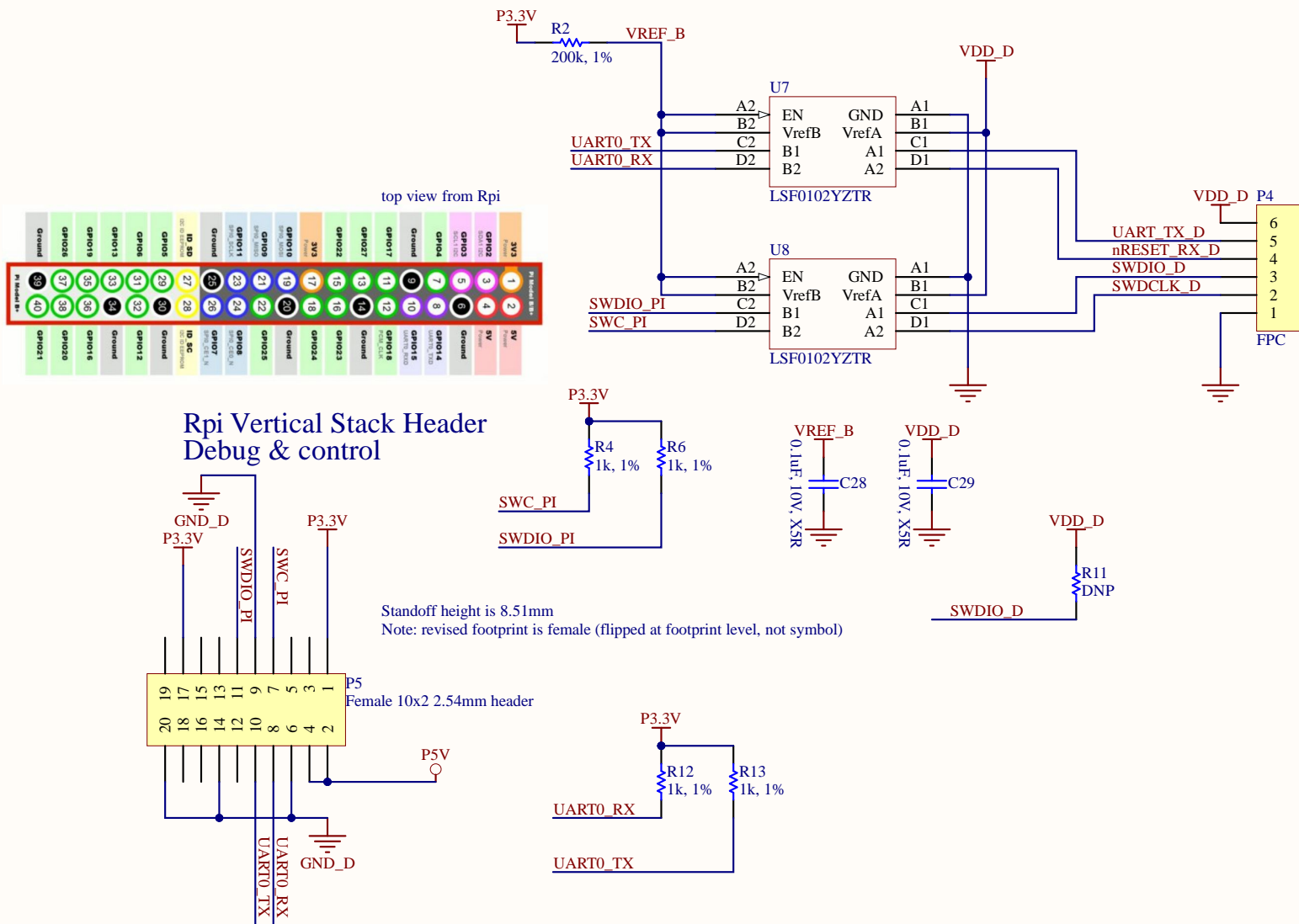
D

1

2

3

4



A

B

C

D



Title		
Simmel - Debug		
Size	Number	Revision
A		
Date:	4/17/2020	Sheet of
File:	F:\largework\...\debug.SchDoc	Drawn By:

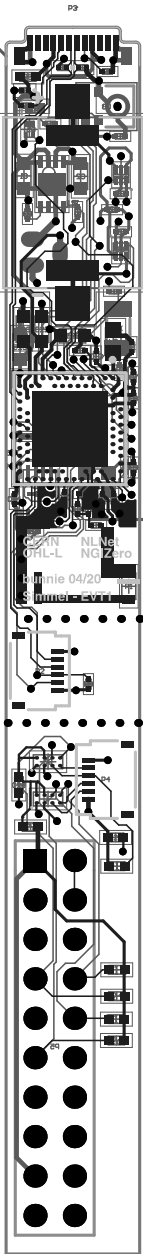
1

2

3

4

Route outline along midline



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.010mm	3.5	
1	Top Layer	Copper	0.036mm		
	Dielectric 2	PP-006	0.071mm	4.1	
2	Layer 1	Copper	0.035mm		
	Dielectric 1	FR-4	0.500mm	4.8	
3	Layer 2	Copper	0.035mm		
	Dielectric 3	PP-006	0.071mm	4.1	
4	Bottom Layer	Copper	0.036mm		
	Bottom Solder	Solder Resist	0.010mm	3.5	
	Bottom Overlay				

Total board thickness: 0.804mm

Solder mask green
Silkscreen white
Finish ENIG

Target 0.145mm to 50 ohm in stack