100/100

Tristan Denning

ECE 310 – Microelectronics I

Homework #5

Fall 2021

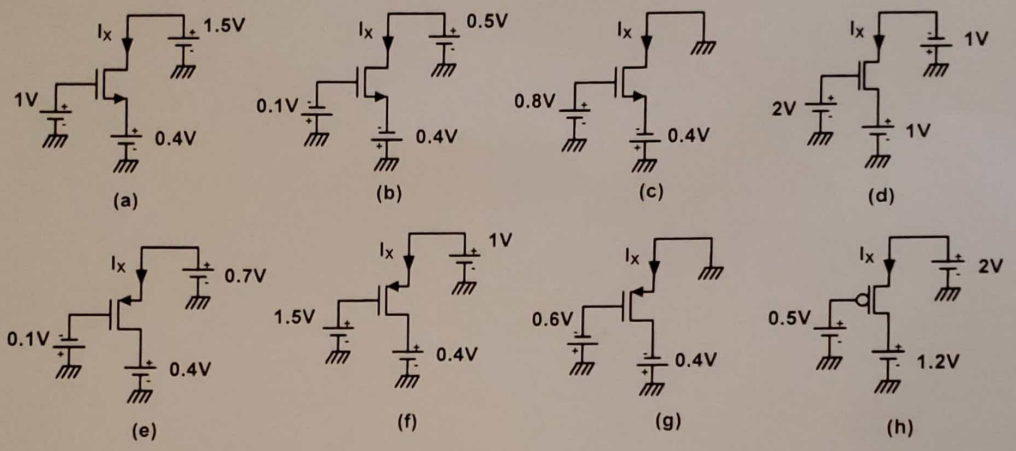
Dr. Suat Ay

(Due Date: 10/25/2021, 8.30am, Monday)

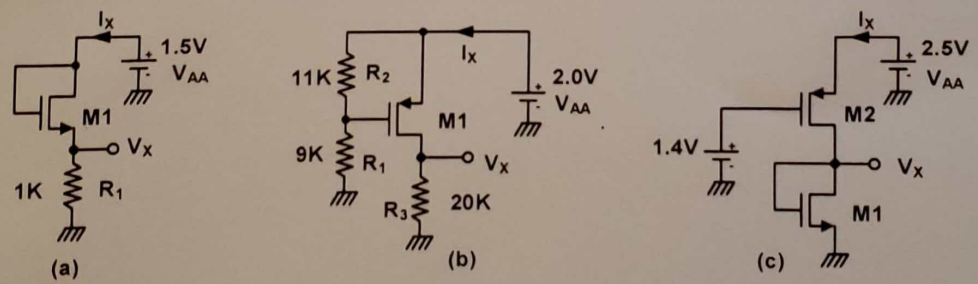
For the problems below, use;

KP_n=100 μA/V², V_{THn}=+0.5V for NMOS, and KP_p=50μA/V², V_{THp}= -0.4V for PMOS transistors.

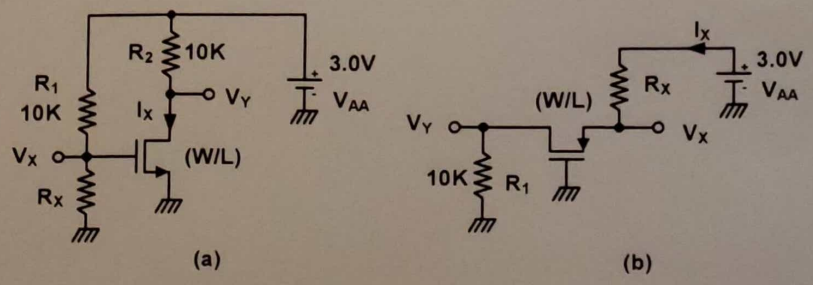
1. **(40 points)** Find the operating conditions (ON/OFF, LIN/SAT) and biasing conditions (V_{OD}, V_{DSAT}, I_X) of the following transistors. Use $(W/L)_n$=10 and $(W/L)_p$=5.



2. **(30 points)** Find the operating conditions (ON/OFF, LIN/SAT) and unknown voltage and current values (V_X, I_X) of the following transistors and circuits. Use $(W/L)_n$=10 and $(W/L)_p$=5.



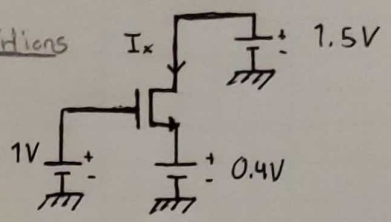
3. **(30 points)** Find unknown parameters (V_X, I_X, V_Y, W/L) of the following circuits by biasing NMOS transistor 0.3V in ON and 0.5V in SAT region while PMOS transistor 0.8V in ON and 0.5V in SAT region.



Tristan Denning | ECE-310 Homework 5 Problem 1(a.) | HW # 05

1(a)

1 Situation: Find the operating conditions (ON/OFF, LIN/SAT) and Biasing Conditions (V_{DD}, V_{DSAT}, I_x) of the following transistors.



Given Values: $\left(\frac{W}{L}\right)_n = 10$, $\left(\frac{W}{L}\right)_p = 5$,

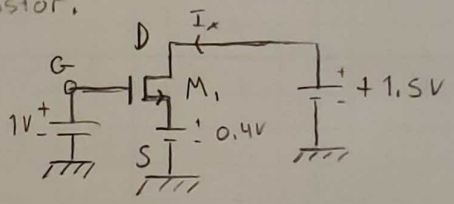
$KP_n = 100\ \mu A/V^2$ $V_{THn} = +0.5V$, $KP_p = 50\ \mu A/V^2$, $V_{THP} = -0.4V$ for parts (a)-(h).

2 Goal: To determine the biasing conditions and operating conditions as defined in the problem statement for the given transistor.

3 Plan: To utilize known relationships for V_{DD}, $V_{D,sat}$, V_{THn}, V_{THp}, I_{SD}, I_{DS}, V_{GS}, V_{SD}, V_{DS} ...etc... to determine the biasing conditions and operating conditions for the given transistor.

4 Solution:

Redraw



Observe: NMOS transistor $\because V_D > V_S$ $1.5 > 0.4$

$V_D = 1.5V$
$V_G = 1.0V$
$V_S = 0.4V$

(ON/OFF) $V_{GS} = 1.0 - 0.4 = 0.6V$

$V_{GS} > V_{TH,n}$
$0.6V > 0.5V$ $\therefore$ M_1 is ON ✓

(SAT/LIN, V_{DD})

$V_{DD} = V_{GS} - V_{TH} = 0.6 - 0.5 = 0.1V$ $\therefore$ $V_{DD} = 0.1V$ ✓

$V_{DS} = 1.5 - 0.4 = 1.1V$

$V_{DS} > V_{DD}$
$1.1V > 0.1$ $\therefore$ M_1 is SAT ✓

1/20

1(a) (continued)

(V_O,SAT)

$$V_{O,SAT} = V_{OS} - V_{OD}$$
$$= 1.1V - 0.1V$$
$$\boxed{V_{O,SAT} = 1.0V}$$

(I_x)

$$I_x = \frac{1}{2} KP_n \left(\frac{W}{L}\right)_n (V_{OD})^2$$
$$= 0.5(100 \times 10^{-6})(10)(0.1)^2$$
$$\boxed{I_x = 5\,\mu A}$$

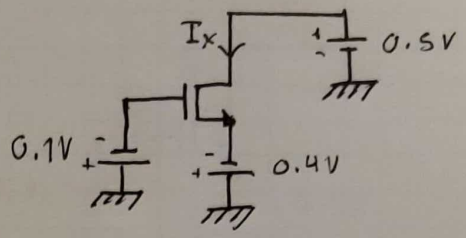
5 Sanity Check:

Unit analysis, I_x

$$I_x[A] = \left[\frac{A \times 10^{-6}}{V^2}\right] \cdot [-] \cdot [V^2]$$
$$[A] = [A]$$

* Answer is in correct units, and in appropriate magnitude, [μA]

1(b.) 1 Situation: (See 1(a).)

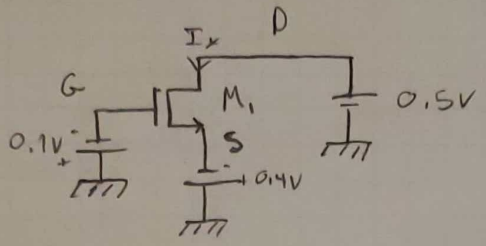


2 Goal: (See 1(a.))

3 Plan: (See 1(a.))

4 Solution:

Redraw:



Observe: NMOS Transistor with $V_D > V_S$, $0.5 > -0.4$

$V_D = 0.5V$
$V_S = -0.4V$
$V_G = -0.1V$

(ON/OFF) $V_{GS} = V_G - V_S = -0.1 - (-0.4)$
$V_{GS} = -0.3V$

$V_{GS} < V_{TH}$

$-0.3 < 0.5V$

$\therefore$ **M_1 is OFF**

$\therefore$ **$V_{DD} = V_{DSAT} = I_x = \emptyset$**

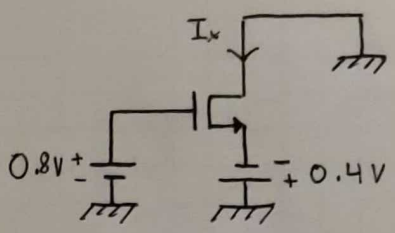
$\therefore$ **Neither LIN NOR SAT**

5 Sanity Check

Reasonable result from straightforward process.

Tristan Denning | Problem 1(C) | HW # 05

1(C.) 1 Situation: (See 1(a))

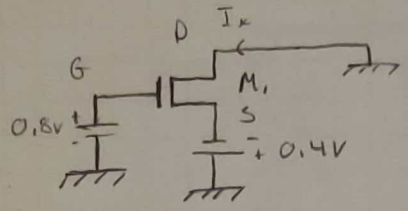


2 Goal: (See 1(a))

3 Plan: (See 1(a))

4 Solution:

Redraw:



Observe: NMOS Transistor

$V_D = 0$

$V_G = 0.8$

$V_S = -0.4$

$V_{DS} = 0.4\,V$

(ON/OFF) $V_{GS} = 0.8 - (-0.4) = 1.2\,V$

$V_{GS} > V_{TH,n}$

$1.2 > 0.5$

$\therefore$ **M_1, ON**

(SAT/LIN, V_{DD})

$V_{DD} = V_{GS} - V_{TH}$

$= 1.2 - 0.5$

$\therefore$ **$V_{DD} = 0.7\,V$**

$V_{DS} < V_{DD}$

$0.4 < 0.7\,V$ $\therefore$ **M_1 is in LIN mode**

$\therefore$ **$V_{D,SAT} = \emptyset$**

(I_x) LIN Region: $I_x = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n \left(2(V_{DD})(V_{DS}) - V_{DS}^2\right)$

$= 0.5\,(100\times10^{-6})(10)\left(2(0.7)(0.4) - (0.4)^2\right)$

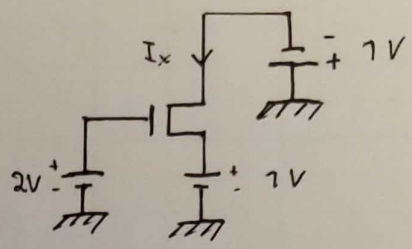
$I_x = 200\,\mu A$

5 Sanity Check:

Reasonable result from straightforward process.

1(d.)

1 Situation: (See 1(a.))

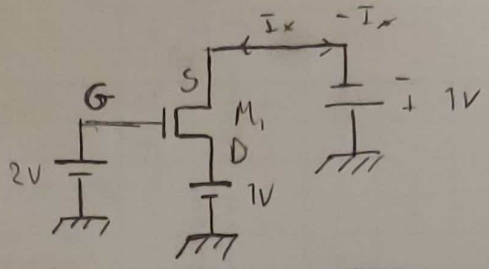


2 Goal: (See 1(a))

3 Plan: (See 1(a))

4 Solution:

Redraw:



Observe: Not defined as NMOS or PMOS

let I_x be a negative current, so current flows from D to S as labeled $(-I_x) = I_{DS}$

$V_D = 1V$

$V_S = -1V$

$V_G = 2V$

Then M_1 is NMOS

(ON/OFF)

$V_D > V_S$; $1V > -1V$

$V_{GS} = 2V + 1V = 3V$

$V_{GS} > V_{TH,n}$

$3V > 0.5V$ $\therefore$ **M_1 ON**

(SAT/LIN, V_{DD})

$V_{GS} - V_{TH} = V_{DD}$

$3 - 0.5 = 2.5V$; **$V_{DD} = 2.5V$**

$V_{DS} < V_{DD}$

$1 - (-1)V < 2.5V$

$2V < 2.5V$

$\therefore$ **M_1 In LIN Region**

$\therefore$ **$V_{D,SAT} = \emptyset$**

(I_x) in linear

$$-I_x = I_{DS} = \frac{1}{2} k P_n \left(\frac{W}{L}\right)_n \left(2(V_{OD})(V_{DS}) - V_{DS}^2\right)$$

$$= 0.5(100)(1)\left(2(2.5)(2) - (2)^2\right) \times 10^{-6}$$

$I_{DS} = 3\,mA$

$\therefore$ **$I_x = -3\,mA$**

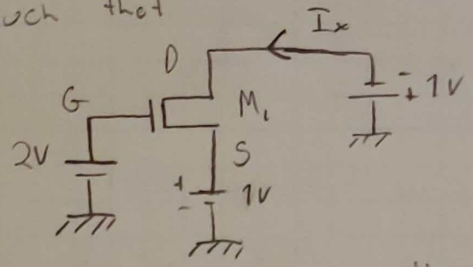
5/20

1(d) (continued)

Sanity Check:

Under the assumption that M_1 was an NMOS Transistor, the result seems reasonable

IF I Chose the S and D to be switched such that



And M_1 is Nmos, this is incorrect, since $V_D < V_S$

I could have instead Chosen the same Configuration as above, but assumed M_1 is PMOS.

Then I_x would be negative, flowing from S to D, (I_{SD})

In which Case: (M_1 is PMOS)

$V_{SG} = 1 - 2 = -1V$

$V_{TH,P} = -0.4V$

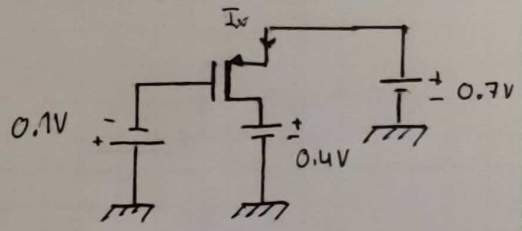
$V_{SG} \overset{?}{>} |V_{THP}|$

$-1V < 0.4V$, So M_1 would be OFF and All other parameters $\varnothing$

$\therefore$ So the assumption that M_1 is NMOS with I_x being negative and the subsequent results seem reasonable

Tristan Deming | Problem 1(e.) | HW # 05

1(e.) 1 Situation: (See 1(a.))

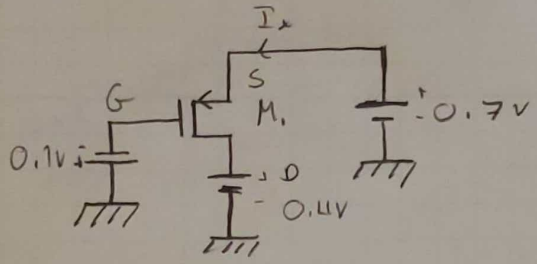


1 Goal: (See 1(a.))

2 Plan: (See 1(a.))

3 Solution:

Redraw:



Observe: PMOS Transistor with $V_S > V_D$

$V_S = 0.7\ V$
$V_D = 0.4\ V$
$V_G = -0.1V$

(ON/OFF)

$V_{SG} = 0.7 - (-0.1)$
$= 0.8V$

$V_{SG} > |V_{THp}|$
$0.8V > 0.4V$ ∴ **M_1, ON**

(SAT/LIN, V_{DD})

$V_{SD} = 0.7 - 0.4$
$= 0.3V$

$V_{DD} = V_{SG} - |V_{THp}|$
$= 0.8 - 0.4$
$= 0.4V$; **$V_{DD} = 0.4\ V$**

$V_{SD} < V_{DD}$
$0.3V < 0.4V$ ∴ **M_1 is in LIN Reg.**

$V_{D,SAT} = \emptyset$ ∵ M_1 is Not saturated

(I_x) Linear Mode $I_{SD} = I_x = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_p \left(2(V_{DD})(V_{SD}) - V_{SD}^2\right)$

$= 0.5(500 \times 10^{-6})(5)(2(0.4)(0.3) - (0.3^2))$

$I_x = 188\ \mu A$

4 Sanity Check: Reasonable result from straight forward process.

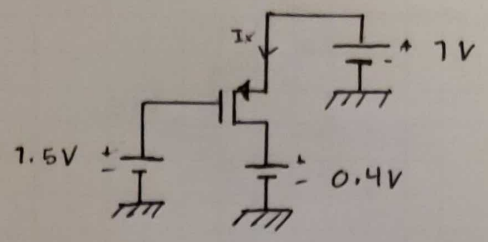
7/20

1(f.)

1 Situation: (See 1(a))

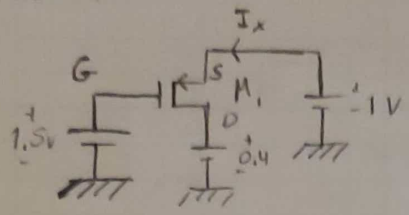
2 Goal: (See 1(a))

3 Plan: (See 1(a))



4 Solution:

Redraw:



Observe: PMOS Transistor, with $V_S > V_D$

$V_S = 1V$
$V_G = 1.5V$
$V_D = 0.4V$

(ON/OFF) $V_{SG} = 1 - 1.5V$
$= -0.5V$

$V_{SG} < |V_{THp}|$
$-0.5V < 0.4V$ $\therefore$ **M_1 is OFF**

$\therefore$ **M_1 is neither SAT nor LIN**

$\therefore$ **$V_{D,SAT}$, V_{OD}, $I_x = \emptyset$**

5 Sanity Check:

Answer is reasonable and came from a straightforward process.

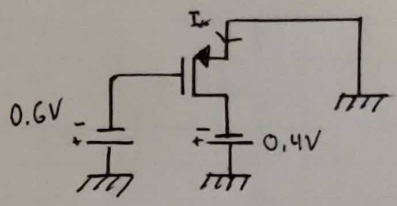
8/20

7(g)

1 Situation: (See 1(a.))

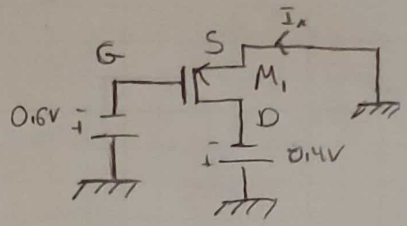
2 Goal: (See 1(a))

3 Plan: (See 1(a.))



4 Solution:

Redraw:



Observe:

$V_S = 0\,V$ ∵ GND

$V_G = -0.6\,V$

$V_D = -0.4V$

(ON/OFF)

$V_{SG} = 0 + 0.6V$

$= +0.6V$

$V_{SG} > |V_{TH,p}|$

$0.6V > 0.4V$ ∴ M_1 ON

(SAT/LIN, V_{OD})

$V_{SD} = 0 - (-0.4V)$

$= 0.4V$

$V_{OD} = V_{SG} - |V_{TH,p}|$; $V_{OD} = 0.2V$

$= 0.6 - 0.4$

$= 0.2V$

$V_{SD} > V_{OD}$

$0.4 > 0.2$ ∴ M_1 is SAT

$V_{O,SAT} = V_{SD} - V_{OD}$

$= 0.4 - 0.2$

$= 0.2V$ ∴ $V_{O,SAT} = 0.2V$

(I_x) SAT region

$I_x = \frac{1}{2} K P_p \left(\frac{W}{L}\right)_p V_{OD}^2$

$= 0.5(50 \times 10^{-6})(5)(0.2^2)$

$I_x = 5\,\mu A$

5 Sanity Check: Answer is reasonable and on the same order of magnitude as results from similar problems

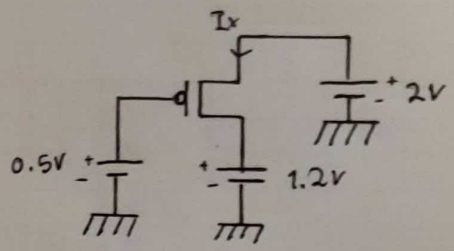
9/20

Tristan Denning | Problem 1(h) | HW # 05

1(h.) 1. Situation: (See 1(a))

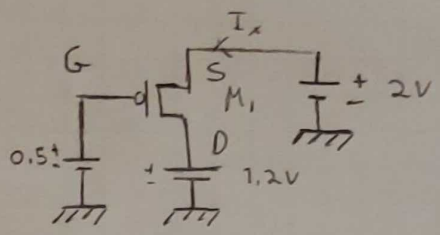
2. Goal: (See 1(a))

3. Plan: (See 1(a))



4. Solution:

Redraw:



Observe: PMOS Transistor

$V_G = 0.5V$
$V_S = 2V$
$V_D = 1.2V$

(ON/OFF)

$V_{SG} = 2 - 0.5$
$= 1.5V$

$V_{SG} > |V_{TH,p}|$
$1.5V > 0.4V$

$\therefore$ **M_1 ON**

(SAT/LIN)

$V_{SD} = 2 - 1.2$
$= 0.8V$

$V_{OD} = V_{SG} - |V_{TH}|$
$= 1.5 - 0.4$
$= 1.1V$

$\therefore$ **$V_{OD} = 1.1V$**

$V_{SD} < V_{OD}$
$0.8 < 1.1$

$\therefore$ **M_1 is in LIN Region**

$\therefore$ **$V_{O\,SAT} = \emptyset$**

(I_x) linear Reg

$$I_x = \frac{1}{2} K_P \left(\frac{W}{L}\right)_p \left(2(V_{OD})(V_{SD}) - (V_{SD})^2\right)$$
$$= \frac{1}{2}(50 \times 10^{-6})(5)\left(2(1.1)(0.8) - (0.8)^2\right)$$

$I_x = 140\,\mu A$

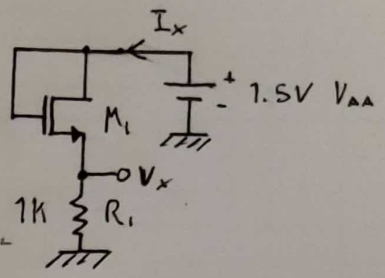
5. Sanity Check

Result is reasonable and came from a straightforward process

10/20

Tristan Denning | Problem 2(a.) | HW# 05

2(a) 1 **Situation:** Find the operating Conditions (ON/OFF, LIN/SAT) and Voltage and Current Values (V_x and I_x) For the Following Transistors. (a–c)



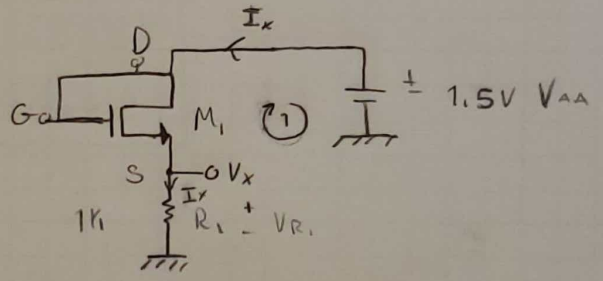
Use: $\left(\frac{W}{L}\right)_n = 10$, $\left(\frac{W}{L}\right)_p = 5$, $kP_n = 100\ \mu A/V^2$, $V_{THn} = 0.5V$, $kP_p = 50\ \mu A/V^2$, $V_{THp} = -0.4V$

2 **Goal:** To determine the biasing Conditions and operating conditions as defined in the problem Statement for each corresponding transistor in parts 2(a) – 2(c).

3 **Plan:** To utilize known relationships and equations for V_{DD}, V_{DSAT}, V_{TH}, I_{SD}, I_{DS}, V_{GS} ... etc.. to determine the operating and biasing Conditions for each transistor

4 **Solution:**

Redraw.



Observe: NMOS Transistor

$V_D = V_{AA} = 1.5V = V_G$

$V_x = V_S$

$\therefore V_{GS} = V_{DS} = 1.5 - V_x$

(SAT/LIN) $V_{DS} > V_{GS} - V_{TH}$

$V_{DS} > V_{GS} - 0.5$

$0 > -0.5$ $\therefore$ M_1 is ON and SAT always.

(I_x) SAT $I_x = \frac{1}{2} kP_n \left(\frac{W}{L}\right)_N (V_{GS} - V_{TH})^2$

KVL (1) $V_{GS} = 1.5 - 1000 I_x$ $\because$ Ohm's law R_1

$\therefore I_x = 0.5(100\times10^{-6})(10)(1.5 - 1000I_x - 0.5)^2$ (1)

2(a) (continued)

Solving equation (1) for I_x yields

$I_x = 268\,\mu A$ or $I_x = 3.732\,mA$

Then $V_x = 1000\,I_x$

$\therefore V_x = 0.268\,V$, or $V_x = 3.732\,V$

To fulfil $V_D > V_S$, $1.5V > V_S$,

$\therefore$ $V_x = 0.268\,V$, $I_x = 268\,\mu A$ must be true

Sanity Check

$$I_x = \frac{1}{2} k P_n \left(\frac{W}{L}\right)_N (V_{GS} - V_{TH})^2$$

$$= 0.0005\left((1.5 - 0.268 - 0.5)^2\right)$$

$$= 268\,\mu A$$

$\therefore$ Plugging V_x into I_x eqn yields the anticipated I_x.

Check ON/OFF $V_{GS} > V_{TH}$

$(1.5 - 0.268) > 0.5$

$1.232 > 0.5$ ✓ M_1 ON

Check SAT/LIN $V_{DS} > V_{GS} - V_{TH}$

$(1.5 - 0.268) > (1.5 - 0.265) - 0.5$

$0 > -0.5$ ✓ M_1 is LIN

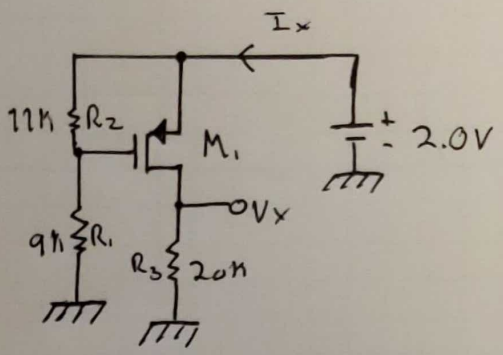
Tristan Denning | Problem 2(b) | HW # 05

2(b)

1 Situation: (See 2(a))

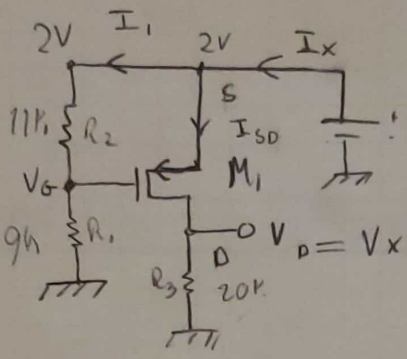
2 Goal: (See 2(a))

3 Plan: (See 2(a))



4 Solution:

Redraw:



Observe: PMOS Transistor

$V_D = V_x$; $V_S = 2V$

Find V_G Nodal Analysis at V_G Node,

$$\frac{2 - V_G}{11000} = \frac{V_G}{9000}$$

$$\therefore V_G = 0.9V$$

$$\therefore V_{SG} = 2 - 0.9 = 1.1V$$

(ON/OFF) $V_{SG} > |V_{THp}|$

$1.1V > 0.4V$ $\therefore$ **M_1 is ON**

(SAT/LIN) Assume Saturation, then Verify

$$I_{SD} = \frac{1}{2} KP_p \left(\frac{W}{L}\right)_p (V_{SG} - V_{TH})^2$$

$$= 0.000125 (1.1 - 0.4)^2$$

$$I_{SD} = 61.25\ \mu A$$

$$\therefore V_x = V_D = 20000 (I_{SD})$$

$$= 1.225\ V$$

$$\therefore \boxed{V_x = 1.225\ V}$$

13/20

2(b) (continued)

$$\therefore \quad V_{SD} = 2 - 1.225 = 0.775$$

Check $V_{SD} > V_{SG} - |V_{THp}|$

$0.775 > 1.1 - 0.4$

$0.775 > 0.7$ ✓

$\therefore$ **M_1 is indeed Saturated**

$$I_x = I_{SD} + I_1$$

$$= 61.25\ \mu A + V_G/9000$$

$$= 61.25 \times 10^{-6} + 0.1 \times 10^{-3}$$

$$\therefore \boxed{I_x = 161.25\ \mu A}$$

Sanity Check:

KVL Right Side:

$2V - V_{SD} - V_o = 0$

$2V - 0.775V - 1.225V = 0$

$0 = 0$ ✓

KVL Left Side:

$V_{R_1} + V_{SG} = 0.775 + 1.225$

$9000(0.1) + 11000(0.1) = 2$

$2V = 2V$ ✓

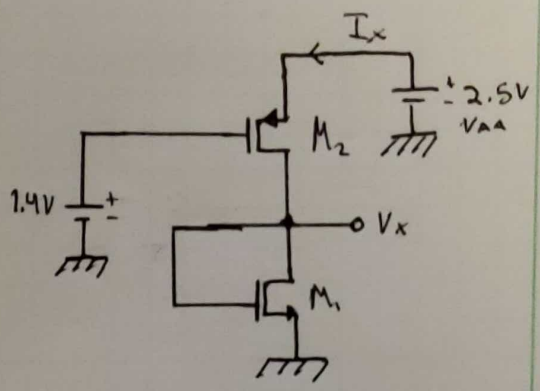
Tristan Denning | Problem 2(c) | HW #05

2(c) **1 Situation:** (See 2(a))

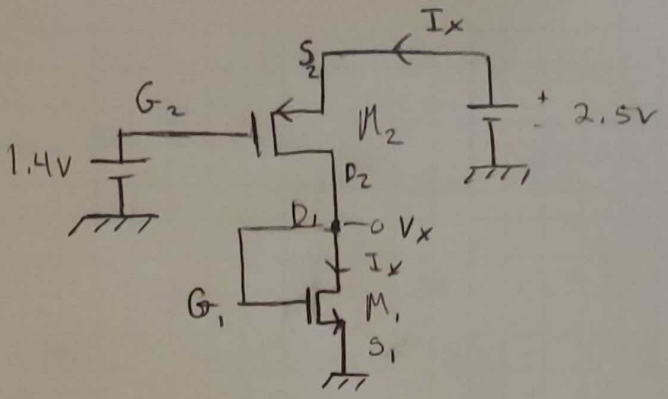
2 Goal: (See 2(a))

3 Plan: (See 2(a))

4 Solution:



Redraw:



Observe M_1, NMOS, M_2, PMOS

$V_{G2} = 1.4$, $V_{S2} = 2.5V$, $V_{D2} = V_{D1}$

$V_{G1} = V_{D1}$, $V_{S1} = 0$

$I_x = I_{SD2} = I_{DS1}$

M_2

(ON/OFF)

$V_{SG} = 2.5 - 1.4$

$= 1.1V$

$V_{SG} > |V_{TH,P}|$

$1.1 > 0.4$

M_2, ON

M_1

(ON/OFF/SAT/LIN)

$V_{GS} = V_{DS}$

$V_{DS} > V_{GS} - V_{TH,N}$

$V_{DS} - V_{GS} > -0.5V$

$0 > -0.5$

$\therefore$ M_1 is SAT and ON

15/20

2(c) (Continued)

Assume M_2 is SAT

$$I_{SD} = I_x = \frac{1}{2} k_p \left(\frac{W}{L}\right)_p (V_{SG} - |V_{TH}|)^2$$

$$= 0.000125 (1.1 - 0.4)^2$$

$$= 61\,\mu A$$

$$\boxed{I_x = 61\,\mu A}$$ * through M_1

Then through M_1, $I_{DS} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_N (V_{GS} - V_{TH})^2$

$$61 \times 10^{-6} = 0.0005 (V_{GS} - 0.5)^2$$

$$61 \times 10^{-6} = 0.0005 (V_x - 0.5)^2$$

$$\therefore V_x = 0.15V \text{ or } 0.85V$$

For $V_x = 0.15$, M_1 cannot be on.

$V_{GS} < V_{TH,n}$

$0.15 < 0.5$ $\because V_{GS} = V_x$

$\therefore$ V_x must be 0.85 V

$$\boxed{V_x = 0.85V}$$

Then $\boxed{M_2 \text{ is SAT}}$

$\because$ $V_{SD} > V_{SG} - |V_{TH,p}|$

$(2.5 - 0.85) > (1.1 - 0.4)$

$1.65 > 0.7$

Sanity Check:

KVL Right Side: $2.5 - V_{SD} - V_x = 0$

$2.5 - 1.65 - 0.85 = 0$

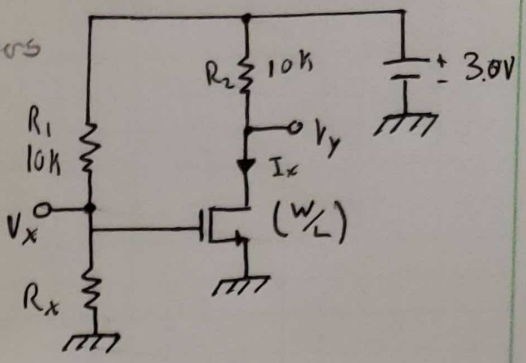
$0 = 0$ ✓

16/20

Tristan Denning | Problem 3(a) | HW # 05

3(a)

1 Situation: Find Unknown Parameters $(V_x, I_x, V_y, W/L)$ of the Following Circuits by biasing NMOS Transister 0.3V in ON and 0.5V in SAT while PMOS Transister 0.8V in ON and 0.5 in SAT region.

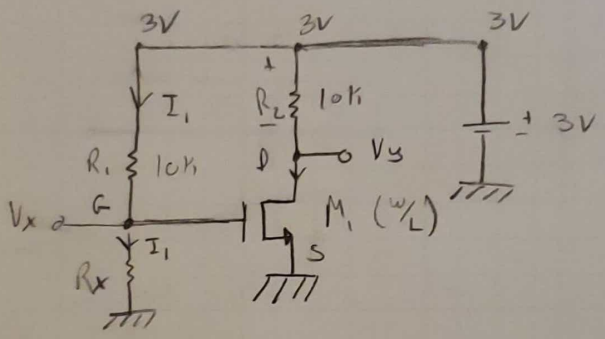


2 Goal: To Find the unknown Parameters (V_x, I_x, V_y and W/L).

3 Plan: To utilize known relationships for V_{DD}, $V_{D,SAT}$, V_{TH}, I_{SD}, I_{DS}, V_G, V_S, V_D ... etc, to set up and solve expressions for (V_x, I_x, V_y, and W/L)

4 Solution:

Redraw



Observe: NMOS Transister

$V_S = 0$

$V_D = V_y$

$V_x = V_G$

$V_{GS} = V_x$

Given:

$$V_{D,SAT} = V_{DS} - V_{DD} = 0.5$$
$$= V_{DS} - (V_{GS} - V_{TH})$$

$$V_{GS} - V_{TH} = 0.3$$

$$\therefore \quad 0.5 = V_{DS} - 0.3$$

$$\therefore \quad V_{DS} = 0.8$$

$$V_D = 0.8 \qquad \because \; V_S = 0$$

$$\therefore \quad \boxed{V_y = 0.8}$$

$$V_{R2} = V_{AA} - V_y$$
$$= 3 - 0.8$$
$$= 2.2\,V$$

17/20

3(a) (Continued)

$V_{R_2} = 2.2V$

$\therefore I_x = \frac{2.2}{10000}$

$\boxed{I_x = 0.22\ mA}$

Solve For V_x

$V_{GS} - V_{TH,N} = 0.3$

$V_x - V_{TH,N} = 0.3$

$V_x - 0.5 = 0.3$

$\therefore \boxed{V_x = 0.8\ V}$

Solve For (W/L)

$I_{x_1} = \frac{1}{2} k_{P_n} \left(\frac{W}{L}\right)(V_{OD})^2$

$\frac{2.2\times10^{-3}(2)}{(100\times10^{-6})(0.3^2)} = \frac{W}{L}$

$\therefore \boxed{\frac{W}{L} = 48.89}$

Solve For R_x

$I_1 = \frac{3 - V_x}{10K}$

$= \frac{3 - 0.8}{10K}$

$= 0.22\ mA$

$\therefore R_x = \frac{V_x}{I_1}$

$= 0.8\ V / 0.22\times10^{-3}\ A$

$\therefore \boxed{R_x = 3636.36\Omega}$

Sanity Check:

$V_{GS} > V_{TH}$

$0.8 > 0.5 \quad \therefore M_1$ is ON ✓

$V_{DS} > V_{OD}$

$0.8 > 0.3 \quad \therefore M_1$ is SAT ✓

KVL Right Side: $3V - (10K)(0.22\times10^{-3}) - V_y = 0$

$3V - 2.2 - 0.8 = 0$

$0 = 0$ ✓

KVL Left Side: $V_x + V_{R_1} - V_{R_2} - V_y = 0$

$0.8 + 2.2 - 2.2 - .8 = 0$

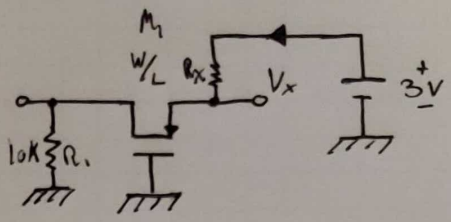
$0 = 0$ ✓

18/20

Tristan Denning | Problem 3(b) | HW # 05

3(b)

Situation: Find the unknown Parameters (V_x, I_x, V_y, W/L) of the Following Circuit. Use $V_{DD} = 0.8V$, and $V_{D,SAT} = 0.5$.

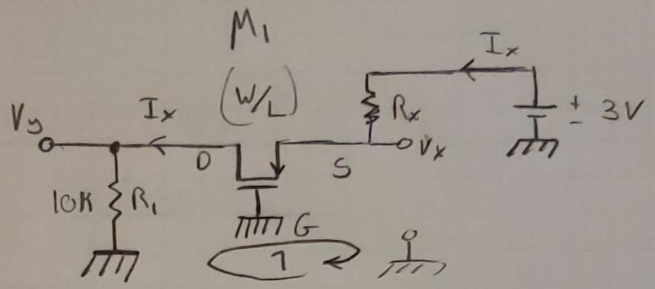


Goal: (See 3(a).)

Plan: (See 3(a).)

Solution:

Redraw



Observe:
$V_G = 0$
$V_D = V_y$
$V_x = V_S$

Given:
$V_{DD} = 0.8V$
$= (V_{SG} - |V_{TH,P}|)$
$0.8 = V_{SG} - 0.4$ $\quad \because V_{TH,P} = -0.4V$
$\therefore V_{SG} = 1.2\ V$

$V_G = 0$, $V_S = 1.2\ V$

$\therefore V_S = \boxed{V_x = 1.2V}$

Given:
$V_{D,SAT} = V_{SD} - V_{DD}$
$0.5 = V_{SD} - 0.8$
$\therefore V_{SD} = 1.3\ V$

KVL ①:
$V_y + V_{SD} - V_x = 0$
$V_y + 1.3 - 1.2 = 0$
$\therefore \boxed{V_y = -1V}$ -0.1

19/20

3(b) (continued)

$$V_y = -1V$$

$$\therefore I_x = V_y / R_1$$

$$= -1/10000$$

$$\boxed{I_x = -100\,\mu A}$$

$$I_x = -100\times10^{-6} = \frac{1}{2} k P_p \left(\frac{W}{L}\right)_p (V_{DD})^2$$

$$W/L = \frac{-2(100\times10^{-6})}{(50\times10^{-6})(0.8^2)}$$

$$\therefore \boxed{W/L = -6.25}$$

Sanity Check

The result for W/L is somewhat insane, since negative width and length are not feasible quantities.

This could be a result of:

1.) I Misunderstand Simple Algebra and the following argument is incorrect:

$$V_{DD} = 0.8V = (V_{SG} - |V_{THp}|) \quad \because \text{Given}$$

$$\therefore V_{SG} = 1.2V \quad \because V_{TH,P} = -0.4V$$

$$\Rightarrow V_{D,SAT} = 0.5 = V_{SD} - V_{DD} \quad \because V_{DD} = 0.8V$$

$$\therefore V_{SD} = 1.3V$$

$$\therefore V_y + V_{SD} = V_{SG} \quad \because \text{KVL}$$

$$V_y = 1.2 - 1.3 = \boxed{-0.1V}$$

or 2.) The Given parameters are not the appropriate quantities for the given PMOS Configuration

or 3.) Some Sign Convention I Overlooked

20/20