+33 7 61 18 28 96
Zürich, Switzerland
tristan.torchet@uzh.ch

Tristan **Torchet**

Scholar
GitHub
Website - LinkedIn

Education

Joint Ph.D. in Electrical Engineering and Neuroscience **Sep 2023 - Present**
Institute of Neuroinformatics, Emerging Intelligent Substrates Lab - ETHZ and UZH
Focus: Hardware-software co-design, dendritic computing, linear sequence models.
Committee: Prof. Melika Payvand (main supervisor), Prof. Shih-Chii Liu, Dr. Abu Sebastian, Prof. Luca Benini.

Master of Science in Electrical Engineering and Information Technology **Sep 2021 - Jul 2023**
ETH Zürich
Main courses: Introduction to Machine Learning, Advanced Machine Learning, Neuromorphic Engineering (I and II), VLSI (I, II and III), Machine Learning on Microcontrollers, Introduction to Neuroinformatics, Deep Leaning in Biological Networks.

Bachelor of Electrical and Electronic Engineering **Sep 2017 - Jul 2021**
École Polytechnique Fédérale de Lausanne (EPFL)
Main courses: Analysis (I, II, III, IV), Physics (I, II, III, IV), Electrotechnics (I and II), Electronics (I and II).
Exchange year: obtained a grant to study one year in Sapienza University, Rome.

Research - Selected Publications

mGRADE: Minimal Recurrent Gating Meets Delay Convolutions for Lightweight Sequence Modeling
- Proposed a hybrid-memory architecture enabling efficient multi-scale temporal processing on edge devices.
- Demonstrated formally the advantages of the hybrid system.
- Showed that the proposed architecture achieves the smallest networks with competitive results on long-range dependency tasks.
- **Torchet, T.**, Metzner, C., et al. mGRADE: Minimal Recurrent Gating Meets Delay Convolutions for Lightweight Sequence Modeling. Under Review (2025).

Quantizing Small-Scale State-Space Models for Edge AI
- Demonstrated efficient low-bit state-space models through quantization-aware training
- Proposed a heterogeneous precision scheme reducing memory 6× without performance loss.
- **Torchet, T.**, Zhao, L. et al. Quantizing Small-Scale State-Space Models for Edge AI. ACM International Conference on Neuromorphic Systems (ICONS) (2025).

DenRAM: Neuromorphic Dendritic Architecture with RRAM for Efficient Temporal Processing with Delays
- Showed how implicitly learning a temporal kernel implements dendritic passive delays.
- Developed a hardware-aware training, compatible with the proposed RRAM circuit, for spiking neural networks (SNN) reaching the best performance for feedforward SNN models.
- **Torchet, T.**, D'Agostino, S., Moro, F. et al. DenRAM: neuromorphic dendritic architecture with RRAM for efficient temporal processing with delays. Nature Communications 15, 3446 (2024).

Projects

Hybrid recurrent-attention LLM
Telluride Workshop 2025

- Pretrained a 370M-parameter pretraining of HGRN-based models on 200B tokens FineWeb-Edu using a 8xH100 cluster.
- Compared pure recurrent model to hybrid HGRN-attention (6:1).
- The goal of this project was to get a first introduction on LLM training using a multi-GPU system. The project is continued for deployment on Loihi-2, implying quantization, further high quality data mixtures and fine-tuning.

LOKUM: SRAM Analog In-Memory-Computing Test Chip
Institute of Neuroinformatics, Emerging Intelligent Substrates Lab - ETHZ and UZH (Prof. Melika Payvand)

- Set up the development pipeline for the Global Foundries 22nm Fully-Depleted Silicon-On-Insulator (FD-SOI), enabling fast prototyping and verification through Siemens QuestaSim®, and Cadence Innovus®.
- Developed the digital side of the chip, comprising the controller of the analog macro and the I/O communication.

Event-driven Dynamic Sparse Training for Spiking Neural Networks
Institute of Neuroinformatics, Neuromorphic Cognitive Systems Lab - ETHZ, UZH (Prof. Giacomo Indiveri)

- Proposed an algorithm (EDST) for spiking neural networks, which keeps a constant high sparsity during the whole training process. EDST performs better than traditional pre-training pruning (static sparsity) and post-training pruning (dropout) techniques. The results were obtained through hardware-aware simulations of a custom ASIC circuit.
- Implemented a digital testbench to verify the CAM array circuits used for routing the spikes of each neuron. Executed mixed signal simulations using the Cadence Virtuoso® AMS Designer simulator.
- Z. Su, H. Hwang, **T. Torchet** and G. Indiveri, Core Interface Optimization for Multi-core Neuromorphic Processors, 2023 28th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), Beijing, China, 2023, pp. 89-98.

Time series forecasts for retail stock management
Prediko (Supervisor: Nicolas Sabatier, CTO)

- Implemented a pipeline for time series forecasts using ARIMA and Gaussian Processes.
- Developed an entire dashboard (front-end and back-end) to monitor the activity of both the company itself and the users of the platform.

SKILLS

Programming	Python (JAX, PyTorch), C, C++, CUDA
Hardware Design	SystemVerilog, Siemens QuestaSim®, Synopsys Design Compiler®, Cadence Innovus®, Cadence Virtuoso®
Communication	French (native), English (C1), Italian (C1), Spanish (B2)

TEACHING

Introduction to Neuroinformatics **ETHZ**
Student supervision
Elija Maria Vida (MSc Thesis), Leo Zhao (MSc Thesis), Christian Metzner (MSc Thesis).