

Industry-Standard Dual Operational Amplifiers

1 Features

- Wide supply range of 3 V to 36 V (B, BA versions)
- Quiescent current: 300 μ A/ch (B, BA versions)
- Unity-gain bandwidth of 1.2 MHz (B, BA versions)
- Common-mode input voltage range includes ground, enabling direct sensing near ground
- 2-mV input offset voltage max. at 25°C (BA version)
- 3-mV input offset voltage max. at 25°C (A, B versions)
- Internal RF and EMI filter (B, BA versions)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Merchant network and server power supply units
- Multi-function printers
- Power supplies and mobile chargers
- Motor control: AC induction, brushed DC, brushless DC, high-voltage, low-voltage, permanent magnet, and stepper motor
- Desktop PC and motherboard
- Indoor and outdoor air conditioners
- Washers, dryers, and refrigerators
- AC inverters, string inverters, central inverters, and voltage frequency drives
- Uninterruptible power supplies
- Electronic point-of-sale systems

3 Description

The LM358B and LM2904B devices are the next-generation versions of the industry-standard operational amplifiers (op amps) LM358 and LM2904, which include two high-voltage (36 V) op amps. These devices provide outstanding value for cost-sensitive applications, with features including low

offset (300 μ V, typical), common-mode input range to ground, and high differential input voltage capability.

The LM358B and LM2904B op amps simplify circuit design with enhanced features such as unity-gain stability, lower offset voltage maximum of 3 mV (2 mV maximum for LM358BA and LM2904BA), and lower quiescent current of 300 μ A per amplifier (typical). High ESD (2 kV, HBM) and integrated EMI and RF filters enable the LM358B and LM2904B devices to be used in the most rugged, environmentally challenging applications.

The LM358B and LM2904B amplifiers are available in micro-sized packaging, such as the SOT23-8, as well as industry standard packages including SOIC, TSSOP, and VSSOP.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
LM358B, LM358BA, LM2904B, LM2904BA, LM358, LM358A, LM2904, LM2904V, LM258, LM258A	SOIC (8)	4.90 mm × 3.90 mm
LM358B, LM358BA, LM2904B, LM2904BA, LM358, LM358A, LM2904, LM2490V	TSSOP (8)	3.00 mm × 4.40 mm
LM358B, LM358BA, LM2904B, LM2904BA, LM358, LM358A, LM2904, LM2904V, LM258, LM258A	VSSOP (8)	3.00 mm × 3.00 mm
LM358B, LM358BA, LM2904B, LM2904BA	SOT-23 (8)	2.90 mm × 1.60 mm
LM358, LM2904	SO (8)	5.20 mm × 5.30 mm
LM358, LM2904, LM358A, LM258, LM258A	PDIP (8)	9.81 mm × 6.35 mm
LM158, LM158A	CDIP (8)	9.60 mm × 6.67 mm
LM158, LM158A	LCCC (20)	8.89 mm × 8.89 mm

Family Comparison

Specification	LM358B LM358BA	LM2904B LM2904BA	LM358 LM358A	LM2904	LM2904V LM2904AV	LM258 LM258A	LM158 LM158A	Units
Supply voltage	3 to 36	3 to 36	3 to 30	3 to 26	3 to 30	3 to 30	3 to 30	V
Offset voltage (max, 25°C)	± 3 ± 2	± 3 ± 2	± 7 ± 3	± 7 ± 2	± 7 ± 2	± 5 ± 3	± 5 ± 2	mV
Input bias current (typ / max)	10 / 35	10 / 35	20 / 250 15 / 100	20 / 250	20 / 250	20 / 150 15 / 80	20 / 150 15 / 50	nA
Gain bandwidth product	1.2	1.2	0.7	0.7	0.7	0.7	0.7	MHz
Supply current (typ, per channel)	0.3	0.3	0.35	0.35	0.35	0.35	0.35	mA
ESD (HBM)	2000	2000	500	500	500	500	500	V
Operating ambient temperature	-40 to 85	-40 to 125	0 to 70	-40 to 125	-40 to 125	-25 to 85	-55 to 125	°C

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features	1	8 Detailed Description	26
2 Applications	1	8.1 Overview.....	26
3 Description	1	8.2 Functional Block Diagram: LM358B, LM358BA, LM2904B, LM2904BA.....	26
4 Revision History	2	8.3 Feature Description.....	27
5 Pin Configuration and Functions	4	8.4 Device Functional Modes.....	27
6 Specifications	5	9 Application and Implementation	28
6.1 Absolute Maximum Ratings.....	5	9.1 Application Information.....	28
6.2 ESD Ratings.....	5	9.2 Typical Application.....	28
6.3 Recommended Operating Conditions.....	6	10 Power Supply Recommendations	29
6.4 Thermal Information.....	6	11 Layout	29
6.5 Electrical Characteristics: LM358B and LM358BA.....	7	11.1 Layout Guidelines.....	29
6.6 Electrical Characteristics: LM2904B and LM2904BA.....	9	11.2 Layout Examples.....	30
6.7 Electrical Characteristics: LM358, LM358A.....	11	12 Device and Documentation Support	31
6.8 Electrical Characteristics: LM2904, LM2904V.....	12	12.1 Receiving Notification of Documentation Updates..	31
6.9 Electrical Characteristics: LM158, LM158A.....	13	12.2 Support Resources.....	31
6.10 Electrical Characteristics: LM258, LM258A.....	15	12.3 Trademarks.....	31
6.11 Typical Characteristics: LM358B and LM2904B.....	16	12.4 Electrostatic Discharge Caution.....	31
6.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.....	23	12.5 Glossary.....	31
7 Parameter Measurement Information	25	13 Mechanical, Packaging, and Orderable Information	32

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Z (July 2021) to Revision AA (March 2022)	Page
• Added LM358BA and LM2904BA to the <i>Device Information</i> table.....	1
• Added <i>Family Comparison</i> table to the <i>Description</i> section	1
• Raised ESD (CDM) for B-versions and BA-versions from 1 kV to 1.5 kV in the <i>ESD Ratings</i> table	5
• Changed Input Offset Voltage Max of LM2904BA from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ from $\pm 2.5 \text{ mV}$ to $\pm 3.0 \text{ mV}$	9

Changes from Revision Y (February 2021) to Revision Z (July 2021)	Page
• Deleted preview tag from LM358B and LM2904B SOT-23 (8) package in <i>Device Information</i> table.....	1
• Updated DDF (SOT-23) package thermal information in the <i>Thermal Information</i> table.....	6
• Deleted <i>Related Links</i> from the <i>Device and Documentation Support</i> section.....	31

Changes from Revision X (June 2020) to Revision Y (February 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added SOT23-8 (DDF) package information throughout data sheet.....	1
• Deleted preview tag from LM358B and LM2904B VSSOP (8) package in <i>Device Information</i> table.....	1
• Added SOT23-8 (DDF) package information to the <i>Pin Configuration and Functions</i> section.....	4
• Added DDF (SOT-23) package to the <i>Thermal Information</i> table.....	6

Changes from Revision W (October 2019) to Revision X (June 2020)	Page
• Added application links to <i>Applications</i> section.....	1
• Deleted preview tag from LM358B and LM2904B TSSOP (8) package in <i>Device Information</i> table	1

Changes from Revision V (September 2018) to Revision W (October 2019)	Page
• Changed CDM ESD rating for LM358B and LM2904B in <i>ESD Ratings</i>	5

• Changed V_S to V_+ in <i>Recommended Operating Conditions</i>	6
• Changed <i>Thermal Information</i> for the LM158FK and LM158JG devices.....	6
• Added <i>Typical Characteristics</i> section for the LM358B and LM2490B op amps.....	16
• Added test circuit for THD+N and small-signal step response, $G = -1$ in the <i>Parameter Measurement Information</i> section.....	25
• Changed the <i>Functional Block Diagram</i>	26

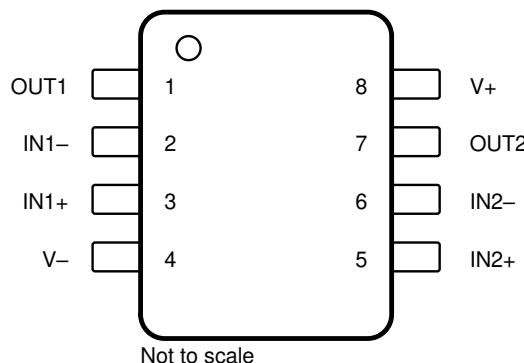
Changes from Revision U (January 2017) to Revision V (September 2018)	Page
• Changed the data sheet title	1
• Changed first four items in the <i>Features</i> section	1
• Changed the first item in the <i>Applications</i> section and added four new items	1
• Changed voltage values in the first paragraph of the <i>Description</i> section.....	1
• Changed text in the second paragraph of the <i>Description</i> section.....	1
• Added devices LM358B and LM2904B to data sheet.....	1
• Changed the first three rows of the <i>Device Information</i> table and added a cross-referenced note for PREVIEW-status devices.....	1
• Added a table note to the <i>Pin Functions</i> table	4
• Changed "free-air temperature" to "ambient temperature" in the <i>Absolute Maximum Ratings</i> condition statement.....	5
• Changed all entries in the <i>Absolute Maximum Ratings</i> table except T_J and T_{stg}	5
• Deleted lead temperature and case temperature from <i>Absolute Maximum Ratings</i>	5
• Changed device listings and their voltage values in the <i>ESD Ratings</i> table	5
• Changed "free-air temperature" to "ambient temperature" in the <i>Recommended Operating Conditions</i> condition statement	6
• Changed table entries for all parameters in the <i>Recommended Operating Conditions</i> table.....	6
• Added rows to the Thermal Information table, and a table note regarding device-package combinations	6
• Deleted the <i>Operating Conditions</i> table.....	15
• Added a condition statement to the <i>Typical Characteristics</i> section.....	23
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference.....	26
• Changed unity-gain bandwidth from 0.7 MHz for all devices to 1.2 MHz for B-version devices.....	27
• Changed slew rate from $3 \text{ V}/\mu\text{s}$ for all devices to $0.5 \text{ V}/\mu\text{s}$ for B-version devices.....	27
• Changed the <i>Section 8.3.3</i> section in multiple places throughout.....	27
• Changed V_{CC} to V_S in the <i>Section 9.1</i> section	28
• Subscripted the suffixes fro R_I and R_F	28
• Changed <i>Operational Amplifier Board Layout for Noninverting Configuration</i> with an image that includes a dual op amp.....	30

Changes from Revision T (April 2015) to Revision U (January 2017)	Page
• Changed data sheet title.....	1

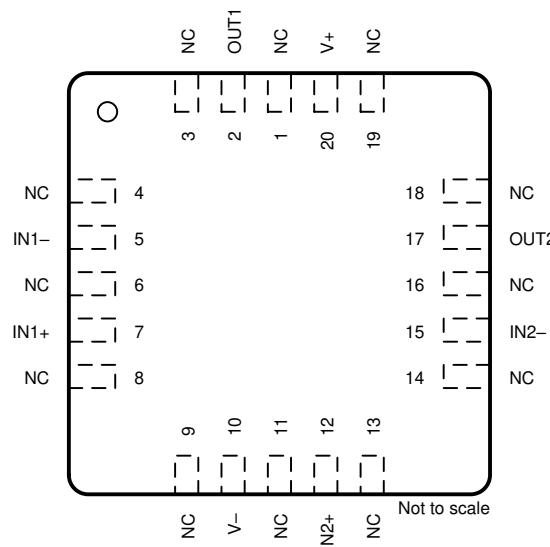
Changes from Revision S (January 2014) to Revision T (April 2015)	Page
• Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision R (July 2010) to Revision S (Jauary 2014)	Page
• Converted this data sheet from the QS format to DocZone using the PDF on the web.....	1
• Deleted <i>Ordering Information</i> table.....	1
• Updated <i>Features</i> to include Military Disclaimer.....	1
• Added <i>Typical Characteristics</i> section.....	23

5 Pin Configuration and Functions



**Figure 5-1. D, DDF, DGK, P, PS, PW, and JG Package
 8-Pin SOIC, SOT23-8, VSSOP, PDIP, SO, TSSOP,
 and CDIP Top View**



NC - No internal connection

**Figure 5-2. FK Package
 20-Pin LCCC
 Top View**

Table 5-1. Pin Functions

NAME	LCCC ⁽¹⁾	PIN	I/O	DESCRIPTION
		SOIC, SOT23-8, VSSOP, CDIP, PDIP, SO, TSSOP, CFP ⁽¹⁾		
IN1-	5	2	I	Negative input
IN1+	7	3	I	Positive input
IN2-	15	6	I	Negative input
IN2+	12	5	I	Positive input
OUT1	2	1	O	Output
OUT2	17	7	O	Output
V-	10	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	—	No internal connection
V+	20	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see [Section 3](#).

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage, $V_S = ([V_+] - [V_-])$	LM358B, LM358BA, LM2904B, LM2904BA			± 20 or 40	V
	LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V			± 16 or 32	
	LM2904			± 13 or 26	
Differential input voltage, V_{ID} ⁽²⁾	LM358B, LM358BA, LM2904B, LM2904BA, LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V		-32	32	V
	LM2904		-26	26	
Input voltage, V_I	Either input	LM358B, LM358BA, LM2904B, LM2904BA	-0.3	40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	-0.3	32	
		LM2904	-0.3	26	
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_S \leq 15 \text{ V}^{(3)}$				Unlimited	s
Operating ambient temperature, T_A	LM158, LM158A	-55	125		$^\circ\text{C}$
	LM258, LM258A	-25	85		
	LM358B, LM358BA	-40	85		
	LM358, LM358A	0	70		
	LM2904B, LM2904BA, LM2904, LM2904V	-40	125		
Operating virtual-junction temperature, T_J				150	$^\circ\text{C}$
Storage temperature, T_{stg}			-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at IN^+ , with respect to IN^- .
- (3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction.

6.2 ESD Ratings

		VALUE	UNIT
LM358B, LM358BA, LM2904B, AND LM2904BA			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1500	
LM158, LM258, LM358, LM158, LM258A, LM358A, LM2904, AND LM2904V			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, $V_S = ([V_+] - [V_-])$	LM358B, LM358BA, LM2904B, LM2904BA	3	36	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	3	30	
		LM2904	3	26	
V_{CM}	Common-mode voltage		V_-	$V_+ - 2$	V
T_A	Operating ambient temperature	LM358B, LM358BA	-40	85	°C
		LM2904B, LM2904BA, LM2904, LM2904V	-40	125	
		LM358, LM358A	0	70	
		LM258, LM258A	-20	85	
		LM158, LM158A	-55	125	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM258, LM258A, LM358, LM358A, LM358B, LM358BA, LM2904, LM2904B, LM2904BA, LM2904V ⁽²⁾						LM158, LM158A		UNIT	
	D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)		
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8PINS	20 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.7	181.4	80.9	116.9	171.7	164.3	84.0	112.4	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	66.9	69.4	70.4	62.5	68.8	98.1	56.9	63.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.9	102.9	57.4	68.6	99.2	82.1	57.5	100.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.2	11.8	40	21.9	11.5	11.4	51.7	35.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.2	101.2	56.9	67.6	97.9	81.7	57.1	93.3	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	10.6	22.3	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) For a listing of which devices are available in what packages, see [Section 3](#).

6.5 Electrical Characteristics: LM358B and LM358BA

$V_S = (V+) - (V-) = 5 V - 36 V (\pm 2.5 V - \pm 18 V)$, $T_A = 25^\circ C$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10k$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS} Input offset voltage	LM358B			± 0.3	± 3.0	mV	
		$T_A = -40^\circ C$ to $+85^\circ C$			± 4	mV	
	LM358BA				± 2.0	mV	
		$T_A = -40^\circ C$ to $+85^\circ C$			± 2.5	mV	
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ C$ to $+85^\circ C$ ⁽¹⁾			± 3.5	11	$\mu V/^\circ C$
PSRR	Power supply rejection ratio				± 2	15	$\mu V/V$
	Channel separation, dc	$f = 1$ kHz to 20 kHz			± 1		$\mu V/V$
INPUT VOLTAGE RANGE							
V_{CM} Common-mode voltage range	$V_S = 3$ V to 36 V			$(V-)$	$(V+) - 1.5$	V	
	$V_S = 5$ V to 36 V	$T_A = -40^\circ C$ to $+85^\circ C$		$(V-)$	$(V+) - 2$	V	
CMRR Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5$ V	$V_S = 3$ V to 36 V			20	100	$\mu V/V$
	$(V-) \leq V_{CM} \leq (V+) - 2.0$ V	$V_S = 5$ V to 36 V	$T_A = -40^\circ C$ to $+85^\circ C$		25	316	
INPUT BIAS CURRENT							
I_B Input bias current				± 10	± 35	nA	
	$T_A = -40^\circ C$ to $+85^\circ C$ ⁽¹⁾				± 50	nA	
I_{OS} Input offset current				0.5	4	nA	
	$T_A = -40^\circ C$ to $+85^\circ C$ ⁽¹⁾				5	nA	
dI_{OS}/dT	Input offset current drift	$T_A = -40^\circ C$ to $+85^\circ C$			10		$pA/^\circ C$
NOISE							
E_n	Input voltage noise	$f = 0.1$ to 10 Hz			3		μV_{PP}
e_n	Input voltage noise density	$f = 1$ kHz			40		nV/\sqrt{Hz}
INPUT IMPEDANCE							
Z_{ID}	Differential				10 0.1		$M\Omega pF$
Z_{IC}	Common-mode				4 1.5		$G\Omega pF$
OPEN-LOOP GAIN							
A_{OL} Open-loop voltage gain	$V_S = 15$ V; $V_O = 1$ V to 11 V; $R_L \geq 10$ k Ω , connected to (V-)			70	140		V/mV
		$T_A = -40^\circ C$ to $+85^\circ C$		35			V/mV
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.2		MHz
SR	Slew rate	$G = + 1$			0.5		V/ μ s
Θ_m	Phase margin	$G = + 1$, $R_L = 10$ k Ω , $C_L = 20$ pF			56		°
t_{OR}	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		μs
t_s	Settling time	To 0.1%, $V_S = 5$ V, 2-V step, $G = + 1$, $C_L = 100$ pF			4		μs
THD+N	Total harmonic distortion + noise	$G = + 1$, $f = 1$ kHz, $V_O = 3.53$ V _{RMS} , $V_S = 36$ V, $R_L = 100k$, $I_{OUT} \leq \pm 50$ μA , BW = 80 kHz			0.001		%
OUTPUT							
V_O Voltage output swing from rail	Positive rail (V+)	$I_{OUT} = 50$ μA		$I_{OUT} = 50$ μA	1.35	1.42	V
		$I_{OUT} = 1$ mA		$I_{OUT} = 1$ mA	1.4	1.48	V
		$I_{OUT} = 5$ mA ⁽¹⁾		$I_{OUT} = 5$ mA ⁽¹⁾	1.5	1.61	V
	Negative rail (V-)	$I_{OUT} = 50$ μA		$I_{OUT} = 50$ μA	100	150	mV
I_O Output current	$V_S = 15$ V; $V_O = V-$; $V_{ID} = 1$ V	$I_{OUT} = 1$ mA		$I_{OUT} = 1$ mA	0.75	1	V
		$V_S = 5$ V, $RL \leq 10$ k Ω connected to (V-)		$T_A = -40^\circ C$ to $+85^\circ C$	5	20	mV
		$T_A = -40^\circ C$ to $+85^\circ C$			-20	-30	
		$T_A = -40^\circ C$ to $+85^\circ C$			-10		
I_{SC} Short-circuit current	$V_S = 20$ V, $(V+) = 10$ V, $(V-) = -10$ V, $V_O = 0$ V	$I_{SC} = 100$ μA		$I_{SC} = 100$ μA	10	20	
		$T_A = -40^\circ C$ to $+85^\circ C$			5		
		$V_{ID} = -1$ V; $V_O = (V-) + 200$ mV			60	100	μA
C_{LOAD}	Capacitive load drive					100	pF
R_O	Open-loop output resistance	$f = 1$ MHz, $I_O = 0$ A				300	Ω

6.5 Electrical Characteristics: LM358B and LM358BA (continued)

$V_S = (V+) - (V-) = 5 \text{ V} - 36 \text{ V}$ ($\pm 2.5 \text{ V} - \pm 18 \text{ V}$), $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{k}$ connected to $V_S / 2$
(unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5 \text{ V}; I_O = 0 \text{ A}$			300	460
I_Q	Quiescent current per amplifier	$V_S = 36 \text{ V}; I_O = 0 \text{ A}$	$T_A = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$		800	μA

(1) Specified by characterization only.

6.6 Electrical Characteristics: LM2904B and LM2904BA

$V_S = (V+) - (V-) = 5 \text{ V} - 36 \text{ V}$ ($\pm 2.5 \text{ V} - \pm 18 \text{ V}$), $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, $R_L = 10\text{k}$ connected to $V_S/2$
(unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LM2904B		$I_{OUT} = 50 \mu\text{A}$	± 0.3	± 3.0	mV
				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$		± 4	mV
	Input offset voltage drift	LM2904BA				± 2.0	mV
				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$		± 3.0	mV
dV_{OS}/dT				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	± 3.5	12	$\mu\text{V}/^\circ\text{C}$
PSRR	Power Supply Rejection Ratio				± 2	15	$\mu\text{V}/\text{V}$
	Channel separation, dc	$f = 1 \text{ kHz}$ to 20 kHz				± 1	$\mu\text{V}/\text{V}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	$V_S = 3 \text{ V}$ to 36 V			$(V-)$	$(V+) - 1.5$	V
		$V_S = 5 \text{ V}$ to 36 V		$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	$(V-)$	$(V+) - 2$	V
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5 \text{ V}$	$V_S = 3 \text{ V}$ to 36 V		20	100	$\mu\text{V}/\text{V}$
		$(V-) \leq V_{CM} \leq (V+) - 2.0 \text{ V}$	$V_S = 5 \text{ V}$ to 36 V	$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	25	316	
INPUT BIAS CURRENT							
I_B	Input bias current				± 10	± 35	nA
					$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	± 50	nA
I_{OS}	Input offset current				0.5	4	nA
					$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	5	nA
dI_{OS}/dT	Input offset current drift			$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	10		$\text{pA}/^\circ\text{C}$
NOISE							
E_n	Input voltage noise	$f = 0.1$ to 10 Hz			3		μV_{PP}
e_n	Input voltage noise density	$f = 1 \text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$
INPUT IMPEDANCE							
Z_{ID}	Differential				10	$\parallel 0.1$	$\text{M}\Omega \parallel \text{pF}$
Z_{IC}	Common-mode				4	$\parallel 1.5$	$\text{G}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$V_S = 15 \text{ V}$; $V_O = 1 \text{ V}$ to 11 V ; $R_L \geq 10 \text{ k}\Omega$, connected to $(V-)$		$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	70	140	V/mV
					35		V/mV
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.2		MHz
SR	Slew rate	$G = +1$			0.5		$\text{V}/\mu\text{s}$
Θ_m	Phase margin	$G = +1$, $R_L = 10\text{k}\Omega$, $C_L = 20 \text{ pF}$			56		$^\circ$
t_{OR}	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		μs
t_s	Settling time	To 0.1%, $V_S = 5 \text{ V}$, 2-V Step, $G = +1$, $C_L = 100 \text{ pF}$			4		μs
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1 \text{ kHz}$, $V_O = 3.53 \text{ V}_{RMS}$, $V_S = 36 \text{ V}$, $R_L = 100\text{k}$, $I_{OUT} \leq \pm 50\mu\text{A}$, $BW = 80 \text{ kHz}$			0.001		%
OUTPUT							
V_O	Voltage output swing from rail	Positive Rail ($V+$)		$I_{OUT} = 50 \mu\text{A}$	1.35	1.42	V
				$I_{OUT} = 1 \text{ mA}$	1.4	1.48	V
				$I_{OUT} = 5 \text{ mA}$	1.5	1.61	V
		Negative Rail ($V-$)		$I_{OUT} = 50 \mu\text{A}$	100	150	mV
				$I_{OUT} = 1 \text{ mA}$	0.75	1	V
$V_S = 5 \text{ V}$, $R_L \leq 10 \text{ k}\Omega$ connected to $(V-)$				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	5	20	mV
I_O	Output current	Source ⁽¹⁾			-20	-30	mA
				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	-10		
		Sink ⁽¹⁾			10	20	
				$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	5		
$V_{ID} = -1 \text{ V}$; $V_O = (V-) + 200 \text{ mV}$					60	100	μA
I_{SC}	Short-circuit current	$V_S = 20 \text{ V}$, $(V+) = 10 \text{ V}$, $(V-) = -10 \text{ V}$, $V_O = 0 \text{ V}$			± 40	± 60	mA
C_{LOAD}	Capacitive load drive				100		pF
R_O	Open-loop output resistance	$f = 1 \text{ MHz}$, $I_O = 0 \text{ A}$			300		Ω
POWER SUPPLY							

$V_S = (V+) - (V-) = 5 \text{ V} - 36 \text{ V}$ ($\pm 2.5 \text{ V} - \pm 18 \text{ V}$), $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, $R_L = 10\text{k}$ connected to $V_S/2$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	$V_S = 5 \text{ V}$; $I_O = 0 \text{ A}$	$T_A = -40^\circ\text{C} \text{ to } +125^\circ\text{C}$	300	460	μA	
	Quiescent current per amplifier	$V_S = 36 \text{ V}$; $I_O = 0 \text{ A}$			800	μA	

(1) Specified by characterization only

6.7 Electrical Characteristics: LM358, LM358A

For $V_S = (V+) - (V-) = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾			MIN	TYP ⁽²⁾	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS} Input offset voltage	$V_S = 5 \text{ V to } 30 \text{ V}; V_{CM} = 0 \text{ V}; V_O = 1.4 \text{ V}$	LM358 LM358A	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	3	7	9	mV	
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	2	3	5		
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	7	7	20		
dV_{OS}/dT Input offset voltage drift	LM358 LM358A	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	65	100	120	dB	
PSRR Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5 \text{ V to } 30 \text{ V}$			65	100	120	dB	
V_{O1}/V_{O2} Channel separation	$f = 1 \text{ kHz to } 20 \text{ kHz}$			65	100	120	dB	
INPUT VOLTAGE RANGE								
V_{CM} Common-mode voltage range	$V_S = 5 \text{ V to } 30 \text{ V}$	LM358	(V-)	(V+) - 1.5	V			
	$V_S = 30 \text{ V}$	LM358A						
	$V_S = 5 \text{ V to } 30 \text{ V}$	LM358	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	(V-)				
	$V_S = 30 \text{ V}$	LM358A						
CMRR Common-mode rejection ratio	$V_S = 5 \text{ V to } 30 \text{ V}; V_{CM} = 0 \text{ V}$			65	80	100	dB	
INPUT BIAS CURRENT								
I_B Input bias current	$V_O = 1.4 \text{ V}$	LM358 LM358A	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-20	-250	-500	nA	
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-15	-100	-200		
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	2	50	150		
I_{OS} Input offset current	$V_O = 1.4 \text{ V}$	LM358 LM358A	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	2	30	75	nA	
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	10	300	300		
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	10	300	300		
dI_{OS}/dT Input offset current drift	LM358A	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					pA/°C	
NOISE								
e_n Input voltage noise density	$f = 1 \text{ kHz}$			40	40	40	nV/√Hz	
OPEN-LOOP GAIN								
A_{OL} Open-loop voltage gain	$V_S = 15 \text{ V}; V_O = 1 \text{ V to } 11 \text{ V}; R_L \geq 2 \text{ k}\Omega$			25	100	100	V/mV	
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	15				
FREQUENCY RESPONSE								
GBW Gain bandwidth product				0.7	0.7	0.7	MHz	
SR Slew rate	$G = +1$			0.3	0.3	0.3	V/μs	
OUTPUT								
V_O Voltage output swing from rail	Positive rail	$V_S = 30 \text{ V}; R_L = 2 \text{ k}\Omega$	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	4	4	4	V	
		$V_S = 30 \text{ V}; R_L \geq 10 \text{ k}\Omega$		2	3	3		
		$V_S = 5 \text{ V}; R_L \geq 2 \text{ k}\Omega$		1.5				
I_O Output current	Negative rail	$V_S = 5 \text{ V}; R_L \leq 10 \text{ k}\Omega$	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	5	20	20	mV	
		Source		-20	-30	-30		
			LM358A			-60		
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-10				
		Sink		10	20	20		
			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	5				
I_{SC} Short-circuit current	$V_S = 10 \text{ V}; V_O = V_S / 2$			12	30	30	μA	
					±40	±60		
POWER SUPPLY								
I_Q Quiescent current per amplifier	$V_O = 2.5 \text{ V}; I_O = 0 \text{ A}$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	350	600	600	μA	
				500	1000	1000		

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM358 and LM358A.
- (2) All typical values are $T_A = 25^\circ\text{C}$.

6.8 Electrical Characteristics: LM2904, LM2904V

For $V_S = (V+) - (V-) = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾			MIN	TYP ⁽²⁾	MAX	UNIT
OFFSET VOLTAGE							
V_{OS} Input offset voltage	$V_S = 5 \text{ V}$ to maximum; $V_{CM} = 0 \text{ V}$; $V_O = 1.4 \text{ V}$	Non-A suffix devices T _A = -40°C to 125°C A-suffix devices T _A = -40°C to 125°C	3	7	mV		
			10	1			
			2	4			
dV_{OS}/dT Input offset voltage drift		T _A = -40°C to 125°C	7		$\mu\text{V}/^\circ\text{C}$		
PSRR Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5 \text{ V}$ to 30 V		65	100			dB
V_{O1}/V_{O2} Channel separation	$f = 1 \text{ kHz}$ to 20 kHz			120			dB
INPUT VOLTAGE RANGE							
V_{CM} Common-mode voltage range	$V_S = 5 \text{ V}$ to maximum	T _A = -40°C to 125°C	(V-)	(V+) – 1.5	V		
			(V-)	(V+) – 2			
CMRR Common-mode rejection ratio	$V_S = 5 \text{ V}$ to maximum; $V_{CM} = 0 \text{ V}$		65	80			dB
INPUT BIAS CURRENT							
I_B Input bias current	$V_O = 1.4 \text{ V}$	T _A = -40°C to 125°C	–20	–250	nA		
			–500				
I_{OS} Input offset current	$V_O = 1.4 \text{ V}$	Non-V suffix device T _A = -40°C to 125°C V-suffix device T _A = -40°C to 125°C	2	50	nA		
			300				
			2	50			
dI_{OS}/dT Input offset current drift		T _A = -40°C to 125°C	150				pA/°C
NOISE							
e_n Input voltage noise density	$f = 1 \text{ kHz}$			40			nV/ $\sqrt{\text{Hz}}$
OPEN-LOOP GAIN							
A_{OL} Open-loop voltage gain	$V_S = 15 \text{ V}$; $V_O = 1 \text{ V}$ to 11 V ; $R_L \geq 2 \text{ k}\Omega$	T _A = -40°C to 125°C	25	100	V/mV		
			15				
FREQUENCY RESPONSE							
GBW Gain bandwidth product				0.7			MHz
SR Slew rate	G = +1			0.3			V/ μs
OUTPUT							
V_O Voltage output swing from rail	Positive rail	R _L ≥ 10 kΩ Non-V suffix device V _S = maximum; R _L = 2 kΩ V _S = maximum; R _L ≥ 10 kΩ V-suffix device V _S = maximum; R _L = 2 kΩ V _S = maximum; R _L ≥ 10 kΩ	T _A = -40°C to 125°C		V _S – 1.5	V	
					4		
					2		
					6		
					4		
I_O Output current	Negative rail	V _S = 5 V; R _L ≤ 10 kΩ	T _A = -40°C to 125°C		5	mV	
					20		
					–20		
					–30		
I_O Output current	Source	T _A = -40°C to 125°C	–10		mA		
					10		
					20		
I_O Output current	Sink	T _A = -40°C to 125°C	5		μA		
					30		
I_{SC} Short-circuit current	V _S = 10 V; $V_O = V_S / 2$	V _{ID} = -1 V	Non-V suffix device		12	40	mA
			V-suffix device		40		
POWER SUPPLY							
I_Q Quiescent current per amplifier	V _O = 2.5 V; $I_O = 0 \text{ A}$ V _S = maximum; V_O = maximum / 2; $I_O = 0 \text{ A}$	T _A = -40°C to 125°C	350	600	μA		
			500	1000			

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
Maximum V_S for testing purposes is 26 V for LM2904 and 32 V for LM2904V.

- (2) All typical values are T_A = 25°C.

6.9 Electrical Characteristics: LM158, LM158A

For $V_S = (V+) - (V-) = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾			MIN	TYP ⁽²⁾	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_S = 5 \text{ V}$ to 30 V ; $V_{CM} = 0 \text{ V}$; $V_O = 1.4 \text{ V}$	LM158		3	5		mV
				$T_A = -55^\circ\text{C}$ to 125°C		7		
			LM158A			2		
dV_{OS}/dT	Input offset voltage drift		LM158	$T_A = -55^\circ\text{C}$ to 125°C	7			$\mu\text{V}/^\circ\text{C}$
			LM158A	$T_A = -55^\circ\text{C}$ to 125°C	7	15 ⁽³⁾		
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5 \text{ V}$ to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	$f = 1 \text{ kHz}$ to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	$V_S = 5 \text{ V}$ to 30 V	LM158		(V-)	(V+) – 1.5		V
		$V_S = 30 \text{ V}$	LM158A					
		$V_S = 5 \text{ V}$ to 30 V	LM158	$T_A = -55^\circ\text{C}$ to 125°C	(V-)	(V+) – 2		
		$V_S = 30 \text{ V}$	LM158A					
CMRR	Common-mode rejection ratio	$V_S = 5 \text{ V}$ to 30 V ; $V_{CM} = 0 \text{ V}$			70	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	$V_O = 1.4 \text{ V}$	LM158		-20	-150		nA
				$T_A = -55^\circ\text{C}$ to 125°C		-300		
			LM158A			-15	-50	
I_{OS}	Input offset current	$V_O = 1.4 \text{ V}$	LM158		2	30		nA
				$T_A = -55^\circ\text{C}$ to 125°C		100		
			LM158A	$T_A = -55^\circ\text{C}$ to 125°C	2	10	30	
dI_{OS}/dT	Input offset current drift				10			$\text{pA}/^\circ\text{C}$
			LM158A	$T_A = -55^\circ\text{C}$ to 125°C		200		
NOISE								
e_n	Input voltage noise density	$f = 1 \text{ kHz}$				40		$\text{nV}/\sqrt{\text{Hz}}$
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15 \text{ V}$; $V_O = 1 \text{ V}$ to 11 V ; $R_L \geq 2 \text{ k}\Omega$			50	100		V/mV
				$T_A = -55^\circ\text{C}$ to 125°C	25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	$G = +1$				0.3		$\text{V}/\mu\text{s}$
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	$V_S = 30 \text{ V}$; $R_L = 2 \text{ k}\Omega$	$T_A = -55^\circ\text{C}$ to 125°C		4		V
			$V_S = 30 \text{ V}$; $R_L \geq 10 \text{ k}\Omega$			2	3	
			$V_S = 5 \text{ V}$; $R_L \geq 2 \text{ k}\Omega$				1.5	
I_O	Output current	Negative rail	$V_S = 5 \text{ V}$; $R_L \leq 10 \text{ k}\Omega$	$T_A = -55^\circ\text{C}$ to 125°C	5	20		mA
					-20	-30		
			Source	LM158A			-60	
					$T_A = -55^\circ\text{C}$ to 125°C	-10		
			$V_S = 15 \text{ V}$; $V_O = 15 \text{ V}$; $V_{ID} = -1 \text{ V}$	Sink		10	20	
I_{SC}	Short-circuit current	$V_S = 10 \text{ V}$; $V_O = V_S / 2$	$T_A = -55^\circ\text{C}$ to 125°C		5			μA
					12	30		

6.9 Electrical Characteristics: LM158, LM158A (continued)

For $V_S = (V+) - (V-) = 5$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
POWER SUPPLY					
I_Q Quiescent current per amplifier	$V_O = 2.5$ V; $I_O = 0$ A $V_S = 30$ V; $V_O = 15$ V; $I_O = 0$ A	$T_A = -55^\circ\text{C}$ to 125°C	350 500	600 1000	μA

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
Maximum V_S for testing purposes is 30 V for LM158 and LM158A.
- (2) All typical values are $T_A = 25^\circ\text{C}$.
- (3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Electrical Characteristics: LM258, LM258A

For $V_S = (V+) - (V-) = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾			MIN	TYP ⁽²⁾	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_S = 5 \text{ V}$ to 30 V ; $V_{CM} = 0 \text{ V}$; $V_O = 1.4 \text{ V}$	LM258		3	5		mV
				$T_A = -25^\circ\text{C}$ to 85°C		7		
			LM258A		2	3		
dV_{OS}/dT	Input offset voltage drift		LM258	$T_A = -25^\circ\text{C}$ to 85°C		4		$\mu\text{V}/^\circ\text{C}$
				$T_A = -25^\circ\text{C}$ to 85°C	7			
			LM258A		7	15		
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5 \text{ V}$ to 30 V			65	100		dB
V_{O1}/V_{O2}	Channel separation	$f = 1 \text{ kHz}$ to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	$V_S = 5 \text{ V}$ to 30 V	LM258		(V-)	(V+) – 1.5		V
		$V_S = 30 \text{ V}$	LM258A					
		$V_S = 5 \text{ V}$ to 30 V	LM258	$T_A = -25^\circ\text{C}$ to 85°C	(V-)	(V+) – 2		
		$V_S = 30 \text{ V}$	LM258A					
CMRR	Common-mode rejection ratio	$V_S = 5 \text{ V}$ to 30 V ; $V_{CM} = 0 \text{ V}$			70	80		dB
INPUT BIAS CURRENT								
I_B	Input bias current	$V_O = 1.4 \text{ V}$	LM258		-20	-150		nA
				$T_A = -25^\circ\text{C}$ to 85°C		-300		
			LM258A		-15	-80		
I_{OS}	Input offset current	$V_O = 1.4 \text{ V}$	LM258	$T_A = -25^\circ\text{C}$ to 85°C		2	30	nA
				$T_A = -25^\circ\text{C}$ to 85°C		100		
			LM258A	$T_A = -25^\circ\text{C}$ to 85°C	2	15	30	
dI_{OS}/dT	Input offset current drift		LM258A	$T_A = -25^\circ\text{C}$ to 85°C		10	200	pA/°C
NOISE								
e_n	Input voltage noise density	$f = 1 \text{ kHz}$				40		nV/ $\sqrt{\text{Hz}}$
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15 \text{ V}$; $V_O = 1 \text{ V}$ to 11 V ; $R_L \geq 2 \text{ k}\Omega$			50	100		V/mV
				$T_A = -25^\circ\text{C}$ to 85°C		25		
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	$G = +1$				0.3		V/ μs
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	$V_S = 30 \text{ V}$; $R_L = 2 \text{ k}\Omega$	$T_A = -25^\circ\text{C}$ to 85°C		4		V
			$V_S = 30 \text{ V}$; $R_L \geq 10 \text{ k}\Omega$			2	3	
			$V_S = 5 \text{ V}$; $R_L \geq 2 \text{ k}\Omega$			1.5		
I_O	Output current	Negative rail	$V_S = 5 \text{ V}$; $R_L \leq 10 \text{ k}\Omega$	$T_A = -25^\circ\text{C}$ to 85°C		5	20	mV
					-20	-30		
			Source	LM258A			-60	
					$T_A = -25^\circ\text{C}$ to 85°C	-10		
			$V_S = 15 \text{ V}$; $V_O = 15 \text{ V}$; $V_{ID} = -1 \text{ V}$	Sink		10	20	
I_{SC}	Short-circuit current	$V_S = 10 \text{ V}$; $V_O = V_S / 2$		$T_A = -25^\circ\text{C}$ to 85°C		5		μA
						12	30	
POWER SUPPLY								
I_Q	Quiescent current per amplifier	$V_O = 2.5 \text{ V}$; $I_O = 0 \text{ A}$	$V_S = 30 \text{ V}$; $V_O = 15 \text{ V}$; $I_O = 0 \text{ A}$	$T_A = -25^\circ\text{C}$ to 85°C		350	600	μA
						500	1000	

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM258 and LM258A.
(2) All typical values are $T_A = 25^\circ\text{C}$.

6.11 Typical Characteristics: LM358B and LM2904B

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

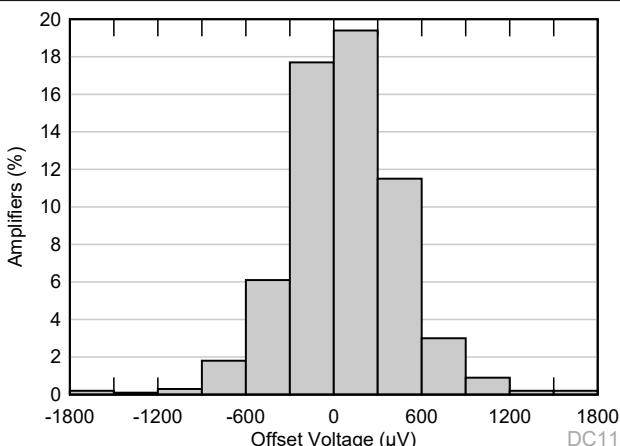


Figure 6-1. Offset Voltage Production Distribution

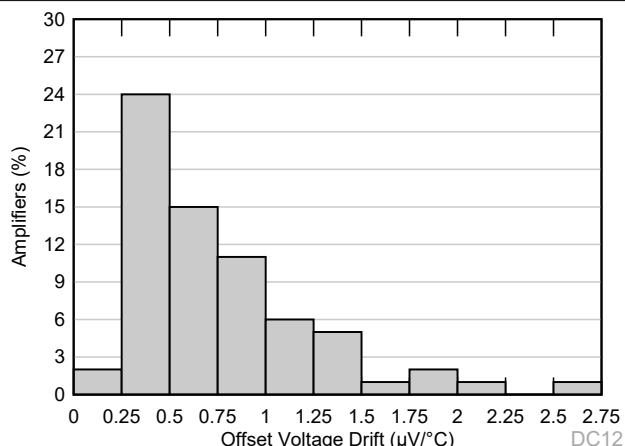


Figure 6-2. Offset Voltage Drift Distribution

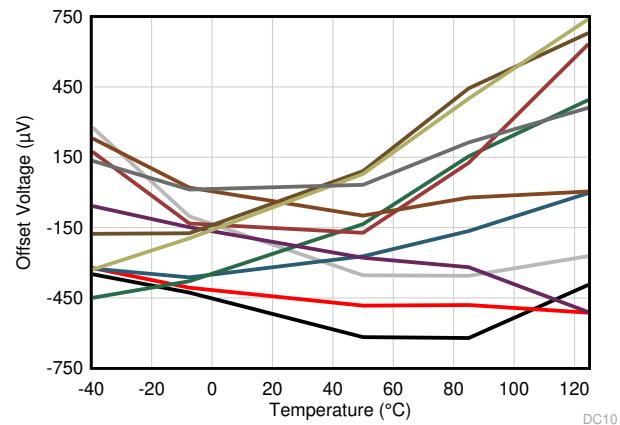


Figure 6-3. Offset Voltage vs Temperature

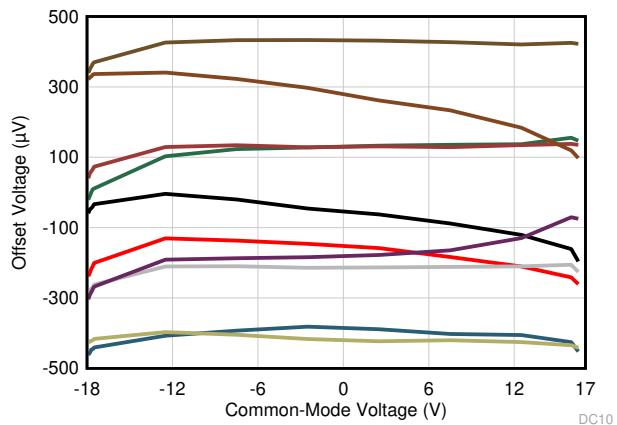


Figure 6-4. Offset Voltage vs Common-Mode Voltage

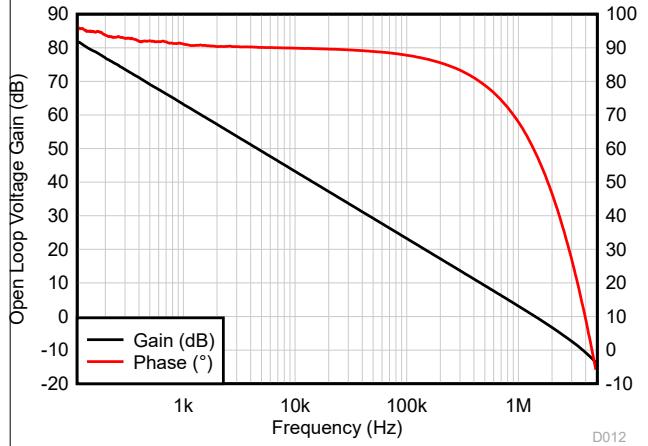


Figure 6-5. Open-Loop Gain and Phase vs Frequency

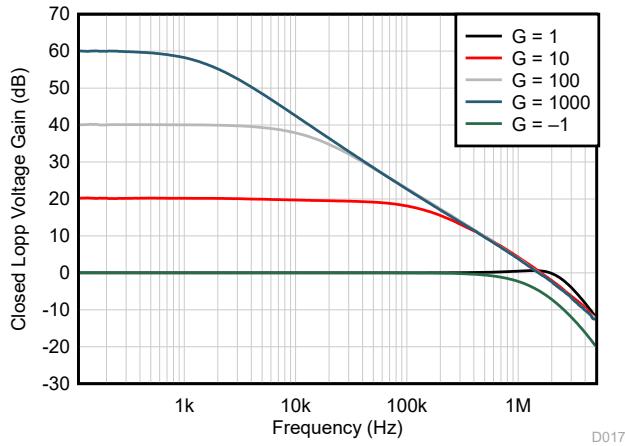


Figure 6-6. Closed-Loop Gain vs Frequency

6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

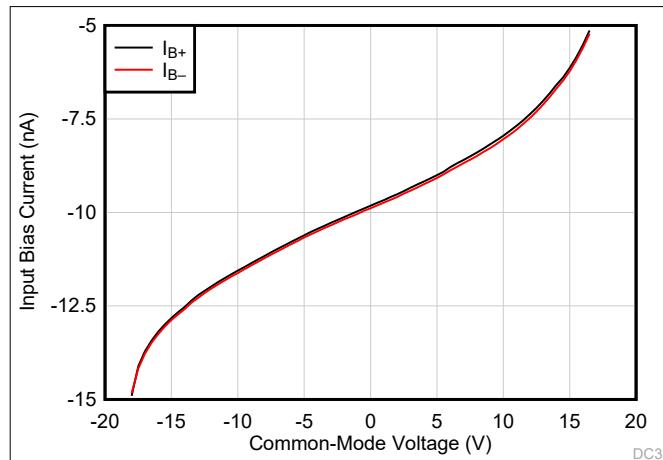


Figure 6-7. Input Bias Current vs Common-Mode Voltage

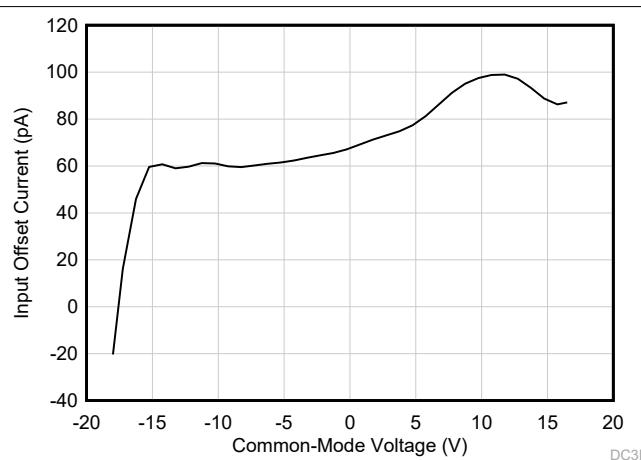


Figure 6-8. Input Offset Current vs Common-Mode Voltage

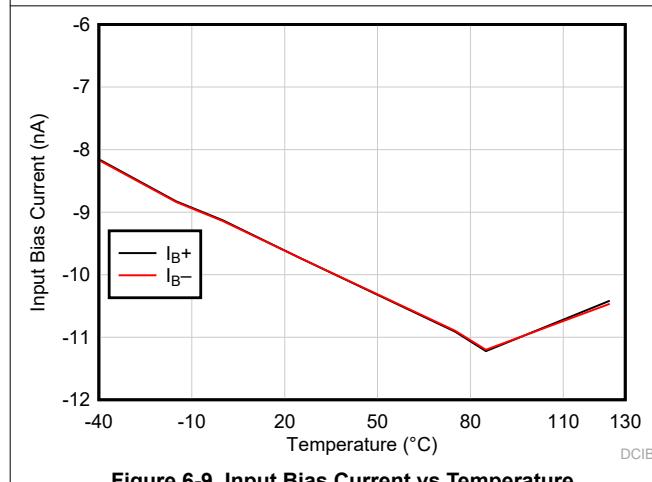


Figure 6-9. Input Bias Current vs Temperature

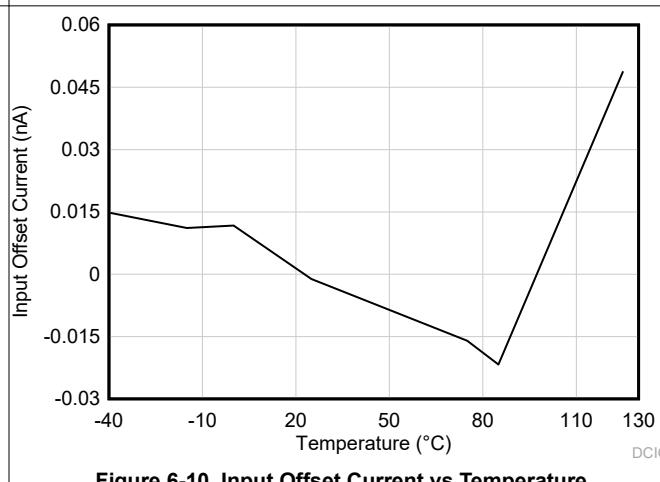


Figure 6-10. Input Offset Current vs Temperature

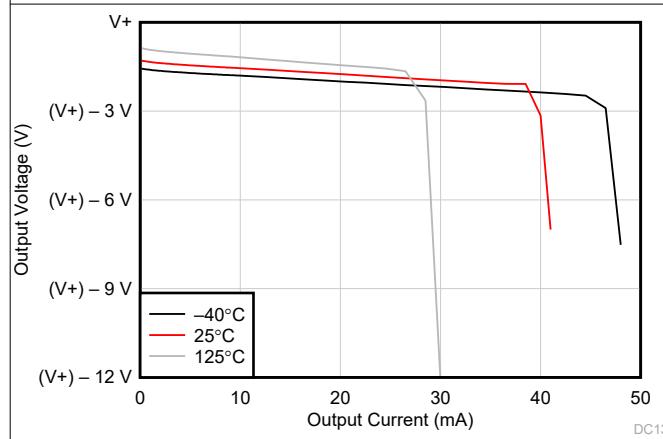


Figure 6-11. Output Voltage Swing vs Output Current (Sourcing)

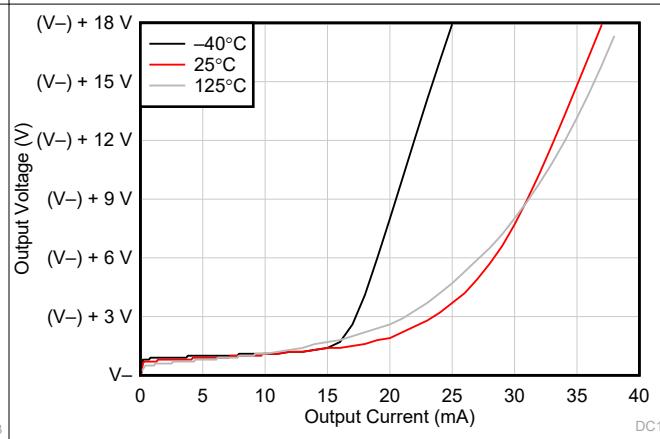
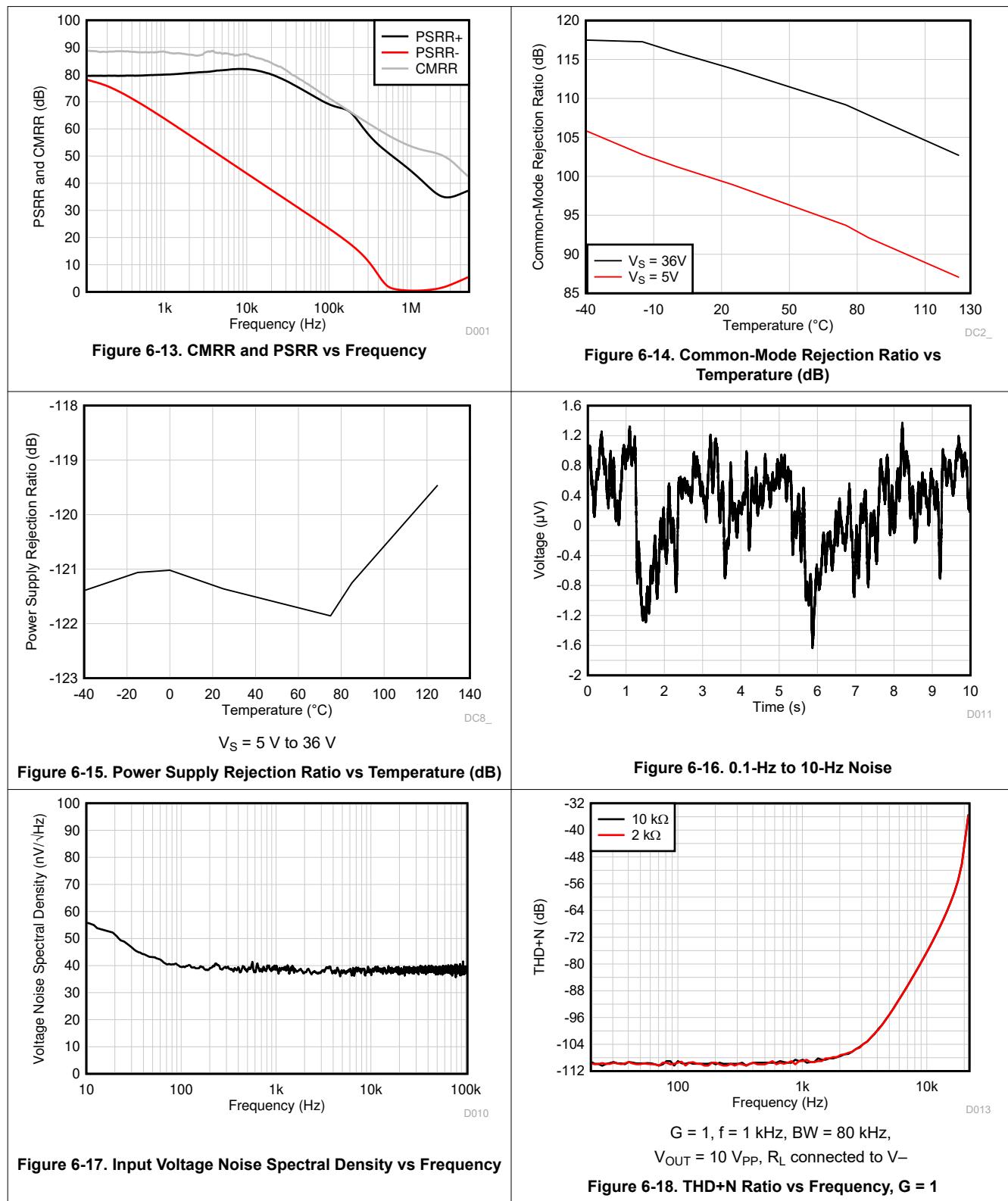


Figure 6-12. Output Voltage Swing vs Output Current (Sinking)

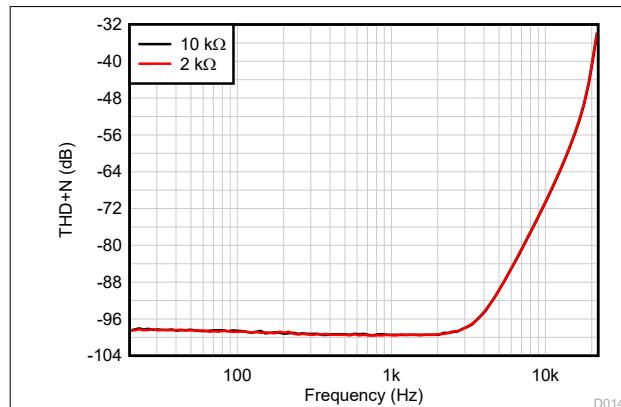
6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.11 Typical Characteristics: LM358B and LM2904B (continued)

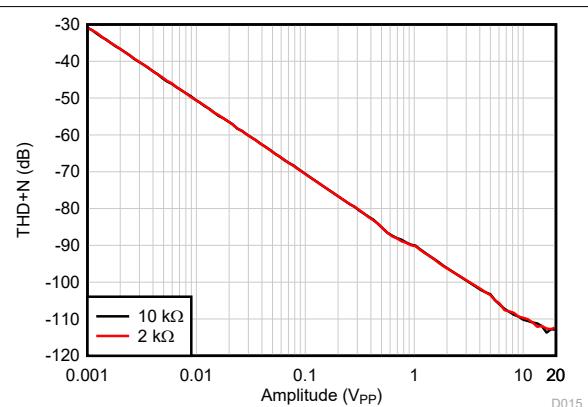
This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 $V_{OUT} = 10\text{ V}_{PP}$, R_L connected to V_-

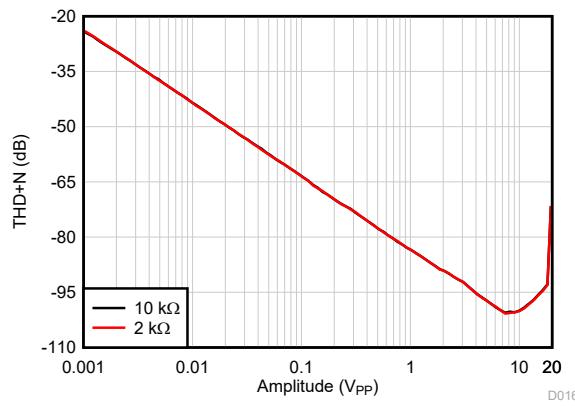
See Figure 7-3

Figure 6-19. THD+N Ratio vs Frequency, $G = -1$



$G = 1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-

Figure 6-20. THD+N vs Output Amplitude, $G = 1$



$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-

See Figure 7-3

Figure 6-21. THD+N vs Output Amplitude, $G = -1$

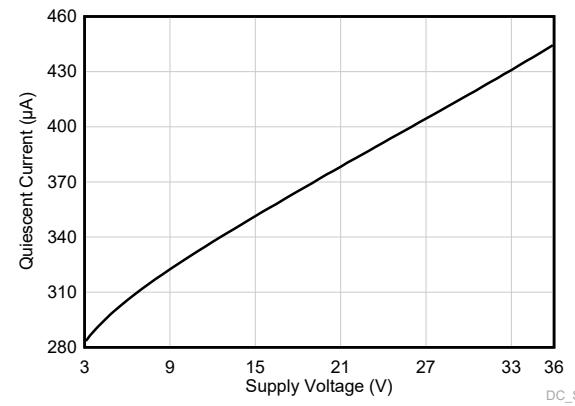


Figure 6-22. Quiescent Current vs Supply Voltage

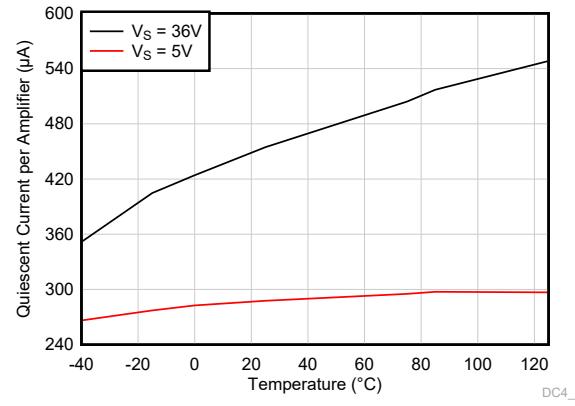


Figure 6-23. Quiescent Current vs Temperature

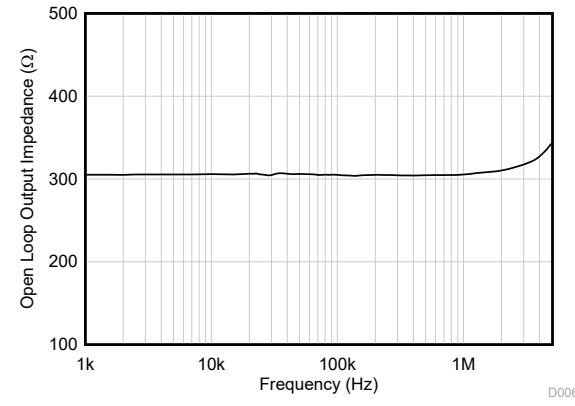
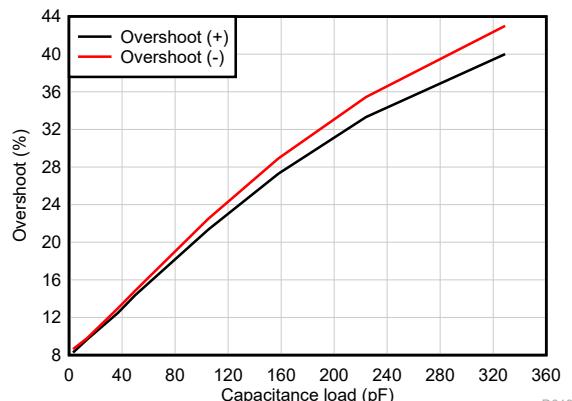


Figure 6-24. Open-Loop Output Impedance vs Frequency

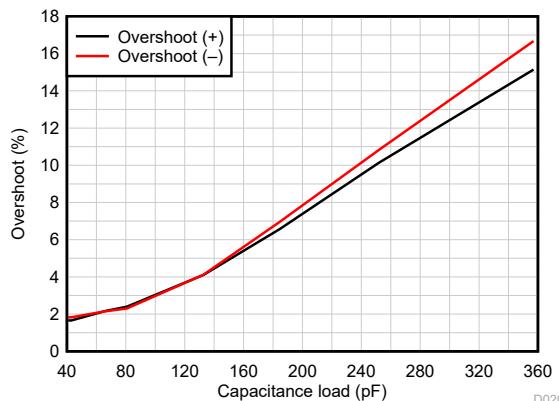
6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



$G = 1$, 100-mV output step, $R_L = \text{open}$

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



$G = -1$, 100-mV output step, $R_L = \text{open}$

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

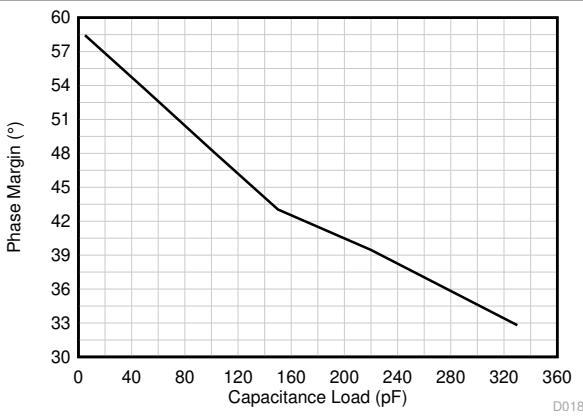
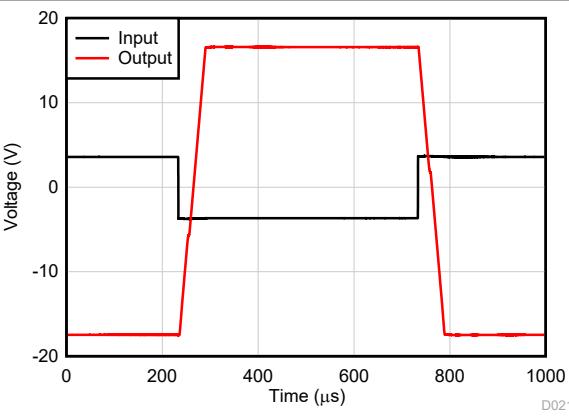
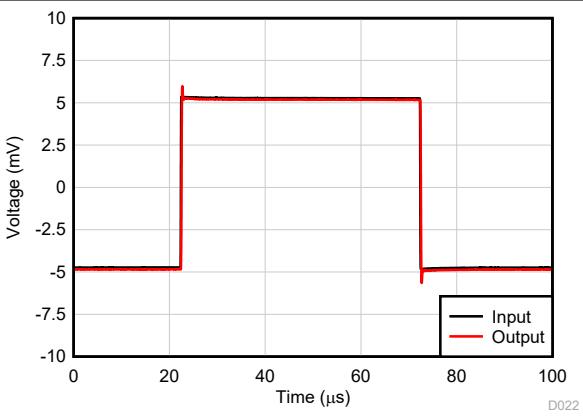


Figure 6-27. Phase Margin vs Capacitive Load



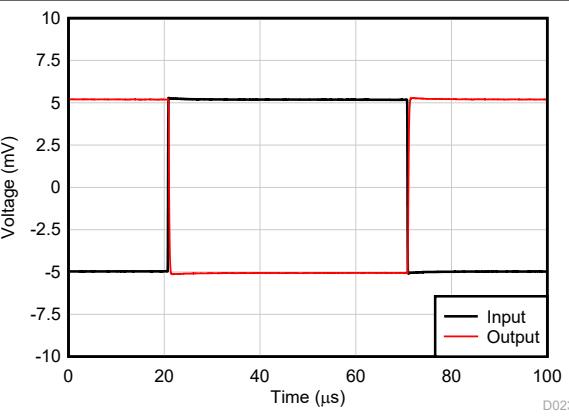
$G = -10$

Figure 6-28. Overload Recovery



$G = 1$, $R_L = \text{open}$

Figure 6-29. Small-Signal Step Response, $G = 1$



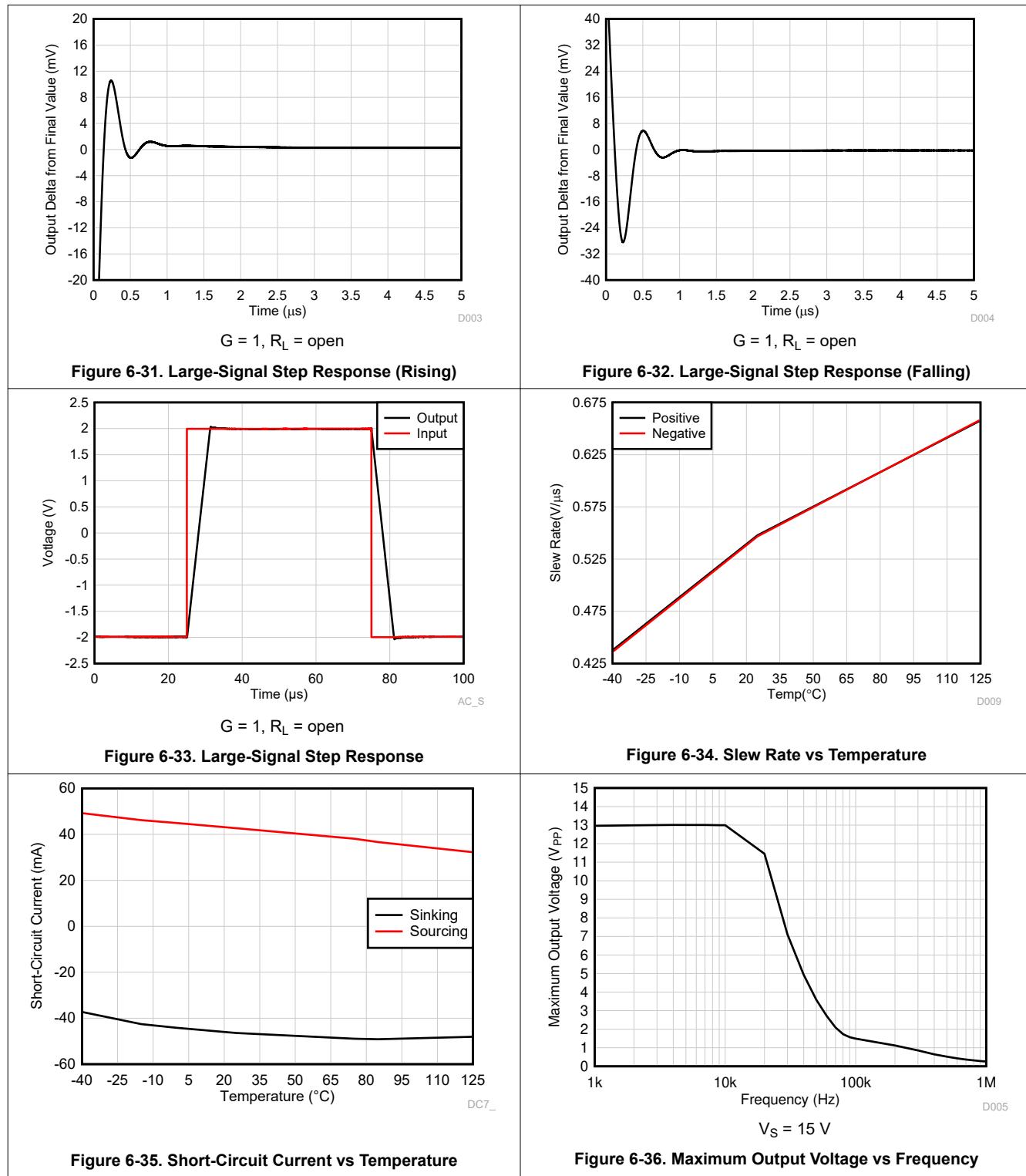
$G = -1$, $R_L = \text{open}$, $R_{FB} = 10\text{K}$

See Figure 7-3

Figure 6-30. Small-Signal Step Response, $G = -1$

6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36 \text{ V} (\pm 18 \text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10 \text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

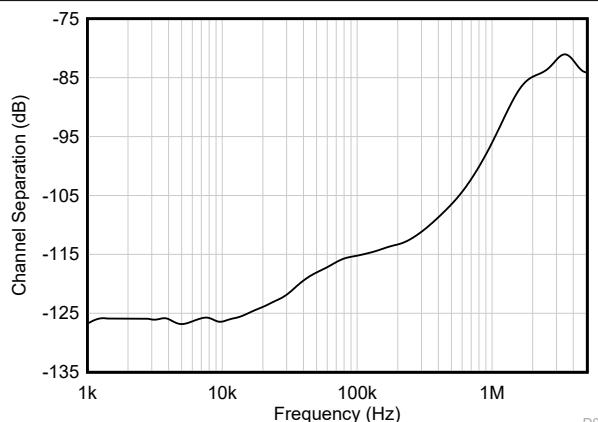


Figure 6-37. Channel Separation vs Frequency

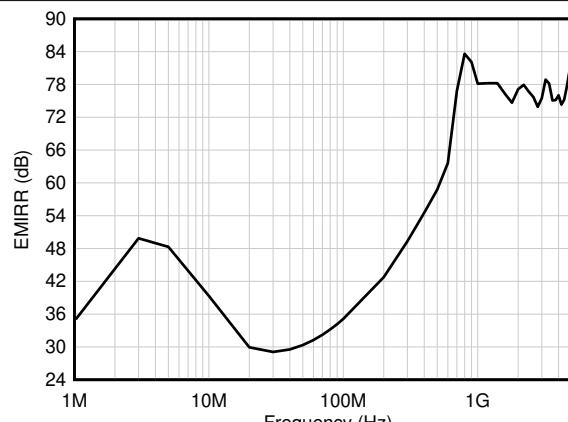


Figure 6-38. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

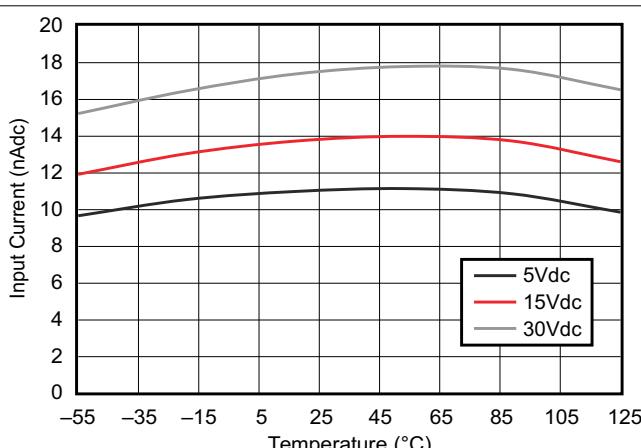


Figure 6-39. Input Current vs Temperature

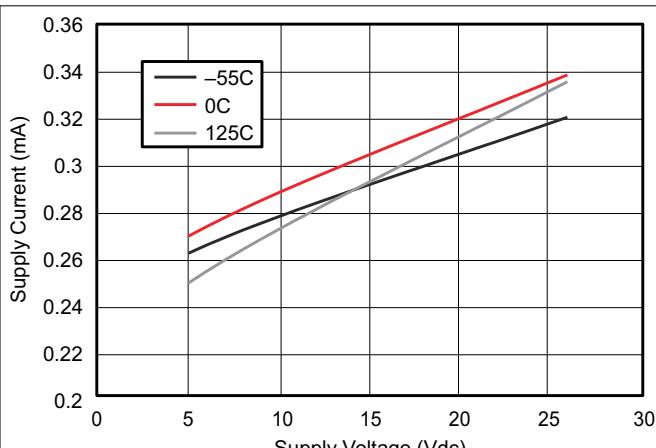


Figure 6-40. Supply Current vs Supply Voltage

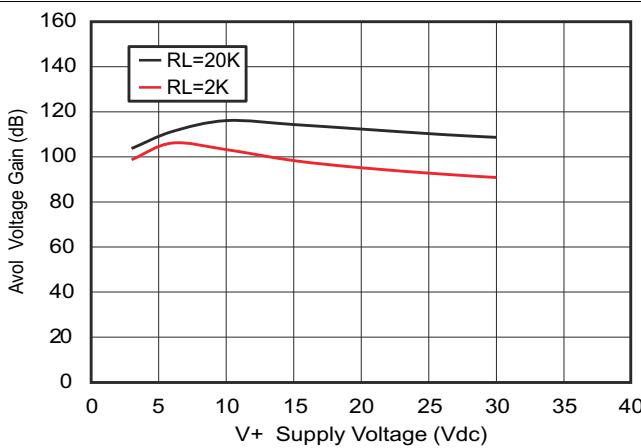


Figure 6-41. Voltage Gain vs Supply Voltage

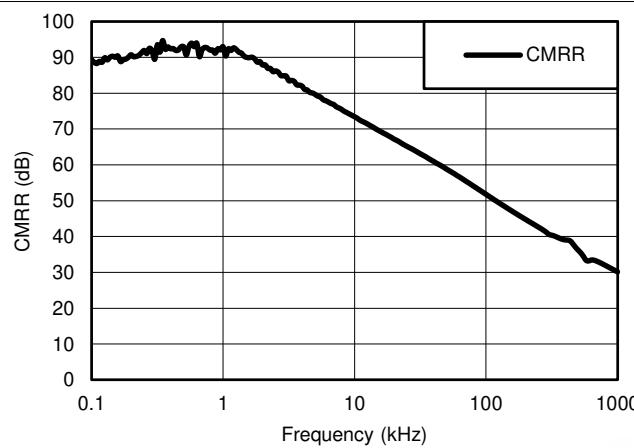


Figure 6-42. Common-Mode Rejection Ratio vs Frequency

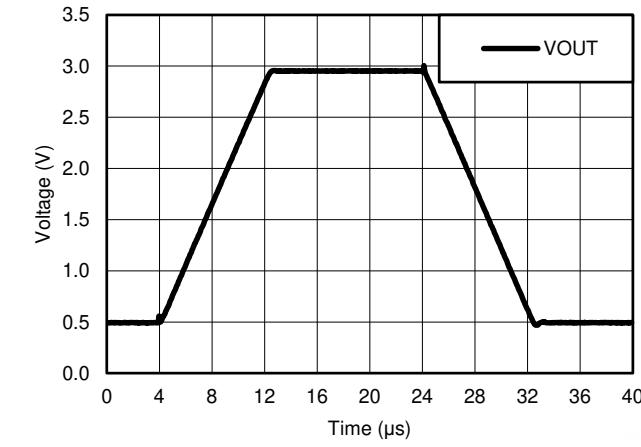


Figure 6-43. Voltage Follower Large Signal Response (50 pF)

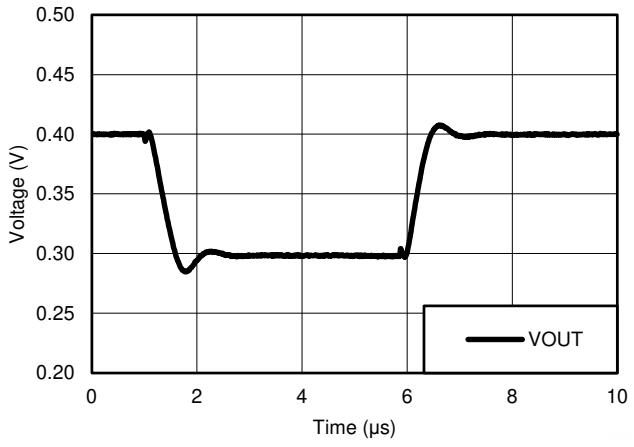


Figure 6-44. Voltage Follower Small Signal Response (50 pF)

6.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V (continued)

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

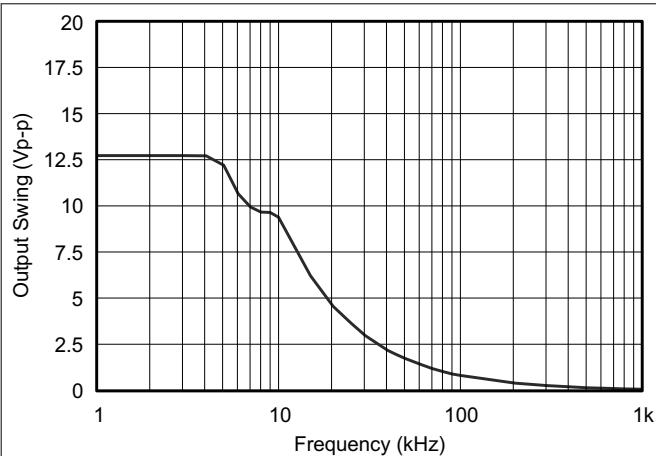


Figure 6-45. Maximum Output Swing vs Frequency ($V_{CC} = 15$ V)

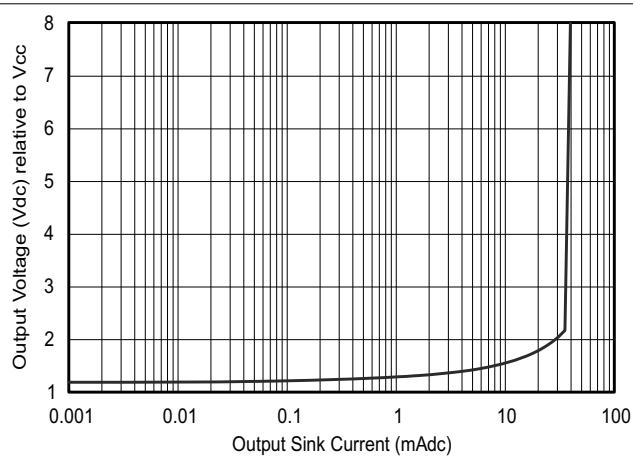


Figure 6-46. Output Sourcing Characteristics

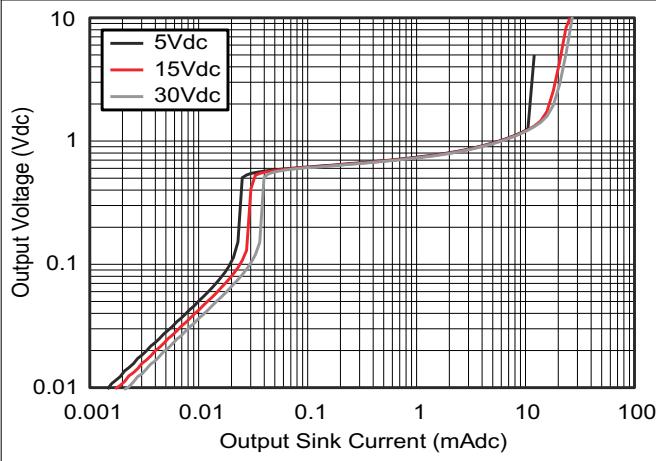


Figure 6-47. Output Sinking Characteristics

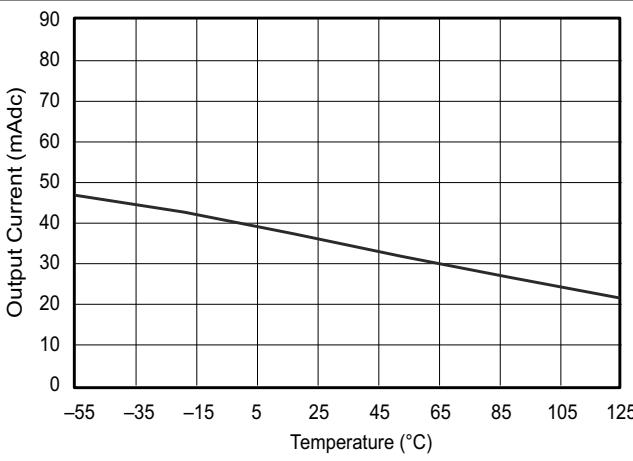


Figure 6-48. Source Current Limiting

7 Parameter Measurement Information

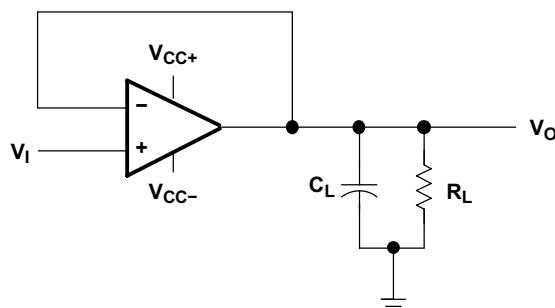


Figure 7-1. Unity-Gain Amplifier

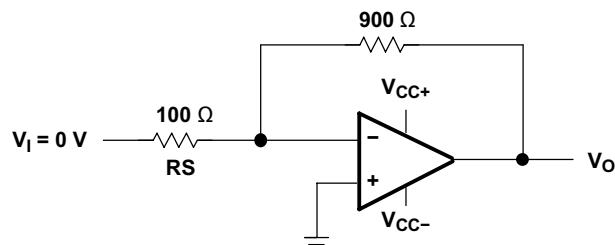


Figure 7-2. Noise-Test Circuit

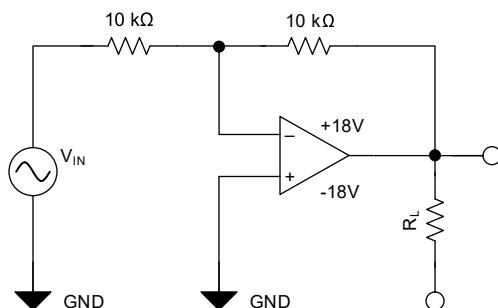


Figure 7-3. Test Circuit, $G = -1$, for THD+N and Small-Signal Step Response

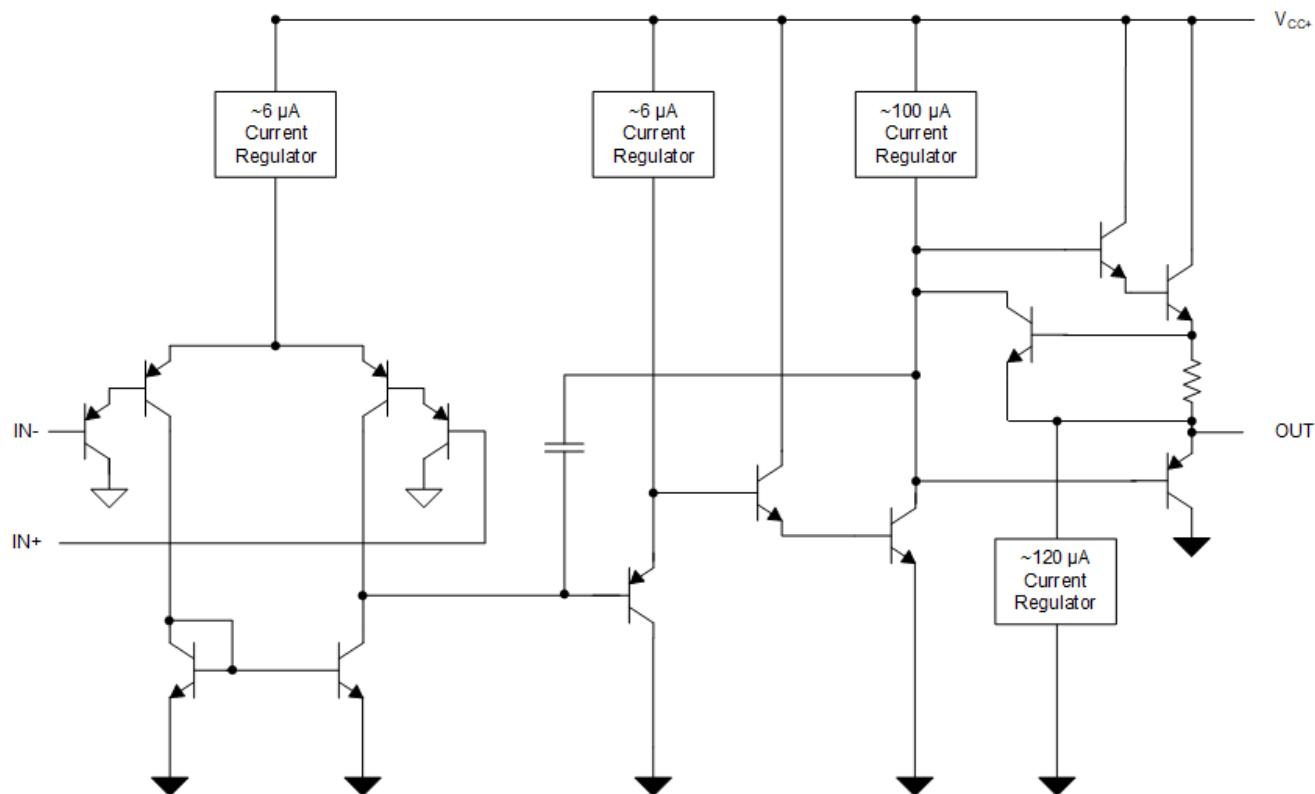
8 Detailed Description

8.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in [Section 6.3](#) and V_S is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ±5-V supplies.

8.2 Functional Block Diagram: LM358B, LM358BA, LM2904B, LM2904BA



8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (B Version).

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate (B Version).

8.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_S - 1.5$ V ($V_S - 2$ V across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V_- then input current should be limited to 1 mA and the output phase is undefined.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

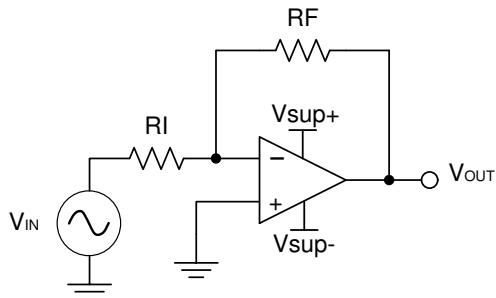


Figure 9-1. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliampere range. This ensures the part does not draw too much current. This example uses $10\text{ k}\Omega$ for R_I which means $36\text{ k}\Omega$ is used for R_F . This was determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

9.2.3 Application Curve

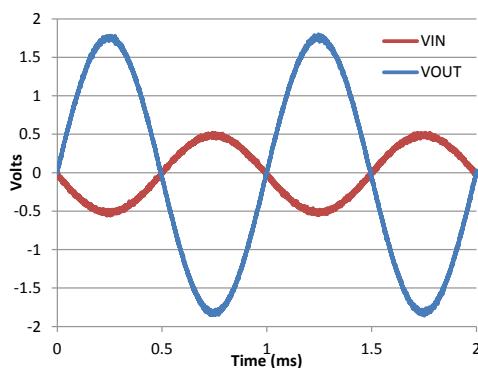


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see [Section 6.1](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 11](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in [Section 11.2](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

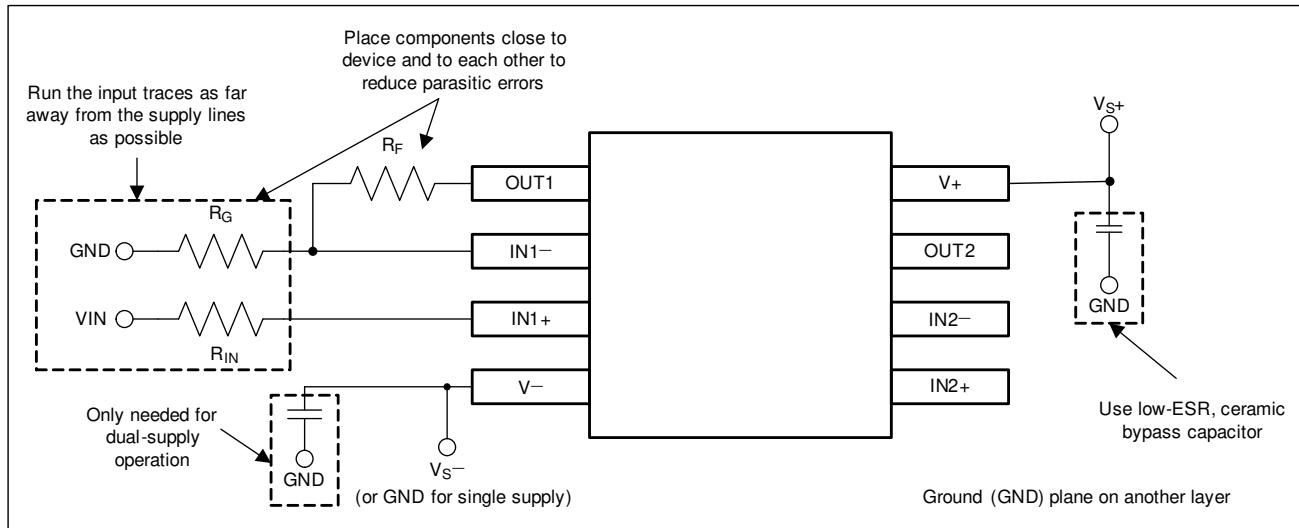


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

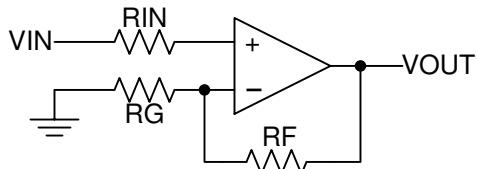


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	Samples
5962-8771001PA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
5962-87710022A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	Samples
5962-8771002PA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158AFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	Samples
LM158AJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158AJG	Samples
LM158AJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158FKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	Samples
LM158JG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158JG	Samples
LM158JGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	(M3L, M3P, M3S, M3 U)	Samples
LM258ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	Samples
LM258APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2U)	Samples
LM258DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258DRG3	OBsolete	SOIC	D	8	TBD		Call TI	Call TI	-25 to 85	LM258	
LM258DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM258PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904BAIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904A	Samples
LM2904BAIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	28CB	Samples
LM2904BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BA	Samples
LM2904BAIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BA	Samples
LM2904BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	28BB	Samples
LM2904BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	Samples
LM2904BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	Samples
LM2904DE4	NRND			75	TBD		Call TI	Call TI	-40 to 125		
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MBU)	Samples
LM2904DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRG3	OBsolete	SOIC	D	8	TBD		Call TI	Call TI	-40 to 125	LM2904	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904DRG4	OBsolete	SOIC	D	8	TBD	Call TI	Call TI	-40 to 125	LM2904		
LM2904P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG3	OBsolete	TSSOP	PW	8	TBD	Call TI	Call TI	-40 to 125	L2904		
LM2904PWRG4-JF	OBsolete	TSSOP	PW	8	TBD	Call TI	Call TI	-40 to 125	L2904		
LM2904QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QDRG4	OBsolete	SOIC	D	8	TBD	Call TI	Call TI	-40 to 125	2904Q1		
LM2904VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM358ADE4	NRND			75	TBD	Call TI	Call TI	0 to 70			
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6U)	Samples
LM358ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358ADRG4	OBsolete	SOIC	D	8	TBD	Call TI	Call TI	0 to 70	LM358A		
LM358AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APW	OBsolete	TSSOP	PW	8	TBD	Call TI	Call TI	0 to 70	L358A		
LM358APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358BAIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	358BA	Samples
LM358BAIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	28DB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L358BA	Samples
LM358BAIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L358BA	Samples
LM358BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358	Samples
LM358BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	358B	Samples
LM358BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	Samples
LM358BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	Samples
LM358D	OBsolete	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	LM358	
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5U)	Samples
LM358DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRG3	OBsolete	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	LM358	
LM358DRG4	OBsolete	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	LM358	
LM358P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PE3	OBsolete	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	LM358P	
LM358PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PW	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	L358	
LM358PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG3	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	L358	
LM358PWRG4	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	L358	
LM358PWRG4-JF	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	L358	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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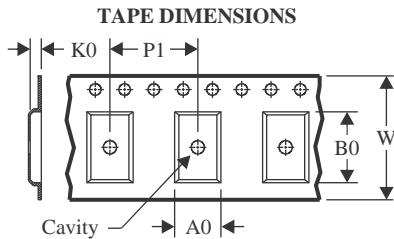
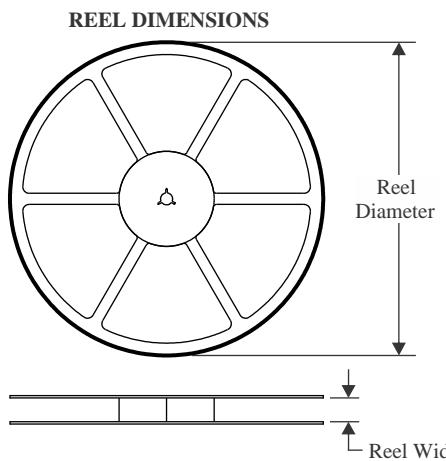
OTHER QUALIFIED VERSIONS OF LM258A, LM2904, LM2904B, LM2904BA :

- Automotive : [LM2904-Q1](#), [LM2904B-Q1](#), [LM2904BA-Q1](#)
- Enhanced Product : [LM258A-EP](#), [LM2904-EP](#)

NOTE: Qualified Version Definitions:

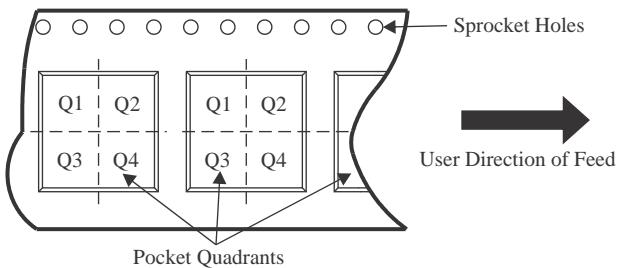
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

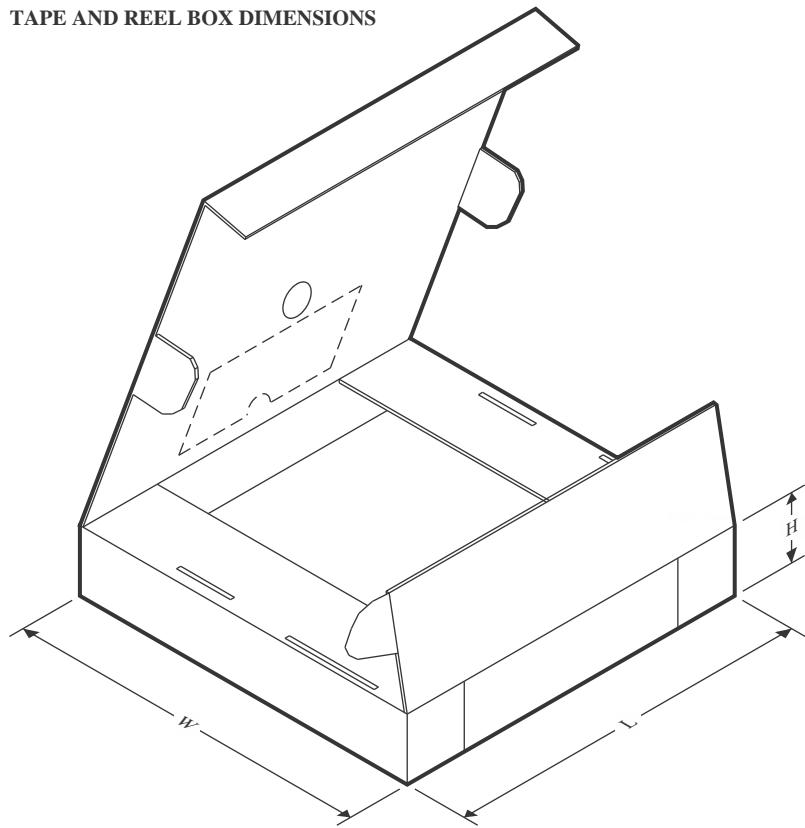


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BAIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2904BAIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2904BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BAIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358BAIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


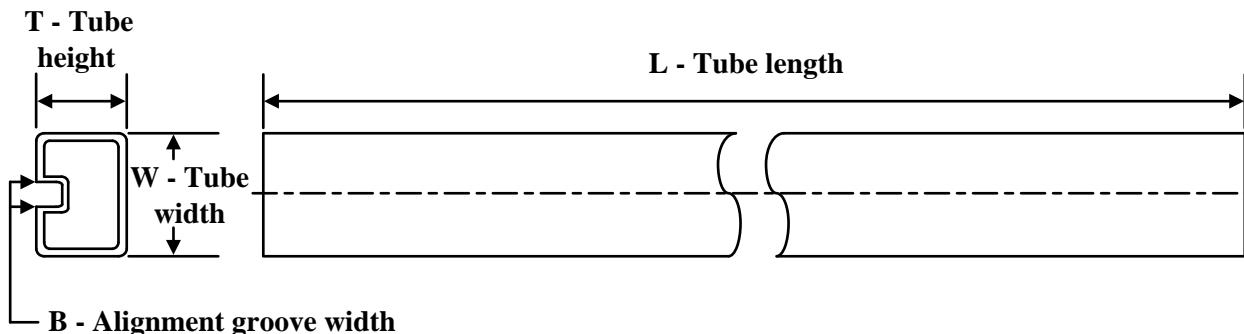
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
LM258ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADR	SOIC	D	8	2500	353.0	353.0	32.0
LM258ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM258ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM258DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM258DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM258DGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LM258DR	SOIC	D	8	2500	356.0	356.0	35.0
LM258DR	SOIC	D	8	2500	356.0	356.0	35.0
LM258DR	SOIC	D	8	2500	340.5	336.1	25.0
LM258DR	SOIC	D	8	2500	353.0	353.0	32.0
LM258DR	SOIC	D	8	2500	353.0	353.0	32.0
LM258DR	SOIC	D	8	2500	340.5	338.1	20.6
LM258DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258DRG4	SOIC	D	8	2500	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM258DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQDRG4	SOIC	D	8	2500	353.0	353.0	32.0
LM2904AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BAIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2904BAIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BAIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904BAIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2904BAIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2904BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904DR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2904PSR	SO	PS	8	2000	356.0	356.0	35.0
LM2904PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM2904PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904QDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904QDR	SOIC	D	8	2500	350.0	350.0	43.0
LM2904VQDR	SOIC	D	8	2500	353.0	353.0	32.0
LM2904VQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM358ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADR	SOIC	D	8	2500	353.0	353.0	32.0
LM358APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358APWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM358BAIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358BAIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM358BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BAIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM358BAIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358BAIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM358BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358BIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM358BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM358BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358DR	SOIC	D	8	2500	353.0	353.0	32.0
LM358DR	SOIC	D	8	2500	340.5	338.1	20.6
LM358PSR	SO	PS	8	2000	356.0	356.0	35.0
LM358PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM358PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-87710012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-87710022A	FK	LCCC	20	55	506.98	12.06	2030	NA
LM158AFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM158FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM258AP	P	PDIP	8	50	506	13.97	11230	4.32
LM258APE4	P	PDIP	8	50	506	13.97	11230	4.32
LM258P	P	PDIP	8	50	506.1	9	600	5.4
LM258P	P	PDIP	8	50	506	13.97	11230	4.32
LM258PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM2904P	P	PDIP	8	50	506	13.97	11230	4.32
LM2904PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM358AP	P	PDIP	8	50	506	13.97	11230	4.32
LM358APE4	P	PDIP	8	50	506	13.97	11230	4.32
LM358P	P	PDIP	8	50	506	13.97	11230	4.32
LM358PE4	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

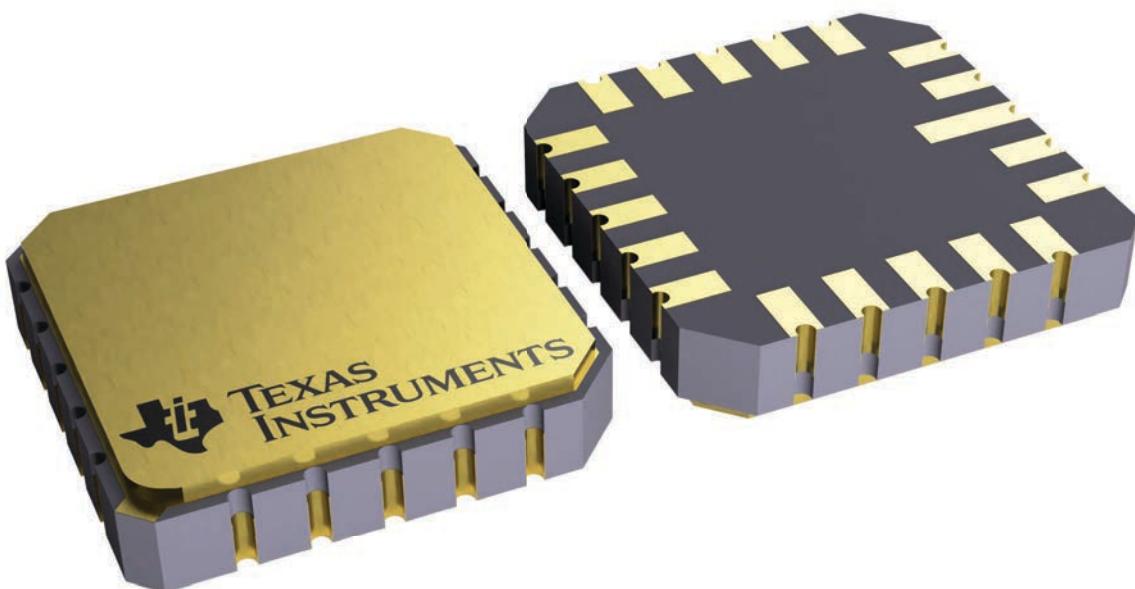
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

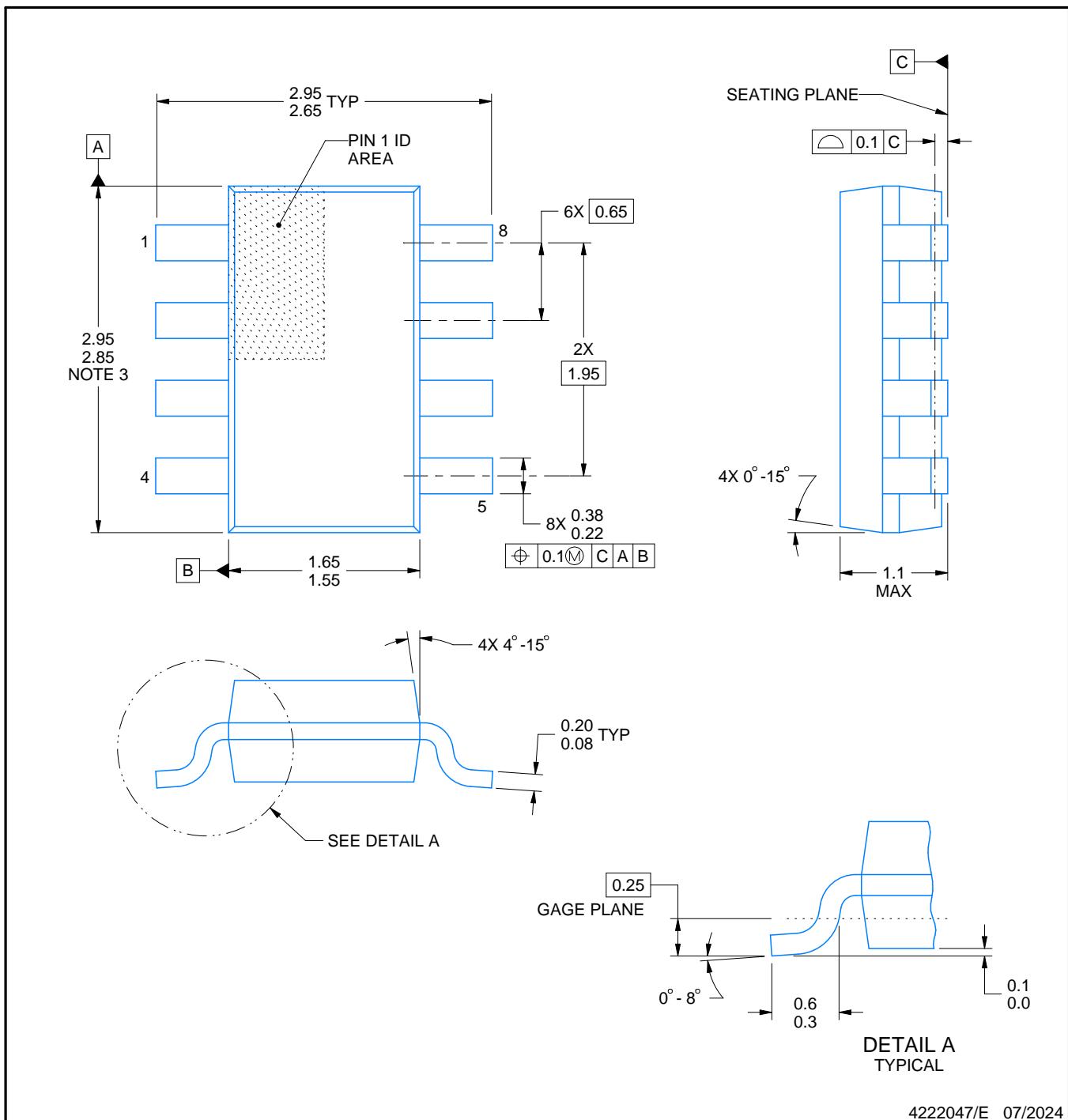
PACKAGE OUTLINE

DDF0008A



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

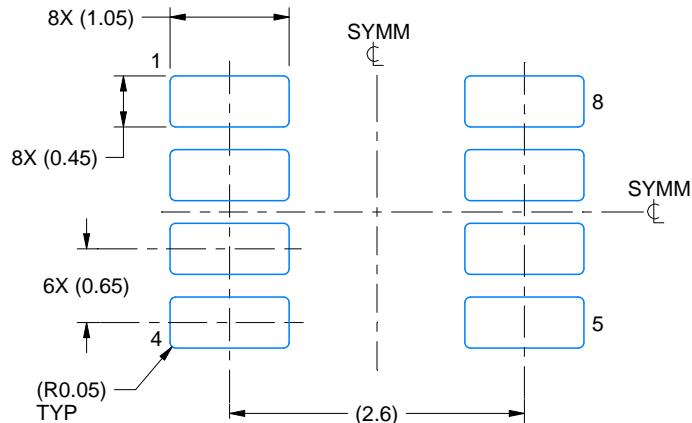
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

DDF0008A

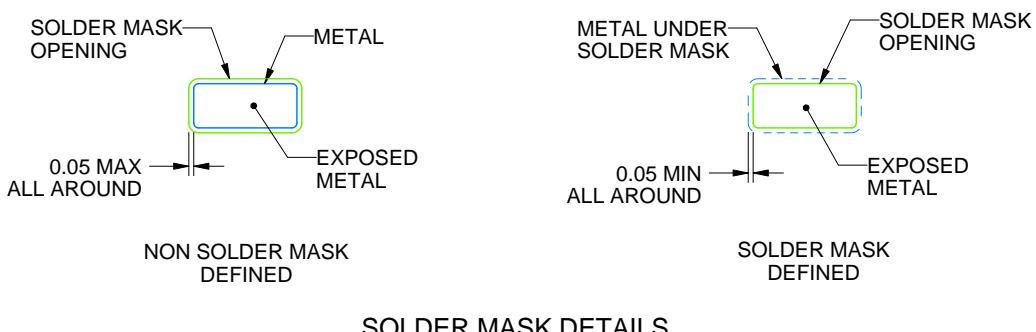
EXAMPLE BOARD LAYOUT

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

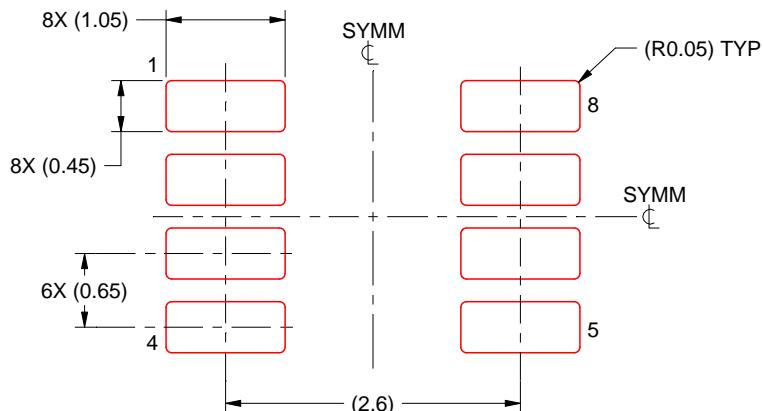
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DDF0008A

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



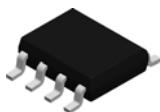
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

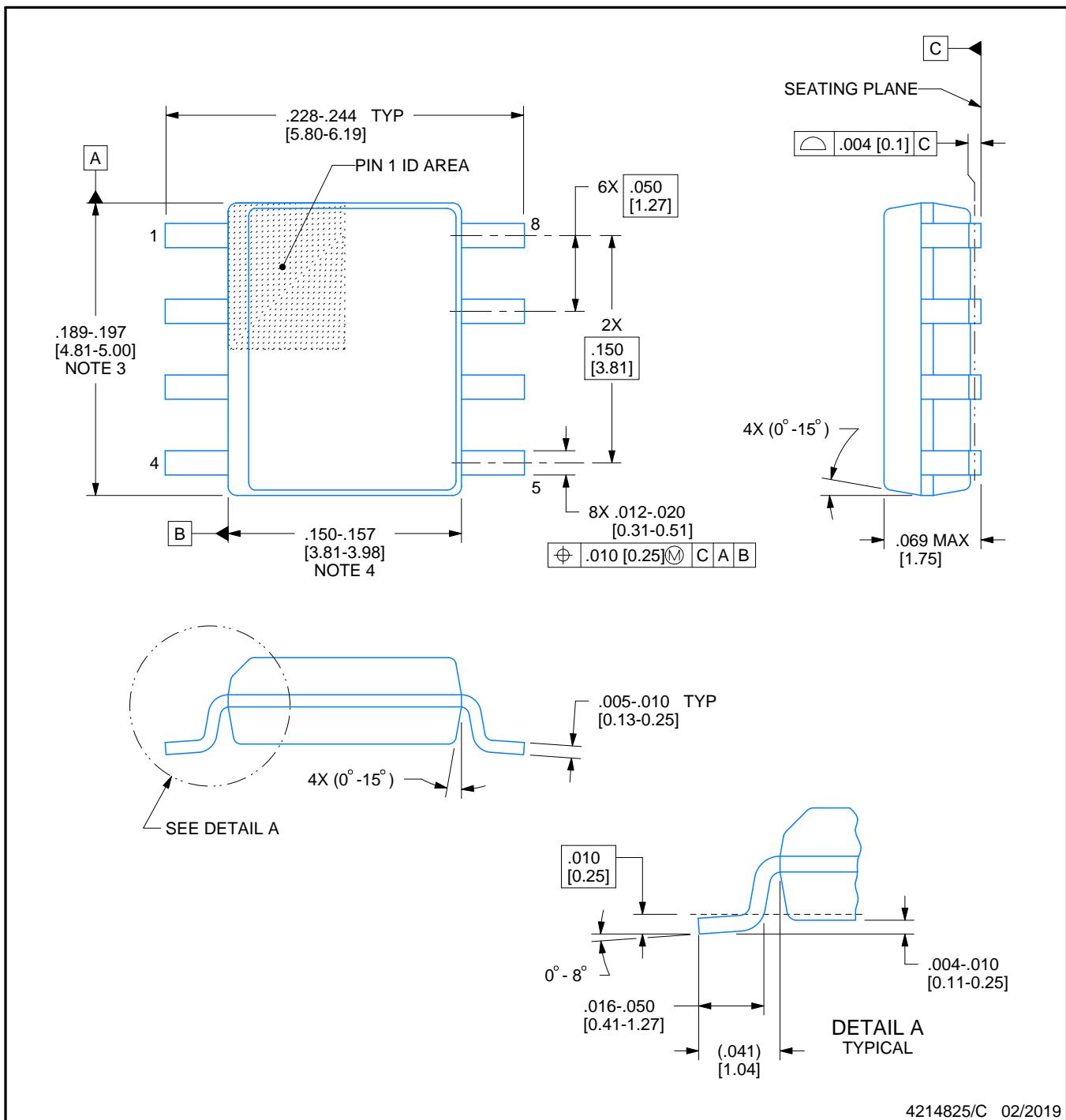
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

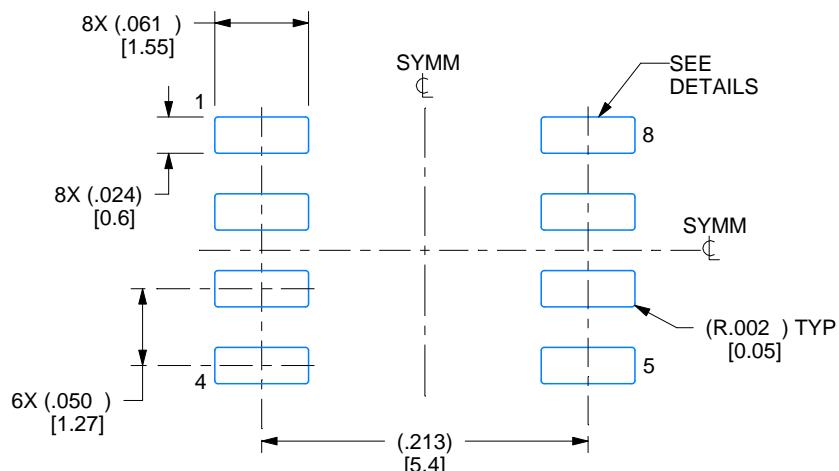
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

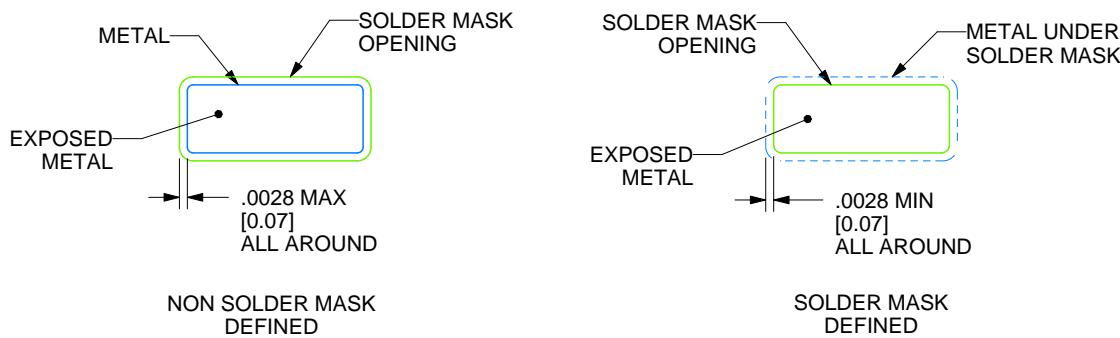
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

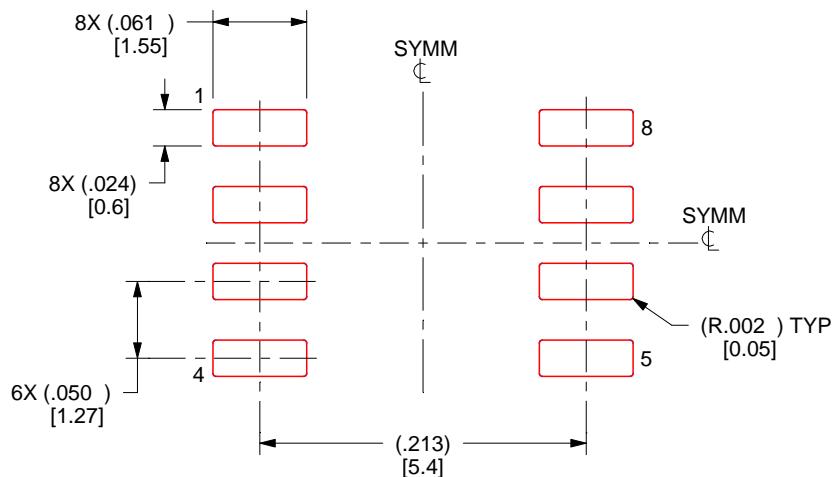
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

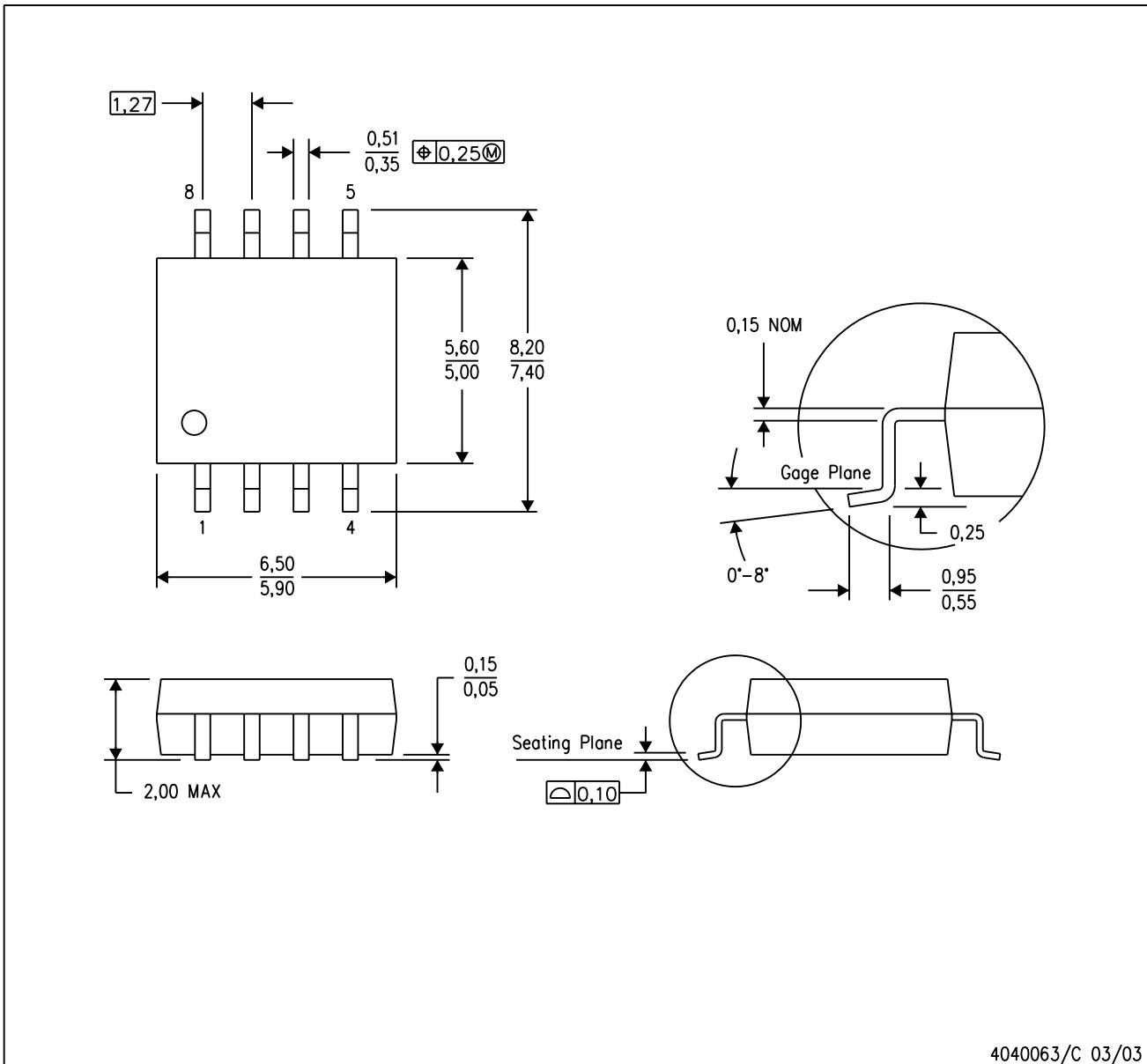
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

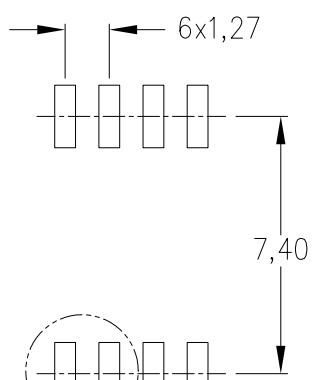
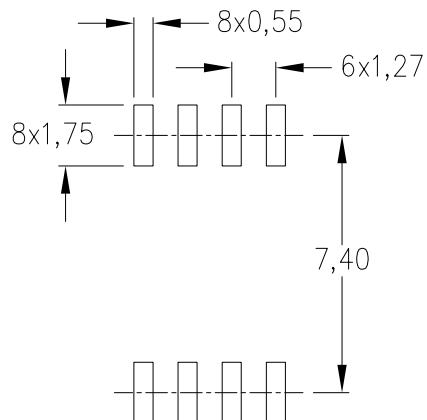
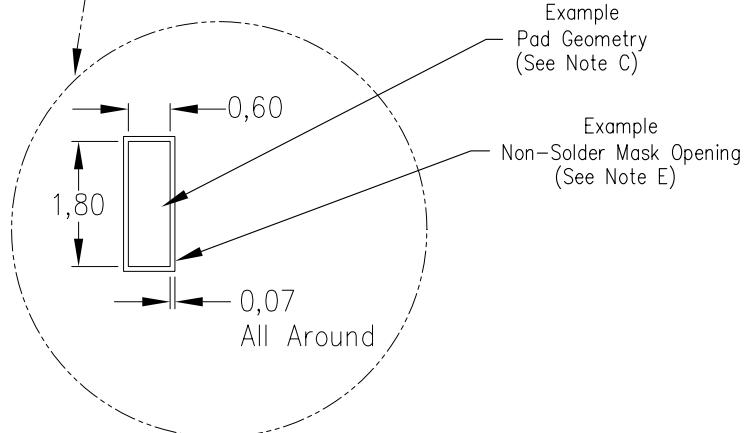


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Non-Solder Mask Opening
(See Note E)

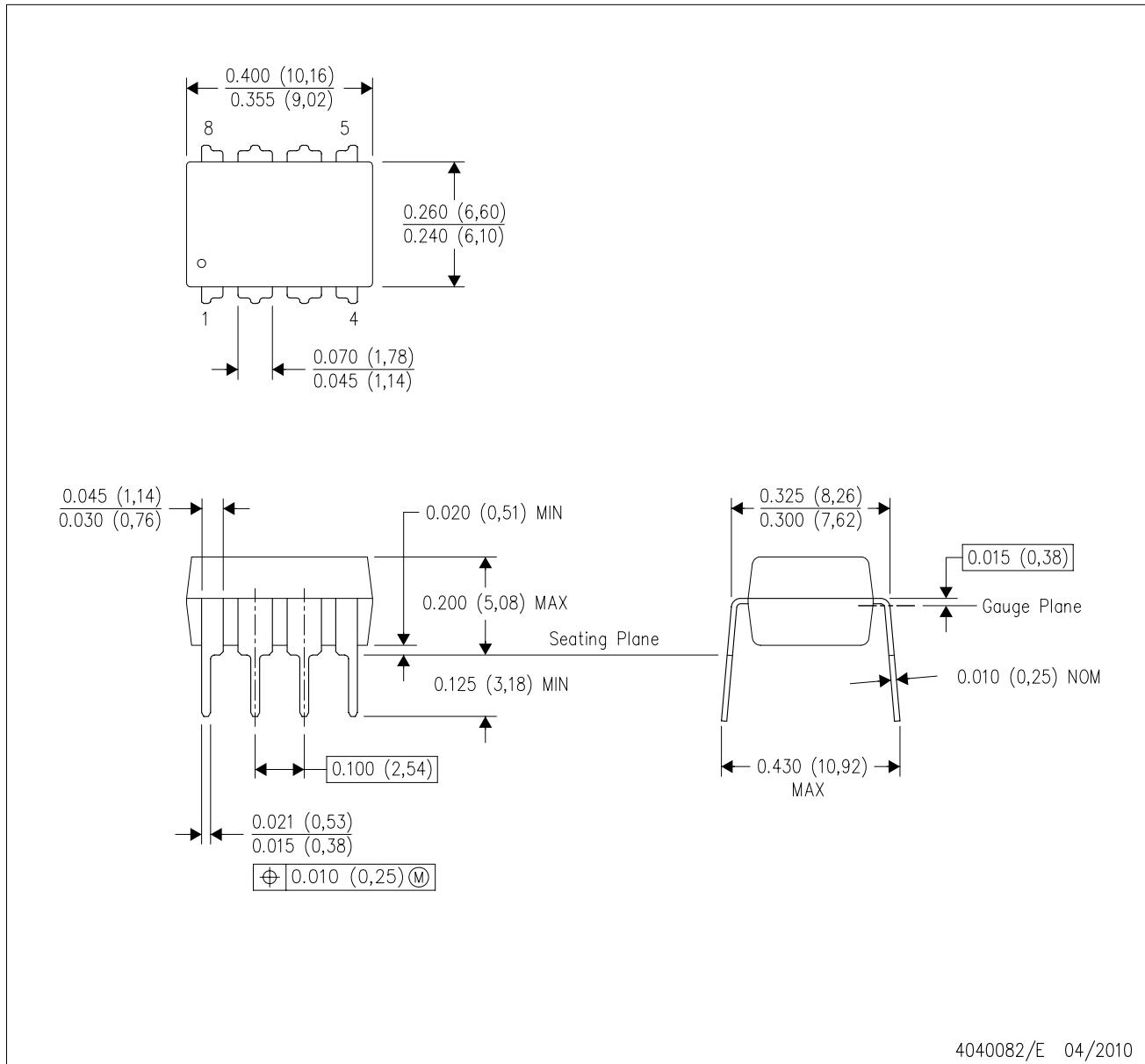
4212188/A 09/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001 variation BA.

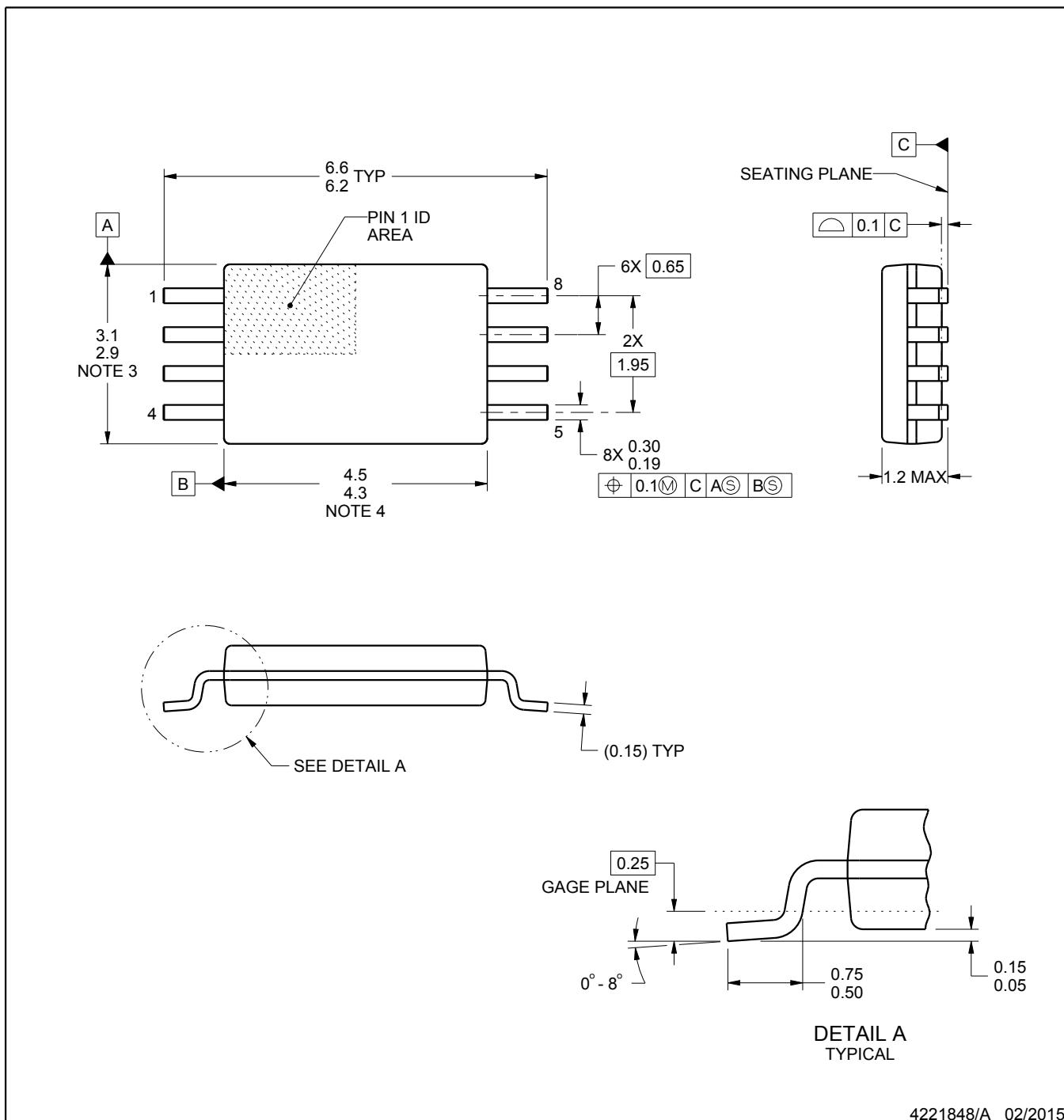
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

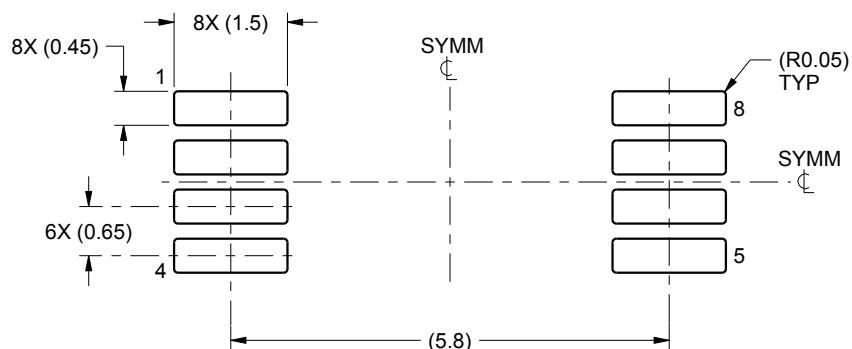
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

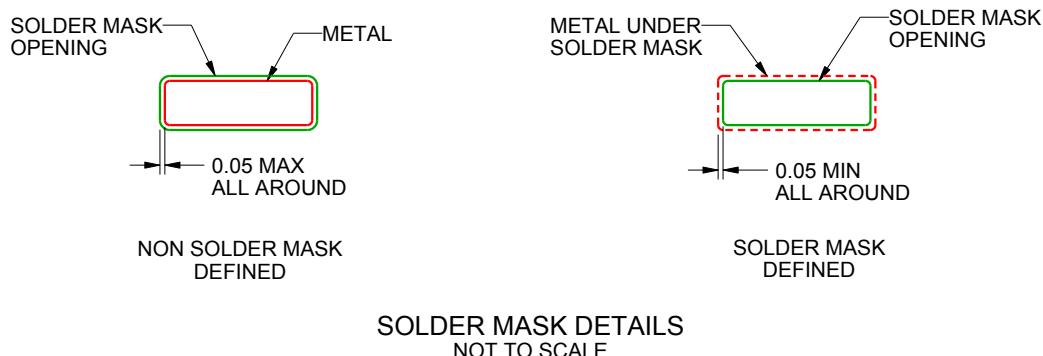
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

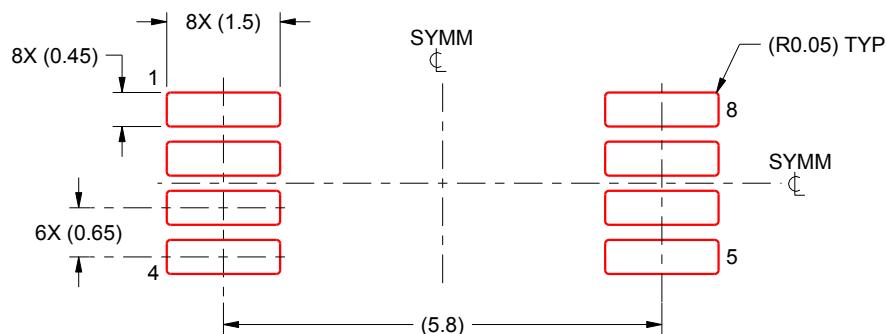
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

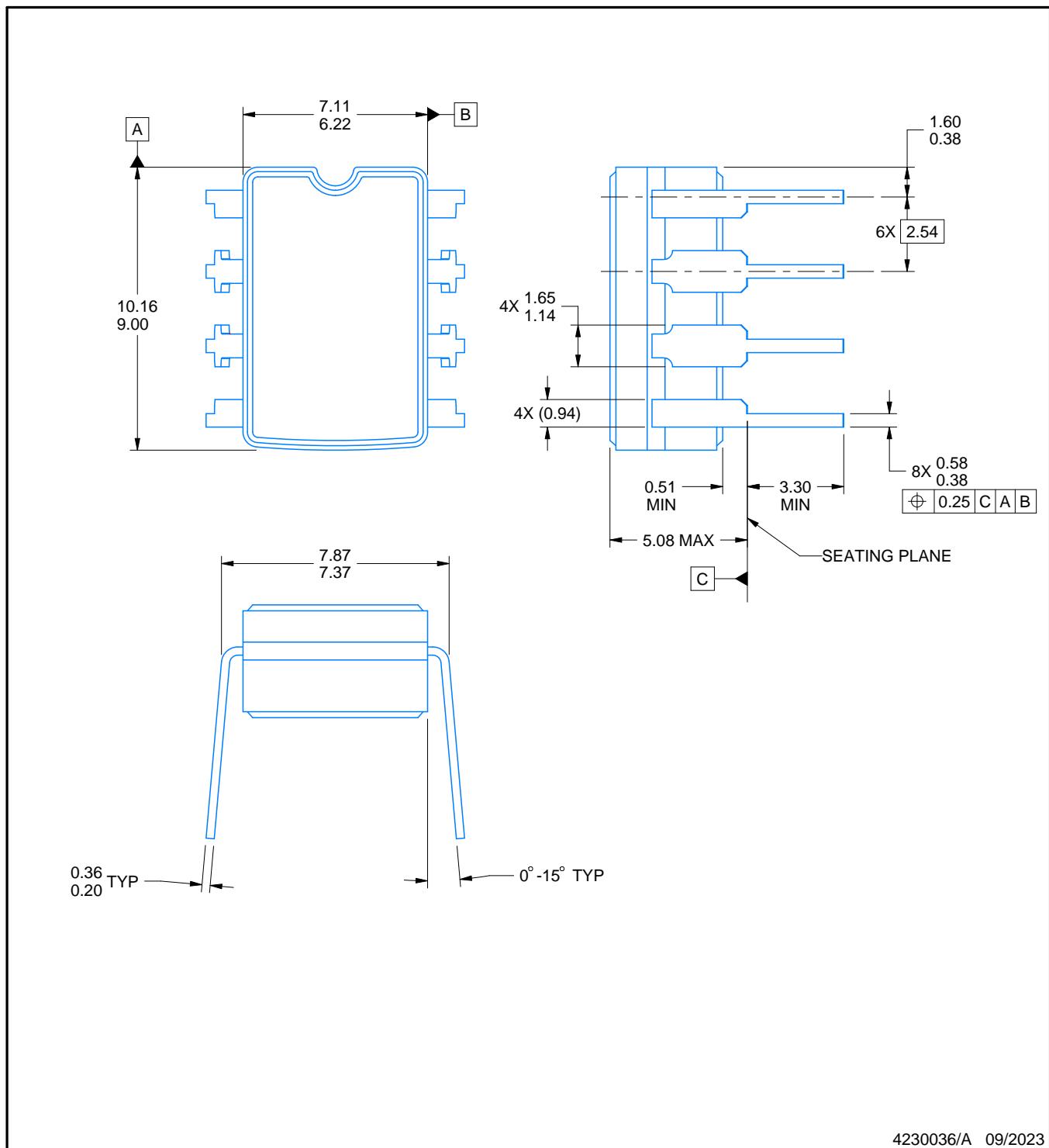
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

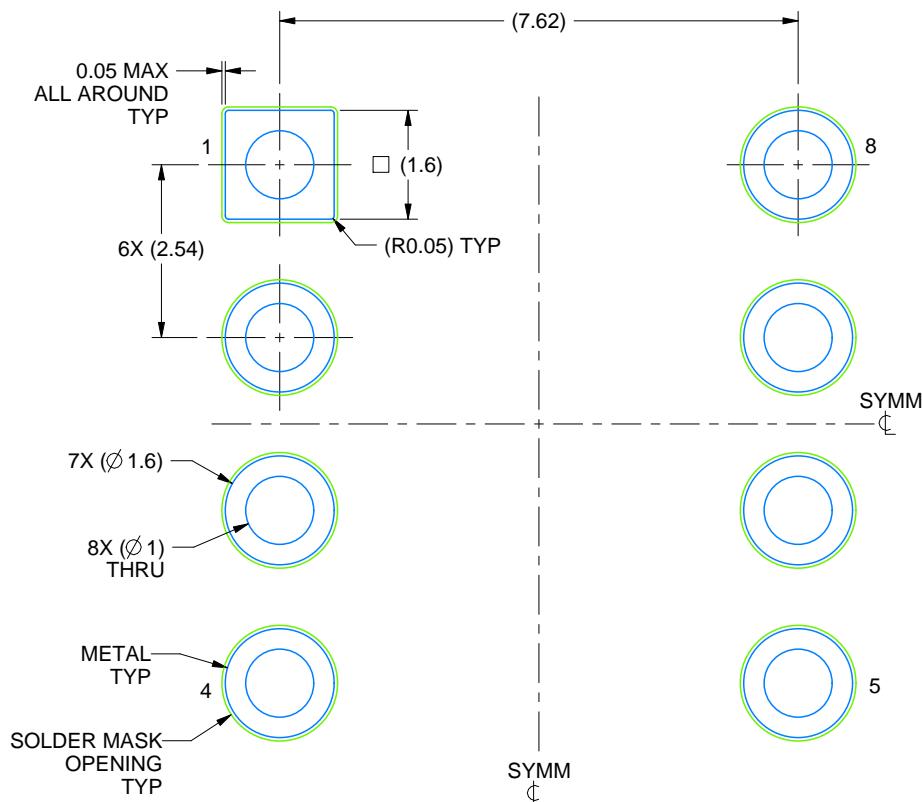
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

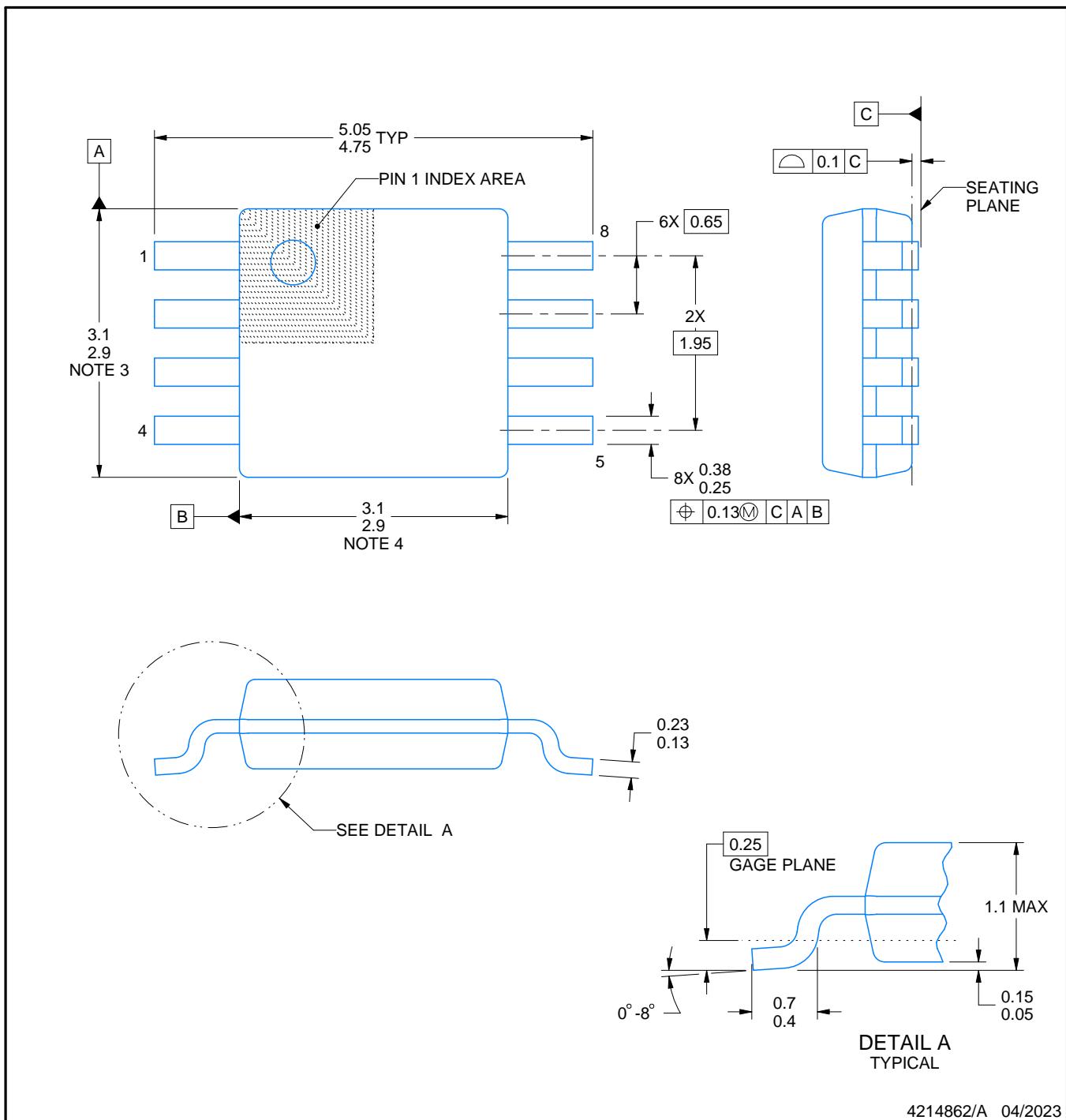
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

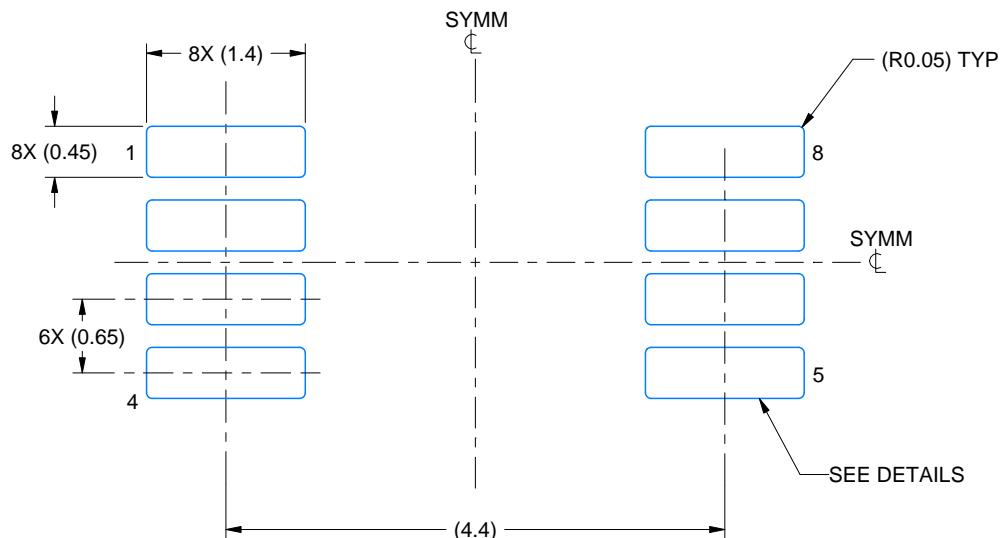
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

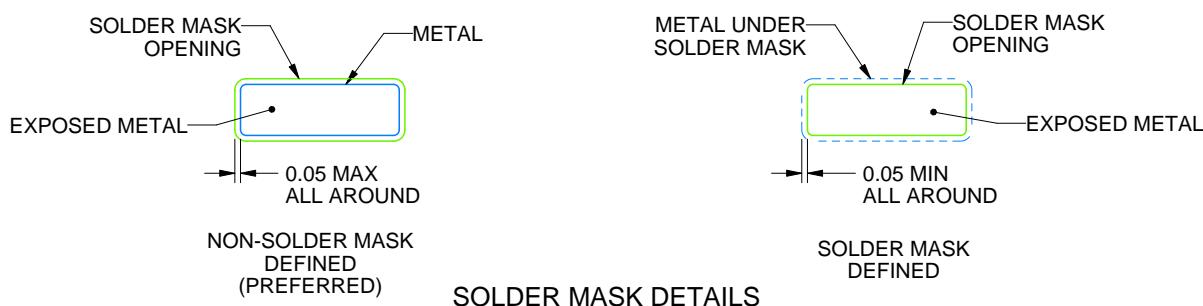
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

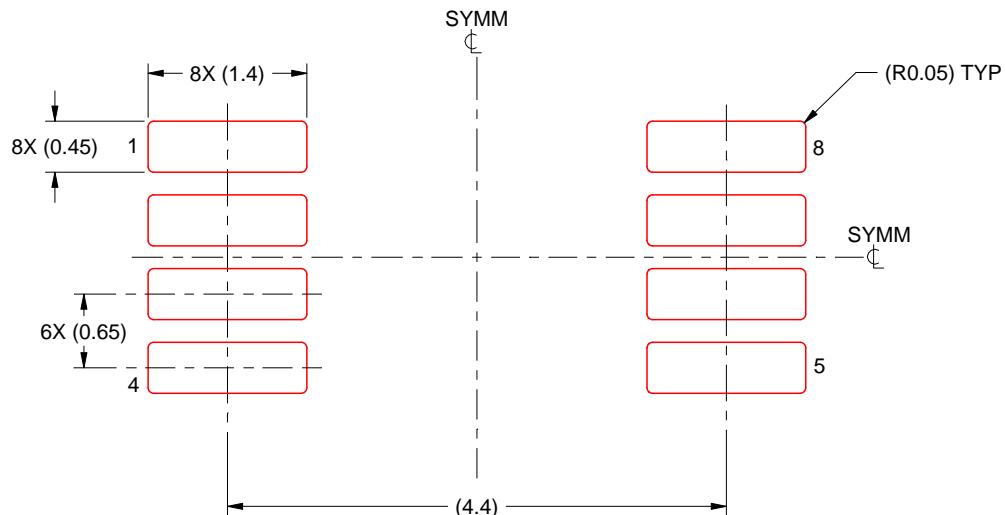
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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