

Design verification report

Design name: MASK_BIU01_fix.gds

OA Number:

Submission date: 23/1/2025

Reviewer: Emmanuel Gooskens

Summary of report: Design violations / errors present - resubmission required

No.	Status description	Current Status
1	Design is accepted for production with no violations	
2	Design is accepted for production with Ligentec-accepted violations.	
3	Design violations / errors present - resubmission required	X
4	Design is accepted for production with waived violations by the customer (see waiver section)	

Following the submission of your design, LIGENTEC is providing you with information regarding design rule violations, design submission violations and other errors present on the submitted design. Attached to this report is the DRC output file please see the end of this report for instructions on how to use this file.

It is important to keep in mind that the design rules are there to ensure your design has the best chance of success. By ensuring your design is free from all violations gives you protection against low yield and increases the reliability of the design. LIGENTEC advises that all violations are corrected, regardless of the severity.

Violations fall into two categories:

- Design rule check (DRC) violations - These are violations found using our DRC script, this will check that the geometric properties of your design follow our design rules, it does not check circuit functionality.
- Design submission check (DSC) violations - These are violations of the rules we have in place to ensure your design is compatible with our process. DSC violations will not appear in the output file attached to this report.

Each violation has a related severity:

- Fatal - This violation must be corrected either because it will cause issues to our process or because the yield will be so low it would not make sense.

- Critical - This violation will cause unpredictable yield and reliability hazards. LIGENTEC will not compensate you for any yield loss and manufacture is entirely at your own risk.
- Warning - Correction is advisable.

DRC violations

Rule	Description	Severity	Comments
1.0 DRC.X1PWidth	X1P width must be $\geq 0.2 \mu\text{m}$.	Critical	Please fix all width violations. # violations: 14
1.0 DRC.X1PFWidth	X1P width must be $\geq 0.180 \mu\text{m}$.	Fatal	Please fix all width violations. # violations: 14
2.0 DRC.X1PSpacing	X1P spacing must be $\geq 0.3 \mu\text{m}$.	Critical	Please fix all spacing violations. # violations: 6521
2.0 DRC.X1PFSpacing	X1P spacing must be $\geq 0.2 \mu\text{m}$.	Fatal	Please fix all spacing violations. # violations: 6480
6.0 DRC.X1PX1PIN Overlap	X1P must overlap X1PIN for proper Black Box connection.	Critical	Bad overlap is usually originated by wrong waveguide connections (different widths or offset) # violations: 7
801	X3PX1PINOverlap	XXXX	# violations: 64
31.0 DRC.P1PWidth	P1P width must be $\geq 0.8 \mu\text{m}$.	Fatal	Please fix all width violations. # violations: 12
315.0 DRC.P1PADSize	P1PAD width must be $\geq 15.0 \mu\text{m}$.	Critical	# violations: 12
316.0 DRC.P1PADWidthInP1R	P1PAD enclosed by P1R by $\geq 2.0 \mu\text{m}$.	Fatal	Please fix all violations. # violations: 12

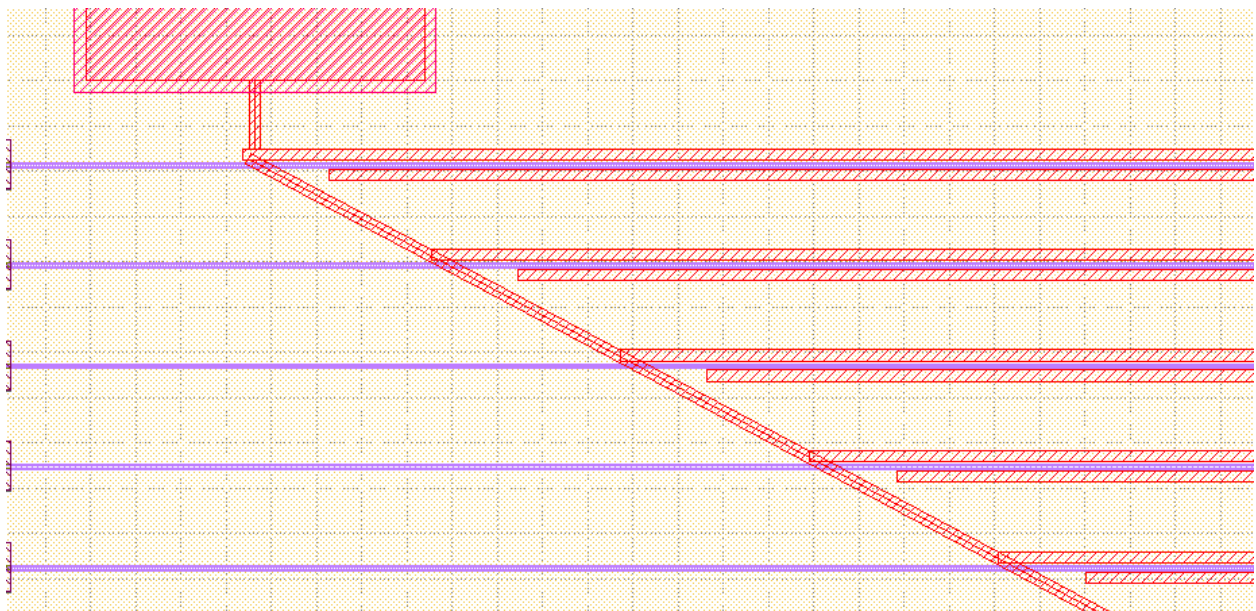
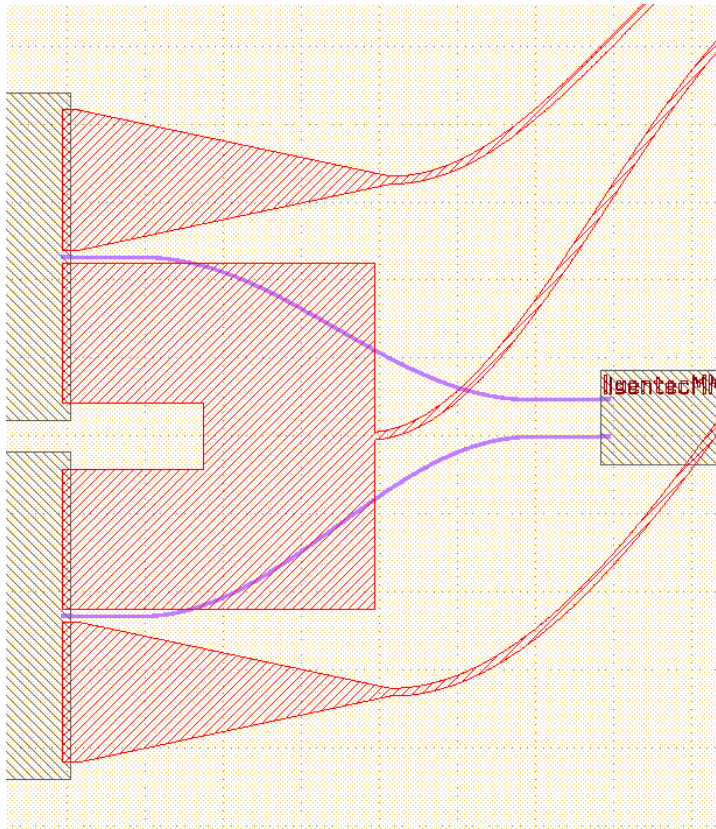
105.0 DRC.CHSEnclosed50e	X1P, X2P, BB, M1P, M1PAD, VIA, P1P, LC1, LC2, LCS, RIBC BB layers must be $\geq 50 \mu\text{m}$ away from CHS edge.	Critical	# violations: 6
107.0 DRC.CHSWithinCSL	CHS has to be enclosed by CSL.	Fatal	# violations: 1
108.0 DRC.CellContained	X1P, X2P, BB, M1P, M1PAD, VIA, P1P, LC1, LC2, LCS, TRN layers must always be inside the CSL layer.	Fatal	# violations: 1
802	CHSLNA15Enclosed50e	XXXX	# violations: 6
1001.0 DRC.BBOverlap	No layer apart from CHS and CSL must overlap with CELLSIZE unless it does too with a BB pin.	Critical	# violations: 1
803	FPINProtrusionLength	XXXX	# violations: 6
804	LNAPLNAPINOverlap	XXXX	# violations: 64
805	LNAM1PWidth	XXXX	# violations: 10
806	LNAM1PFWidth	XXXX	# violations: 10
807	LNAM1PSpacing	XXXX	# violations: 88
808	LNAM1PFSpacing	XXXX	# violations: 58
809	LNAM1PADWithinLNAM1P	XXXX	# violations: 69

DSC violations

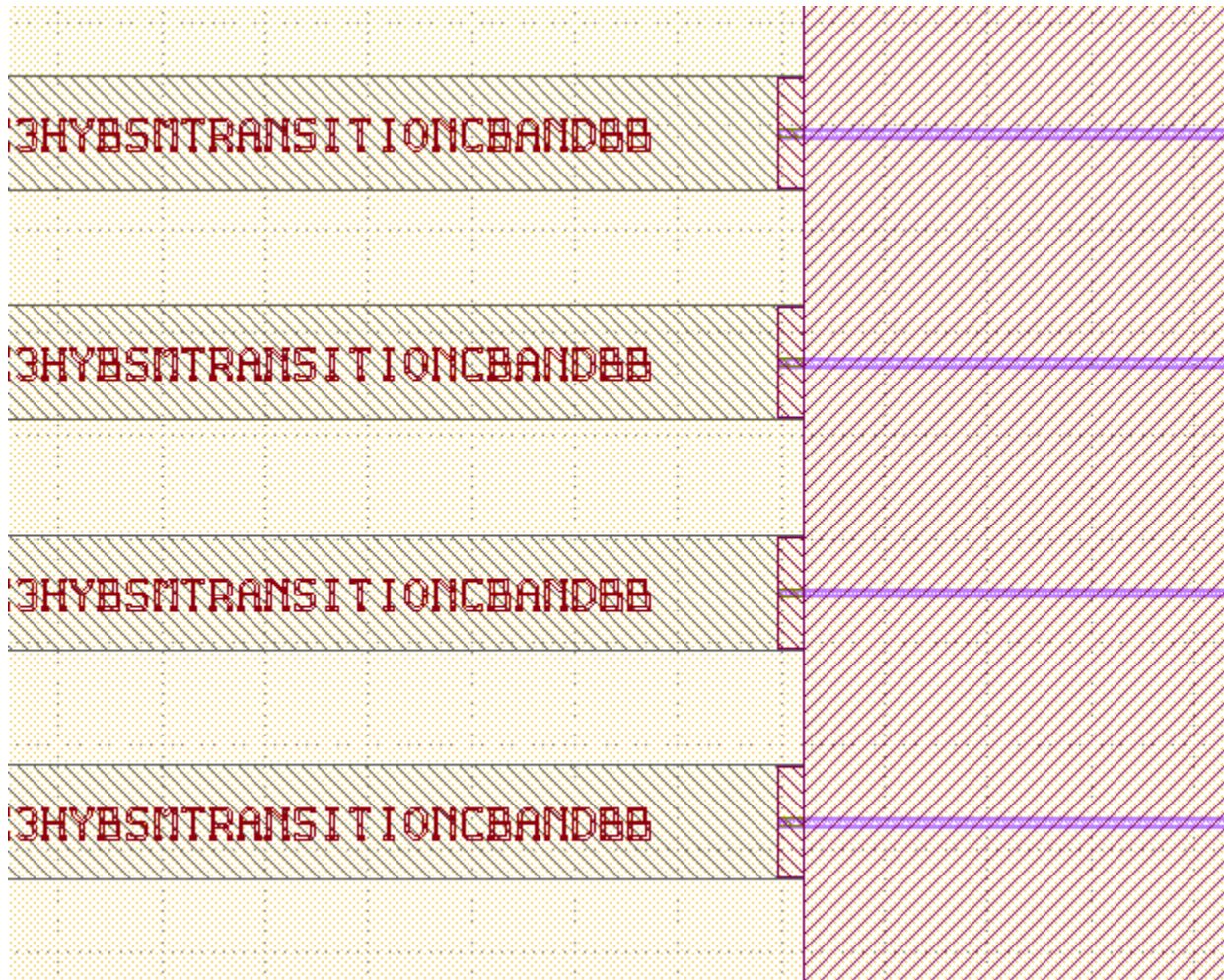
Rule	Description	Severity	Comments
212 DSC.BlackBoxErrorName	Cell name is not in the library.	Fatal	Please check the following cells: ligentecX1X3HybSMTransitionCbandBB\$3 ligentecX1X3HybSMTransitionCbandBB\$2 ligentecMMI2x2BB\$1 ligentecLNA15ModulatorPushPullCbandLongBB\$1
213 DSC.BlackBoxDimensions	Cell center/width/height does not match with BB.	Fatal	Please check the following cells: ligentecLNA15PhaseShifterCbandLongBB bb ((-5,-105;10547,105); lay ((0,0;10552,210)) ligentecLNA15ModulatorPushPullCbandLongBB bb ((-5,-78;10747,78); lay ((0,-78;10752,78)) ligentecInvertedTaper_w1.0 BB bb ((-5,-3;395,3); lay ((0,-3;400,3))
214 DSC.BlackBoxPinLocations	Pins locations do not match with the BB.	Fatal	Please check the following cells: ligentecLNA15PhaseShifterCbandLongBB: Pins in layer X1PIN do not matches ligentecLNA15ModulatorPushPullCbandLongBB: Pins in layer X1PIN do not matches ligentecInvertedTaper_w1.0 BB: Pins in layer X1PIN do

			not matches ligentecInvertedTaper_w1.0 BB: Pins in layer FPIN do not matches
203 DSC.Name of the cell is too long.	Name of the cell cannot contain more than 100 characters.	Passed	
0020 DSC.BBR verification.	The BB replacement did not work as expected.	Fatal	Layer 15/2 remained after BBR.

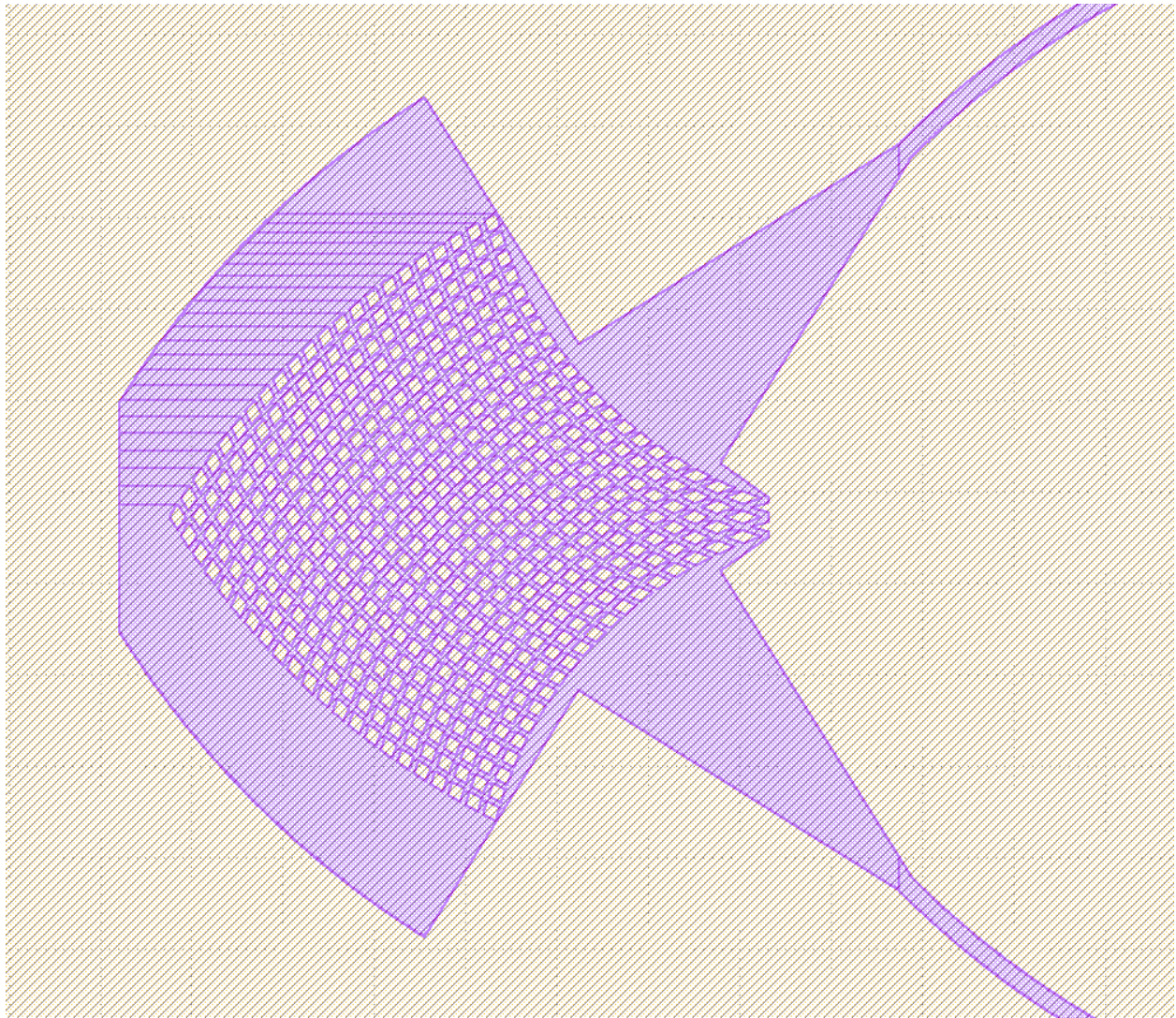
LIGENTEC design comments:



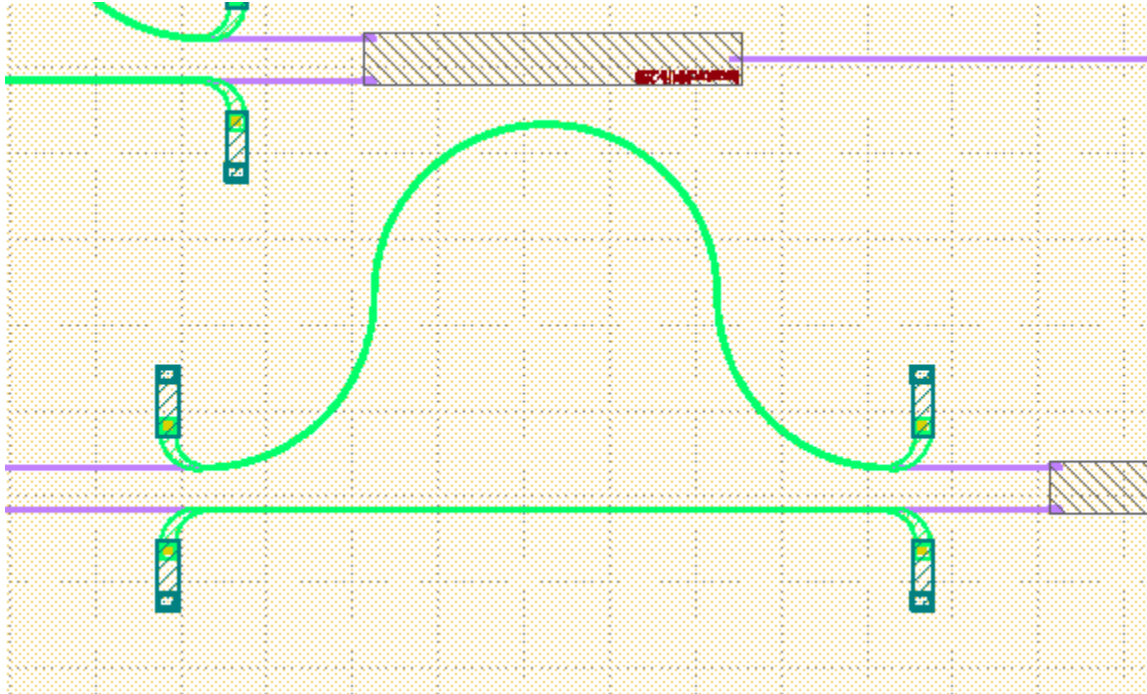
Thin metal lines will cause significant RF loss



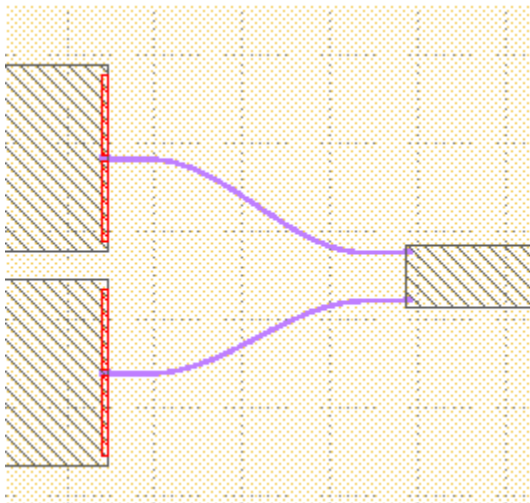
The hybrid mode uses layer 70/0, not 2/0



These structures will not be as well defined as what is drawn, there will be a lithography bias.



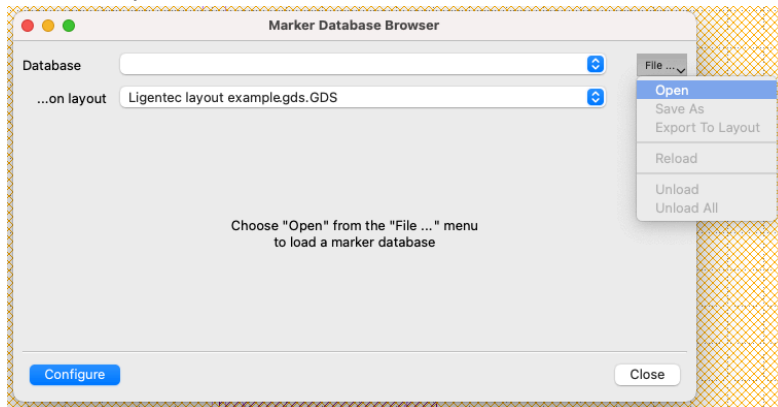
You must use the P1W design layers, as outlined in the LNA design manual



No RF termination. The pad layer is needed to access the metal lines in the modulator BB.

Instruction on viewing the DRC output file

1. Open your original layout file in KLayout
2. Go to Tools>Marker Browser
3. This will open the Marker Database Browser



4. Click on File>Open and select the DRC.results file provided by LIGENTEC
5. The results are then displayed in the Marker Database Browser
6. The violations can be displayed by cell or violation type. By clicking on one of the violations, the layout viewer will highlight that violation.

