Design guidelines for University of Southampton silicon photonics device fabrication 2024

Mask submission deadline – Thursday 7th March 2024

1 File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of 1 nm is used, as per the design template. We recommend dedicated lithography editing software be used in the design of the *.gdsII* file.

2 Process flow

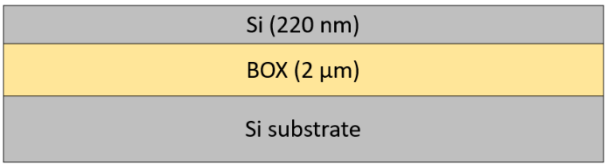
Designs will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 2 µm ± 50 nm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg} = 220 nm ± 20 nm

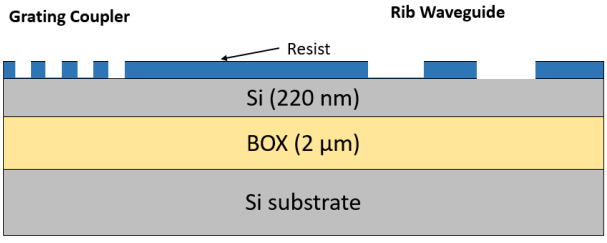
We offer a single silicon etch of 120 nm ± 10 nm. We will deposit a 1 µm ± 100 nm thick silicon dioxide top cladding layer after silicon etching.

The schematic description of the process flow is given below:

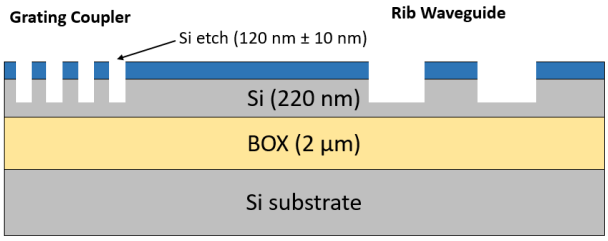
1. Starting SOI substrate



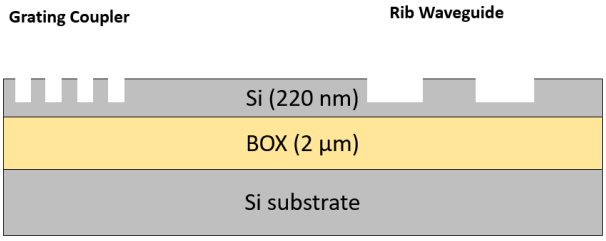
2. Resist patterning for Silicon Etch (GDS layers 3 & 4) – 120 nm ± 10 nm etch



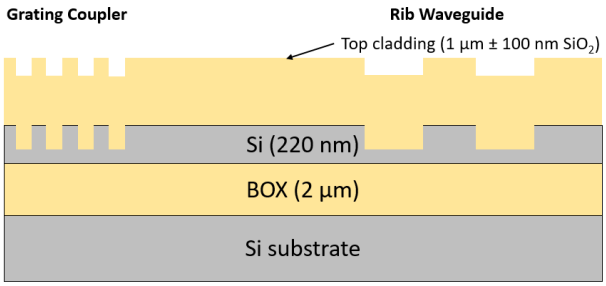
3. Shallow Si etch (120 nm ± 10 nm etch depth)



4. Resist strip



5. Deposition of 1 µm ± 100 nm thick SiO_2 top cladding



3 Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing.

3.1 Design area

The standard user cell has dimensions of **6 x 3 mm²**, as shown in Figure 1.

Figure 1 – User cell design area layout.

3.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm

This layer defines rib waveguides and grating couplers, and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching. During

fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

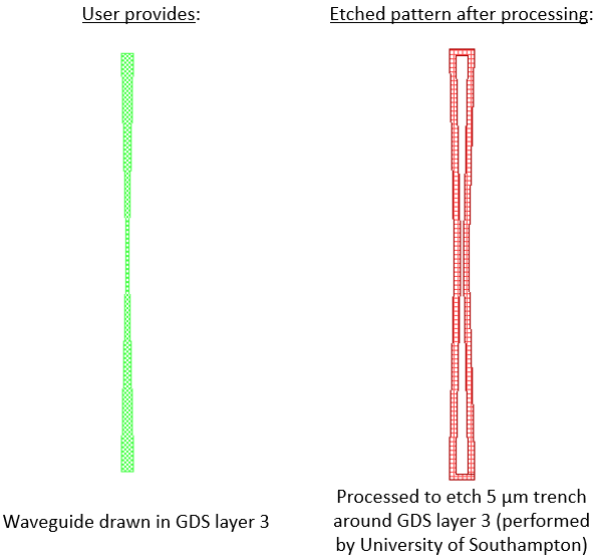


Figure 2 - Description of GDS Layer 3 processing.

GDS Layer 4: Drawn objects on this layer will be exposed to the 120 nm silicon etch. The layer can be used for structures such as labels and grating couplers.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries.

3.3 Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes are detailed in Table 1.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

Table 1 – Design rules summary.

Layer description	GDS number	Field	Minimum feature size	Minimum gap	Max. Feature Width
Silicon Etch (120 nm ± 10 nm)	3	Light	250 nm	200 nm	20 µm
			300 nm	200 nm	N/a
	4	Dark	200 nm	250 nm	20 µm
			200 nm	300 nm	N/a
Cell Outline	99	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a

*Features drawn in the Labels layer will be merged into the Silicon Etch layer by the CORNERSTONE team.

3.4 GDSII template file

A *.gdsII* template file titled 'Design Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

3.5 L-Edit design rule check (DRC)

A Mentor Graphics L-Edit template and design rule check (DRC) file titled 'L-Edit Design Template & DRC' has also been made available. If you have access to Mentor Graphics L-Edit software (license required), you can use this file to check that your designs meet the design rules detailed in Section 3.3. To run the DRC, simply select 'Tools' from the top menu, followed by 'DRC'. Any minimum feature size or minimum gap design rule violations will be flagged, as shown in Figure 3.

It is critical that your submitted mask design does not contain any DRC violations, otherwise it will not be accepted for fabrication and you will have no opportunity to correct it.

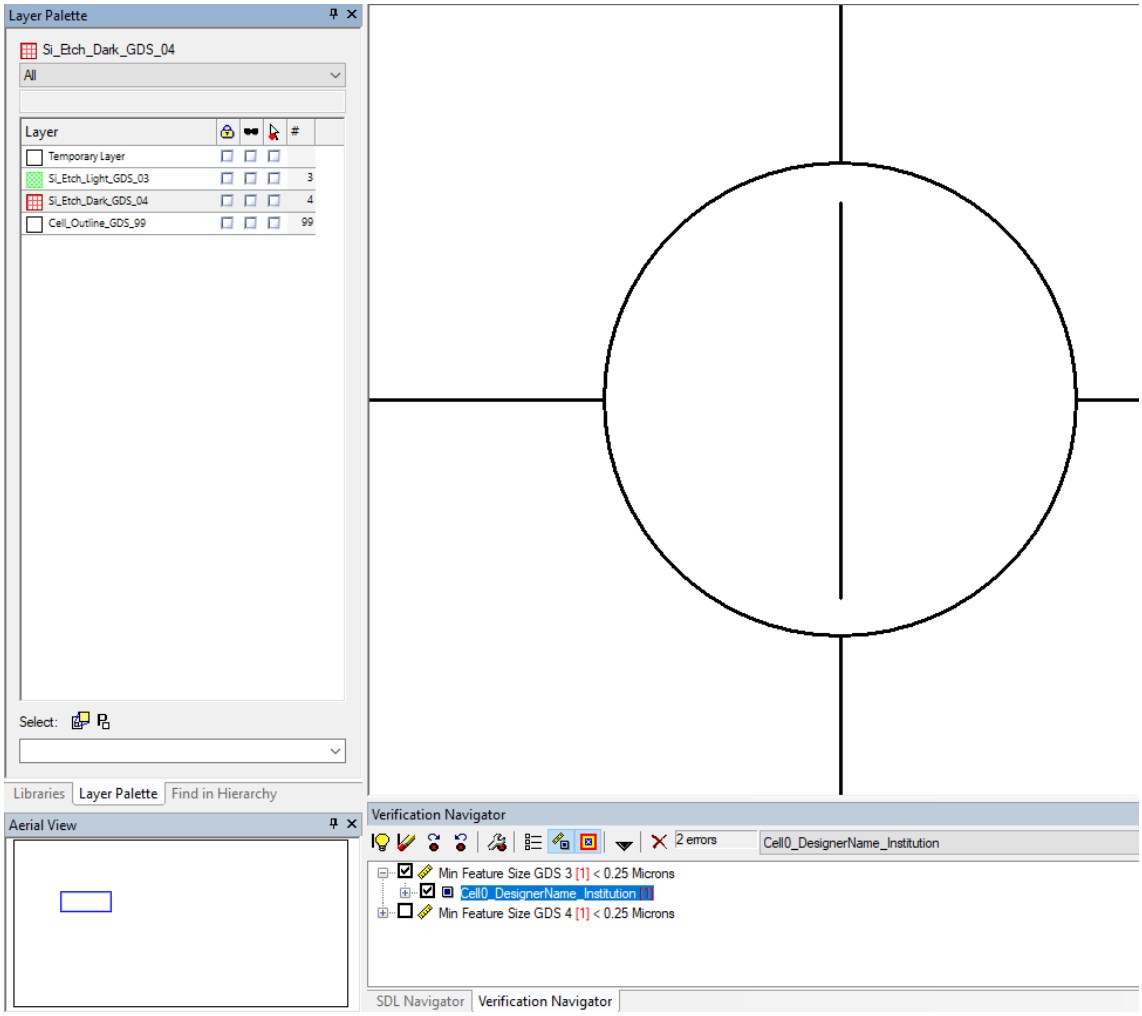


Figure 3 – DRC violation example.

4 Mask submission procedure

Ensure that the top cell in your .gdsII file is titled 'Cell0_*[Name]_[Name of Institution]*'.

Submit your mask design on or before the submission deadline at the top of this document to your supervisor / module coordinator.

Under no circumstances will late submissions be accepted.

5 Mask processing performed by University of Southampton

Upon receipt of your *.gdsII* file, the University of Southampton team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 3.2:

Silicon Etch – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm

1. Grow GDS layer 3 by 5 µm in all directions.
2. Subtract GDS layer 3 from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Combine the output of (2) with GDS layer 4 and GDS layer 100.

6 Technical support

If you have any questions relating to the fabrication process or design rules, please contact your supervisor / module coordinator.