

LAN8742A-breakout-board Fabrication Document

Layer Stack Legend

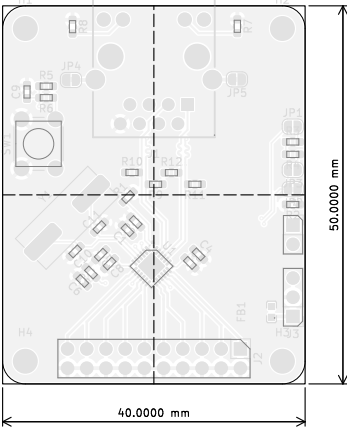
	Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste				Paste Mask	
	F.Silkscreen			Direct Printing	Legend	GBR
	F.Mask		0.02mm	Solder Resist	Solder Mask	GBR
	Copper	L1 (Sig, PWR)	0.035mm (1.00oz)		Signal	GBR
	Prepreg		0.2104mm	FR4_7628	Dielectric	
	Copper	L2 (GND)	0.0152mm (0.43oz)		Plane	GBR
	Core		1.065mm	FR4	Dielectric	
	Copper	L3 (Sig, PWR)	0.0152mm (0.43oz)		Signal	GBR
	Prepreg		0.2104mm	FR4_7628	Dielectric	
	Copper	L6 (Sig, PWR)	0.035mm (1.00oz)		Signal	GBR
	B.Mask		0.02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen			Direct Printing	Legend	GBR
	B.Paste				Paste Mask	

Total thickness: 1.6262mm  
Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0.2032	0.28	L2

Top Fabrication (Scale 1:1)



FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.  
  
DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.  
  
SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 4) SURFACE FINISH: IMMERSION GOLD
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR BLACK.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING YELLOW NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:

A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
B. Tg 170 C OR EQUIVALENT.  
C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY PATAPIMLABS.
- 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE40,000 × 50,000 mm  
BOARD THICKNESS1.626 mm  
TRACE WIDTH0.200 mm  
TRACE TO TRACE0.200 mm  
MIN. HOLE (PTH)0.200 mm  
MIN. HOLE (NPTH)3.200 mm  
ANNULAR RING0.150 mm  
COPPER TO HOLE0.254 mm  
COPPER TO EDGE0.250 mm  
HOLE TO HOLE0.254 mm
- 11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.
- 12) CONFIRM SPACE WIDTHS AND SPACINGS.

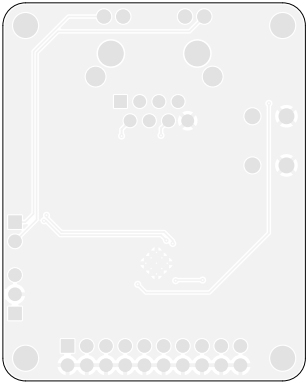
All dimensions are in millimeters unless otherwise specified.

	Comments:	Company: PatapimLabs	Variant: PRELIMINARY	Git Hash: f5059cd
	Sheet Title: Top Fabrication (Scale 1:1)	Board Name: LAN8742A-breakout-board	Project Name: LAN8742A Breakout	
	Sheet Path:	File Name: LAN8742A-breakout.kicad_pcb	Designer: Tropikej	Date: 2024-04-13
			Reviewer:	Revision: + (Unreleased)
			Size: A4	Sheet: 1 of 10

# LAN8742A-breakout-board Fabrication Document

3 × 120°

## Bottom Fabrication (Scale 1:1)



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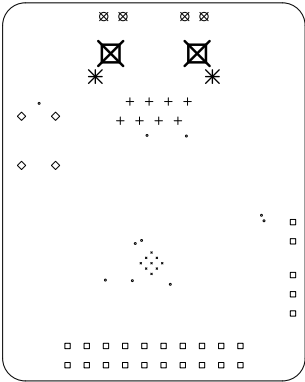
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	Sheet Path:		Reviewer:	Size: A4	Sheet: 2 of 10

LAN8742A-breakout-board Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	9	0.20mm (7.87mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
○	10	0.25mm (9.84mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Via
+	8	1.00mm (39.37mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
□	25	1.00mm (39.37mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
◇	4	1.10mm (43.31mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
⊗	4	1.10mm (43.31mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
※	2	1.80mm (70.87mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
⊠	2	3.30mm (129.92mils)	PTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Pad
Total 64						

Drill Drawing L1 - L4 (Scale 1:1)



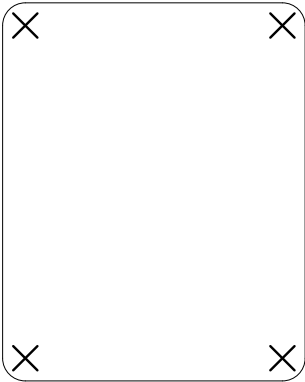
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	Sheet Path:	Reviewer:	Size: A4	Revision: + (Unreleased)
			Sheet: 3 of 10	

# LAN8742A-breakout-board Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
X	4	3.20mm (125,98mils)	NPPTH	Round	L1 (Sig. PWR) - L6 (Sig. PWR)	Mechanical
	Total 4					

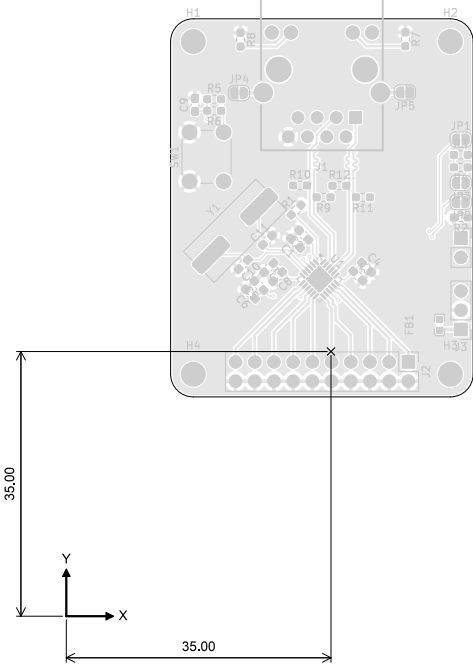
Drill Drawing L1 - L4 (Scale 1:1)



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	Sheet Title: Drill Drawing (L1 - L4)	File Name: LAN8742A-breakout.kicad_pcb	Designer: Tropikej	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 4 of 10

LAN8742A-breakout-board Fabrication Document

Top Test Points (Scale 1:1)



Ref.	Net	X [mm]	Y [mm]
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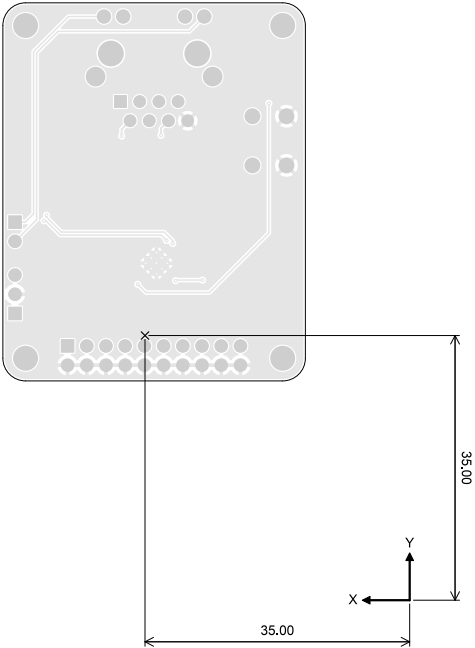
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# LAN8742A-breakout-board Fabrication Document

Bottom Test Points (Scale 1:1)



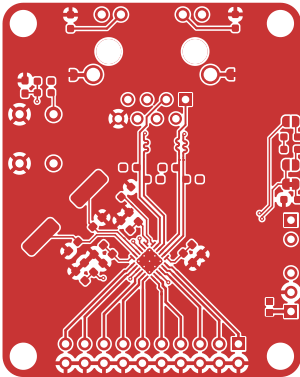
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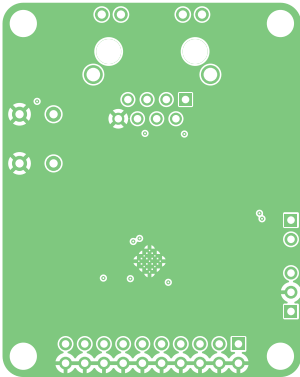
L1 (Sig, PWR) (Scale 1:1)



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	Sheet Title: L1 (Sig, PWR) (Scale 1:1)	File Name: LAN8742A-breakout.kicad_pcb	Designer: Tropikej	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer:	Size: A4	Sheet: 7 of 10

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L2 (GND) (Scale 1:1)

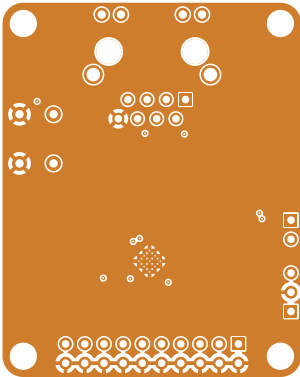


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	Sheet Title: L2 (GND) (Scale 1:1)	File Name: LAN8742A-breakout.kicad_pcb	Designer: Tropikej	Date: 2024-04-13	Revision: + (Unreleased)
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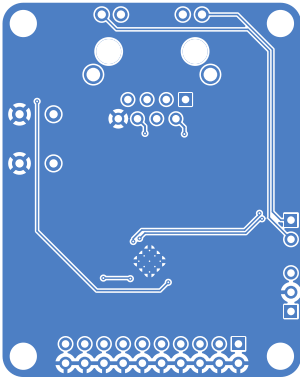
L3 (Sig, PWR) (Scale 1:1)



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	Sheet Title: L3 (Sig, PWR) (Scale 1:1)	File Name: LAN8742A-breakout.kicad_pcb	Designer: Tropikej	Date: 2024-04-13	Revision: + (Unreleased)
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L6 (Sig, PWR) (Scale 1:1)



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