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CS110: Computer Architecture
Spring, 2024

Assignment 4: Digital circuit

Attention: Recommend using LaTeXto complete your work. You can use any tool, such as Logisim, Visio, Draw.io, PowerPoint, etc., to create diagrams. However, handwritten or hand-drawn content is not acceptable.

1 Combinational logic

Analyze the circuit shown in Fig. 1 and answer the following questions:

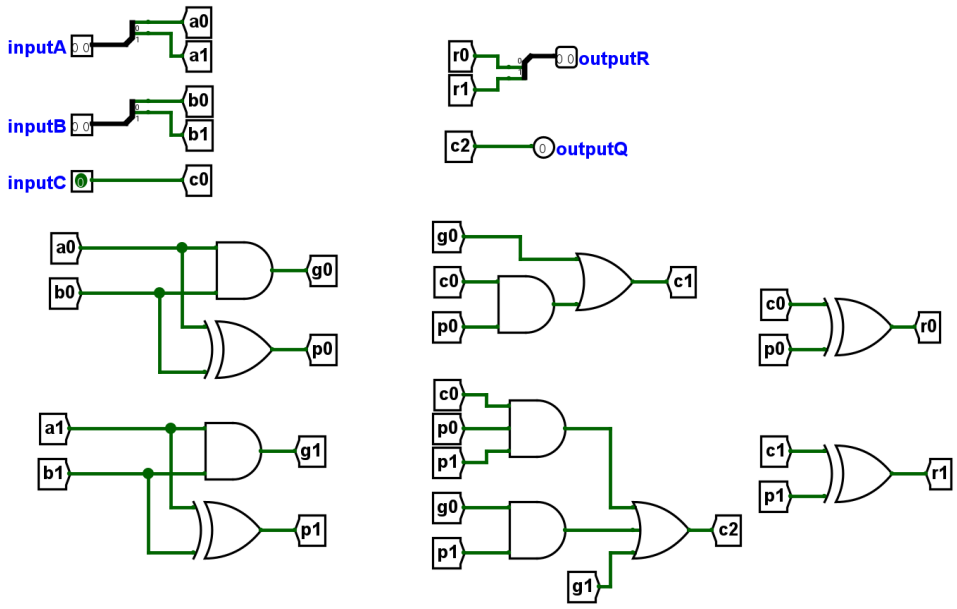


Figure 1: A 2-bit arithmetic circuit

(a) Draw the truth table of this circuit.**[10 pt]**

(b) Which kind of arithmetic operation (addition, subtraction, multiplication, division, shift, or comparison) is performed by this circuit? What are the advantages and disadvantages of the circuit in Fig. 1 compared to the corresponding arithmetic circuit mentioned in Digital circuits I?**[10 pt]**

(c) Assume that all 2-input logic gates have 1 ns delay, all 3-input logic gates have 2 ns delay, and other delays are not considered. Calculate the max delay of this circuit.**[10 pt]**

Answer to Question 1

(a)

A_0	A_1	B_0	B_1	c_0	g_0	g_1	p_0	p_1	c_1	c_2	r_0	r_1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1	0	0	0	1	0
0	0	1	0	1	0	0	1	0	1	0	0	1
0	0	1	1	0	0	0	1	1	0	0	1	1
0	0	1	1	1	0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0	1	0	0	0	1
0	1	0	0	1	0	0	0	1	0	0	1	1
0	1	0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	0	0	0	1	1	0
0	1	1	0	0	0	0	1	1	0	0	1	1
0	1	1	0	1	0	0	1	1	1	1	0	0
0	1	1	1	0	0	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1	0	1	1	0	1
1	0	0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	1	0	0	1	0	1	0	0	1
1	0	0	1	0	0	0	1	1	0	0	1	1
1	0	0	1	1	0	0	1	1	1	1	0	0
1	0	1	0	0	1	0	0	0	1	0	0	1
1	0	1	0	1	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	1	1	1	0	0
1	0	1	1	1	1	0	0	1	1	1	1	0
1	1	0	0	0	0	0	1	1	0	0	1	1
1	1	0	0	1	0	0	1	1	1	1	0	0
1	1	0	1	0	0	1	1	0	0	1	1	0
1	1	0	1	1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	0	0	1	1	1	0	0
1	1	1	0	1	1	0	0	1	1	1	1	0
1	1	1	1	0	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0	0	1	1	1	1

(b) it is a addition operation.

Advantages: Shorter delay, capable of parallel computation across multiple bits;

Disadvantages: Requires more logic gates.

(c)

the longest circuit path is c2→3-or→3-and→p0/p1→2-xor

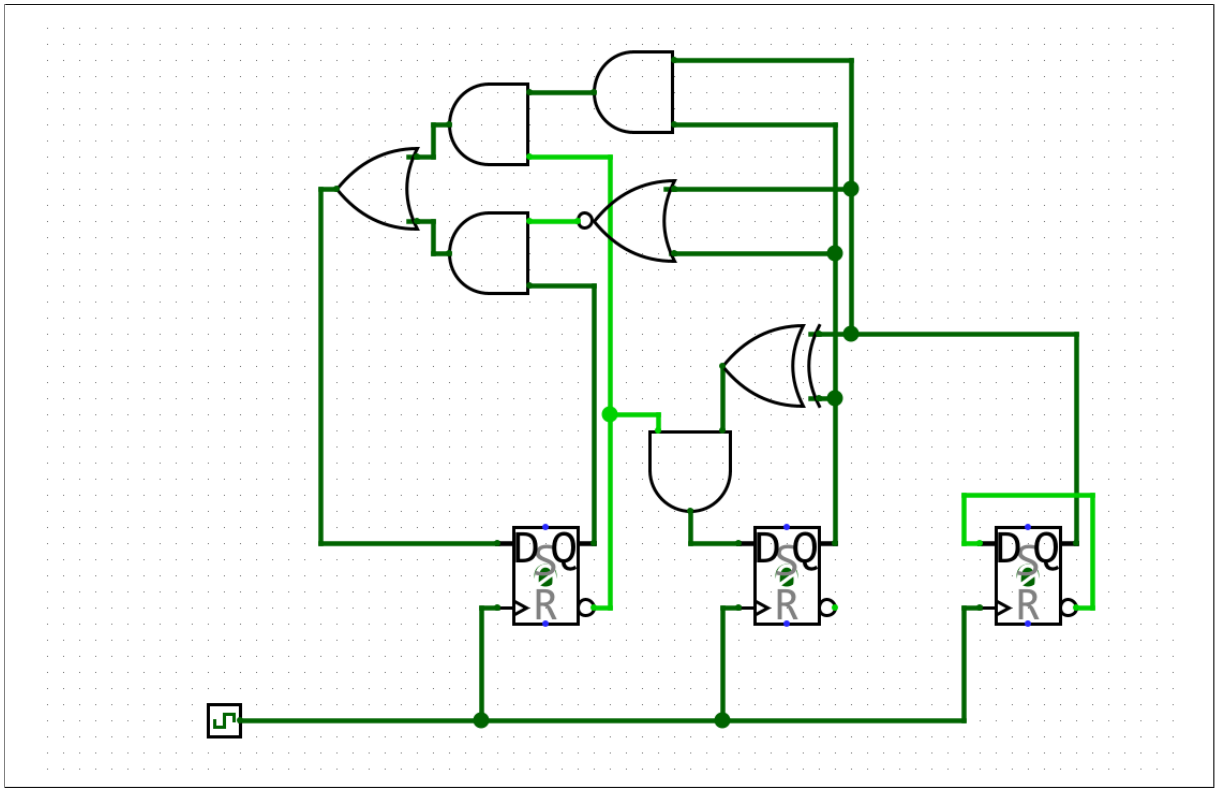
then the max delay is $2 \times 2 + 1 \times 1 = 5$

2 SDS

Draw a counter that counts from 0 to 5 using three D flip-flops (each flip-flops represents one output bit) and some 2-input logic gates (AND, OR, NOT). Please use the method taught in class to build a Moore FSM that implements the circular counter. Complete the state transition logic and output logic. **[35 pt]**

Figure 2: The counter cycles through the process of counting from 0 to 5.

Answer to Question 2



3 Finite state machine

The function of a vending machine which sells bottles of soda is described below:

- Each bottle costs $1.50.
- The machine only accepts $0.50 and $1 coins. If a customer inserts enough coins, the machine will dispense a bottle of soda (FSM will output "1", otherwise "0") and returns change if needed , e.g., the output of DISPENSE states may be "1 $0.5", other states' output may be "0 $0".
- The process happens one coin at a time, and there is no simultaneous insertion of multiple coins or shipping of multiple bottles. After each transaction, the vending machine enters the IDLE state.
- We don't need to account for a scenario where a customer inserts coins but decides not to make a purchase.

(a) Draw the FSM (Moore machine) for this vending machine.**[15 pt]**

(b) Draw the FSM (Mealy machine) for this vending machine.**[10 pt]**

(c) Could Moore machines and Mealy machines be converted into each other to implement the same function? Compare their difference.**[10 pt]**

Answer to Question 3

Your answer here.