

# UNIT-3: AMPLIFIERS & Oscillators

## Amplifiers.

- An amplifier is used to increase the amplitude of a signal waveform, without changing other parameters of the waveform such as frequency or wave shape.
- In other words, an amplifier is an electronic device that increases the voltage, current or power of a signal.

## Types of Amplifiers.

- Many different types of amplifier are found in electronic circuits. They are:

### 1) a.c coupled amplifiers :

An amplifier circuit that uses AC coupling in order to block DC current and allows only ac components of a signal are transferred from one stage to another.

### 2) d.c coupled amplifiers :

In d.c (direct) coupled amplifiers, stages are coupled together in such a way that stages are not isolated to dc potentials. Both ac and dc signal components are transferred from stage to stage.

### 3) Large-signal amplifiers :

Large signal amplifiers also known as Power Amplifiers are capable of providing large amount of power to the load. Typically from 1V to 100V or more.

### 4) Small-signal Amplifiers :

Small signal amplifiers also known as Voltage Amplifiers are capable of handling small input ac signals. Typically a few μV or a few mV.

## 5) Audio Frequency amplifiers:

This amplifier is used to increase the amplitude of an audio signal, in the range of human hearing (audio signals) that approximately 20Hz to 20kHz.

## 6) Wideband amplifiers:

Wideband amplifiers are capable of amplifying a very wide range of frequencies, typically from a few tens of hertz to several mega hertz.

## 7) Radio frequency amplifiers:

Radio frequency amplifiers operate in the band of frequencies that is normally associated with radio signals typically from 100kHz to over 1GHz.

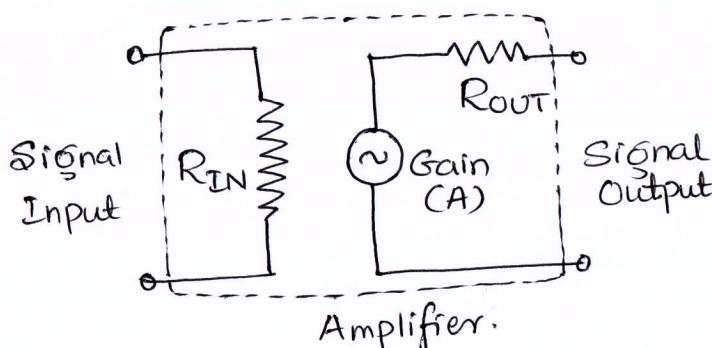
## 8) Low-noise amplifiers:

A low noise amplifier is an electronic amplifier that amplifies a very low-power signal. It will increase the power of both the signal and the noise present at its input, but the amplifier will also introduce some additional negligible noise to the signal being amplified. These amplifiers are usually designed for use with very small signal levels (usually less than 10mV or so).

Amplifiers can be thought of as a simple box or block containing the amplifying device, such as BJT, FET or Operational amplifier which has two input terminals and two output terminals with the output signal being much greater than that of the input signal as it has been "Amplified".

→ An ideal signal amplifier will have 3 main properties: Input Resistance ( $R_{IN}$ ), Output Resistance ( $R_{OUT}$ ) and of course amplification known commonly as Gain, or A.

### Ideal Amplifier Model



→ The amplified difference between the input and output signals is known as the Gain of the amplifier.

### GAIN

- Gain is basically a measure of how much an amplifier "amplifies" the input signal.
- for eg: If we have an input signal of 1V and an output of 50V, then the gain of the amplifier would be "50".
- In other words, the input signal has been increased by a factor of 50. This increase is called Gain.
- Amplifier gain is simply the ratio of the output divided by the input.
- Gain has no units as its a ratio.
- It is denoted as "A", for Amplification.

→ The introduction to the amplifier gain can be said to be the relationship that exists between the signal measured at the output with the signal measured at the input

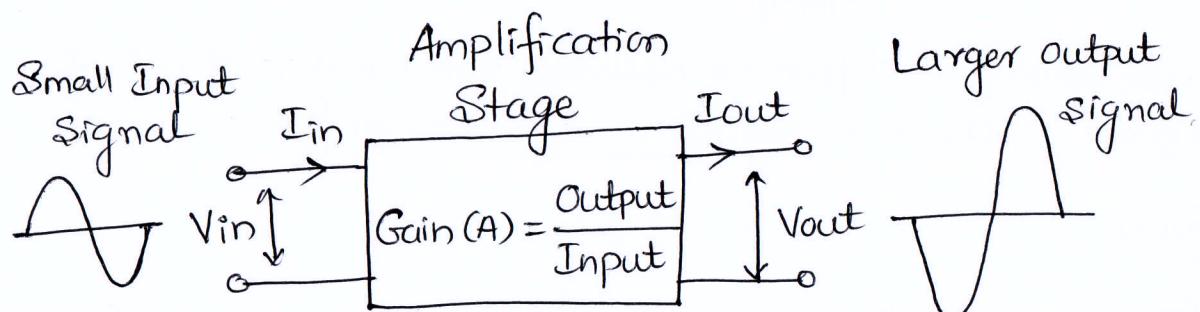
→ There are 3 different kinds of amplifier gain which can be measured and these are:

$$\text{i) Voltage gain } (A_v) = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_{\text{out}}}{V_{\text{in}}}.$$

$$\text{ii) Current gain } (A_i) = \frac{\text{Output Current}}{\text{Input current}} = \frac{I_{\text{out}}}{I_{\text{in}}}.$$

$$\text{iii) Power gain } (A_p) = \frac{\text{Output power}}{\text{Input power}} = \frac{P_{\text{out}}}{P_{\text{in}}}$$

### Amplifier Gain of the Input Signal.



→ Note that, since power is the product of current and voltage ( $P = IV$ ), we can infer that :

$$A_p = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_{\text{out}} \times V_{\text{out}}}{I_{\text{in}} \times V_{\text{in}}} = \frac{I_{\text{out}}}{I_{\text{in}}} \times \frac{V_{\text{out}}}{V_{\text{in}}} = [A_i A_v]$$

→ The power gain ( $A_p$ ) can also be expressed in Decibels (dB).

→ To calculate the gain of the amplifier in Decibels or dB, we can use the following expressions:

Voltage Gain in dB:  $A_v = 20 \times \log_{10}(A_v)$

Current Gain in dB:  $A_i = 20 \times \log_{10}(A_i)$

Power Gain in dB:  $A_p = 10 \times \log_{10}(A_p)$

→ Note that the DC power gain of an amplifier is equal to ten times the common log of the O/p to i/p ratio, whereas voltage and current gains are 20 times the common log of the ratio.

### Examples:

1) An amplifier produces an output voltage of 2V for an input of 50mV. If the input and output currents in the condition are 4mA and 200mA respectively. determine: the voltage gain, the current gain, the power gain.

Sol<sup>1</sup>: Given:  $V_{out} = 2V$ ,  $V_{in} = 50mV$ ,  $I_{in} = 4mA$ ,  $I_{out} = 200mA$

$$\therefore A_v = \frac{V_{out}}{V_{in}} = \frac{2V}{50mV} = 40$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{200mA}{4mA} = 50$$

and  $A_p = A_i \times A_v = 50 \times 40 = 2000$

2) The following measurements were made during a test on an amplifier:  $V_{in} = 250mV$ ,  $V_{out} = 10V$ ,  $I_{in} = 2.5mA$ ,  $I_{out} = 400mA$ . Determine  $A_v$ ,  $A_i$ ,  $A_p$ .

Sol<sup>2</sup>:  $A_v = \frac{V_{out}}{V_{in}} = \frac{10}{250mV} = 4$ ,  $A_i = \frac{I_{out}}{I_{in}} = \frac{400mA}{2.5mA} = 160$

$$A_p = A_i \times A_v = 160 \times 4 = 640$$

3) Determine the voltage, current and power gain of an amplifier that has an input signal of 1mA at 10mV and a corresponding output signal of 10mA at 1V. Also, express all three gains in decibels (dB).

Sol: Given:  $I_{in} = 1\text{mA}$ ,  $V_{in} = 10\text{mV}$ ,  $I_{out} = 10\text{mA}$ ,  $V_{out} = 1\text{V}$ .

$$\therefore A_v = \frac{V_{out}}{V_{in}} = \frac{1\text{V}}{10\text{mV}} = 100$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{10\text{mA}}{1\text{mA}} = 10$$

$$A_p = A_i \times A_v = 10 \times 100 = 1000$$

Amplifier Gains in Decibels(dB) :

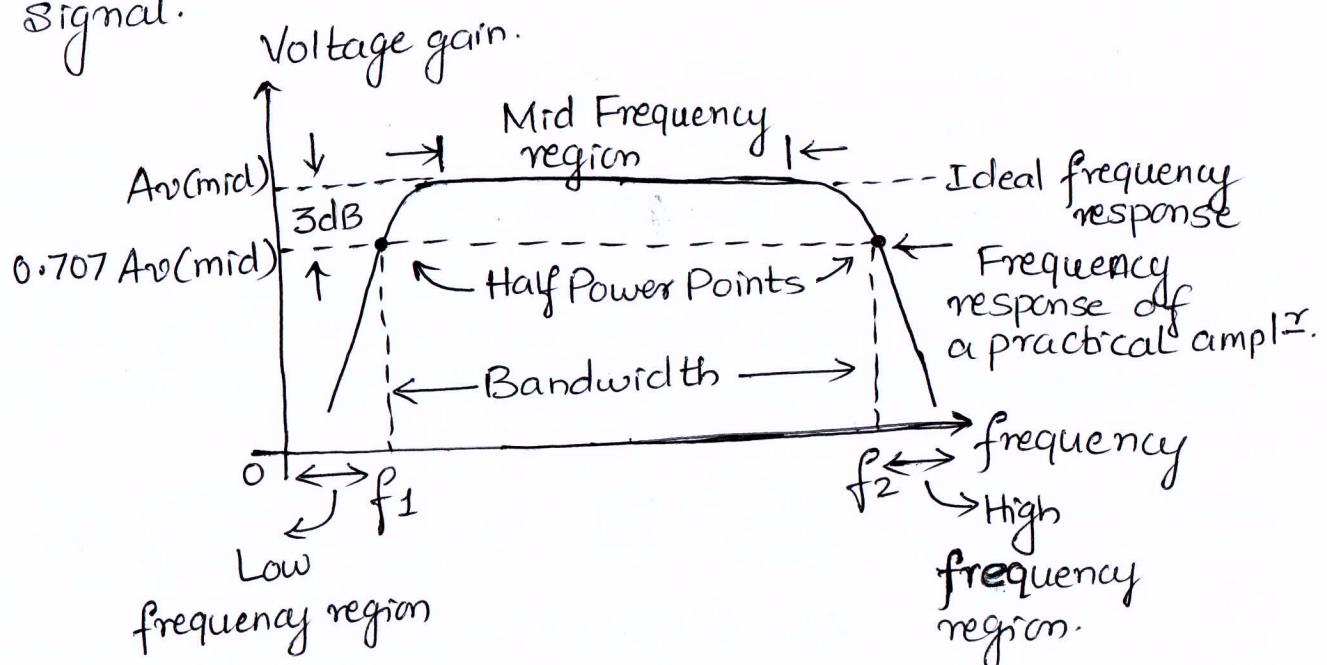
$$A_v = 20 \log_{10} A_v = 20 \log 100 = 40\text{dB}$$

$$A_i = 20 \log_{10} A_i = 20 \log 10 = 20\text{dB}$$

$$\& A_p = 10 \log_{10} A_p = 10 \log 1000 = 30\text{dB}$$

## Frequency Response.

→ The frequency response curve is a plot of the voltage gain of an amplifier against the frequency of input signal.



→ It is seen from the frequency response curve of an audio frequency amplifier that the gain of the amplifier remains fairly constant in the mid-frequency range, while the gain varies with frequency in low and high frequency regions of curve.

→ To indicate how constant an amplifier's gain is with frequency variation, we may specify the range of frequencies over which the gain does not deviate more than 70.7% of the maximum gain at some reference mid-frequency. This is shown in above fig', where these two frequencies are indicated as  $f_1$  &  $f_2$ .

→ Bandwidth of the amplifier is defined as the difference between  $f_2$  and  $f_1$ ; i.e., 
$$\boxed{B.W = f_2 - f_1}$$
.

→ The frequency,  $f_2$  is an high frequency region, while the frequency  $f_1$  is an low frequency region.

→ These two frequencies are also referred to as half-power frequencies or half-power points. Since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one-half the power at the reference frequency in mid-frequency region.

→ An audio amplifier works over the frequency range  $20\text{Hz}$  to  $20\text{kHz}$ . At half power frequencies, i.e. at  $f_1$  and  $f_2$  the gain is  $3\text{dB}$  less than the maximum amplifier gain in dB.

Let us assume that  $A_v = 100$ , then

$$\text{Gain in dB} = 20 \log_{10} 100 = 20 \times 2 = [40]$$

$$\text{at } f_1 \text{ and } f_2 \quad A_v = \frac{100}{\sqrt{2}} = 70.7$$

$$\therefore \text{Gain in dB at } f_1 \text{ & } f_2 = 20 \log 70.7 = [37]$$

$$\therefore \text{Maximum voltage - Gain at } f_1 \text{ & } f_2 = 40 - 37 = [3 \text{ dB}]$$

→ An amplifier has bandwidth of 500 kHz. If the lower cut-off frequency is 25 Hz, what is its upper cut-off frequency? Also find the voltage gain at the lower cut-off frequency if the midband gain is 120.

Sol<sup>n</sup>: Given: BW = 500 kHz,  $f_1 = 25 \text{ Hz}$ ,  $A_{mid} = 120$ .

$$\text{BW} = f_2 - f_1$$

$$\begin{aligned}\therefore f_2, \text{upper cutoff frequency} &= \text{BW} + f_1 \\ &= 500 \text{ kHz} + 25 \text{ Hz} \\ &= [500025 \text{ Hz}]\end{aligned}$$

The voltage gain at lower cut-off is 0.707 times the  $A_{mid}$ .

∴ Voltage gain at lower cut-off frequency is

$$0.707 \times 120 = [84.84]$$

### Phase Shift

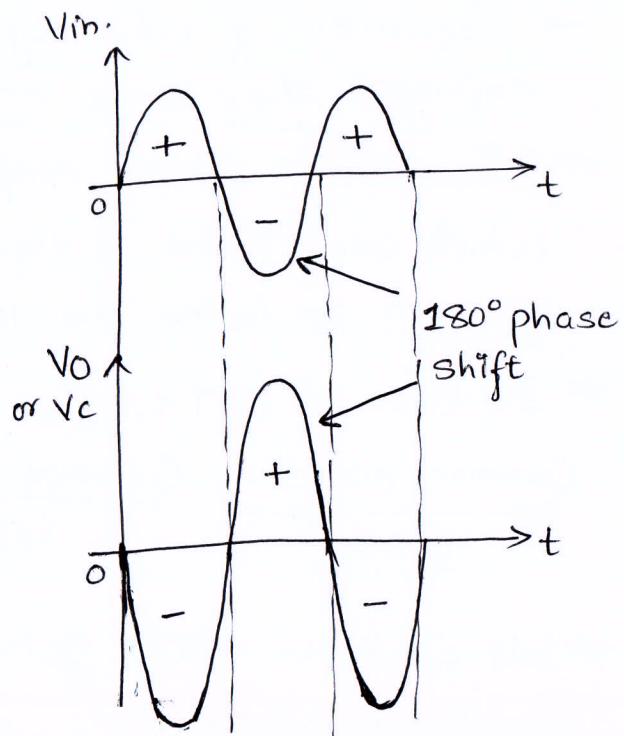
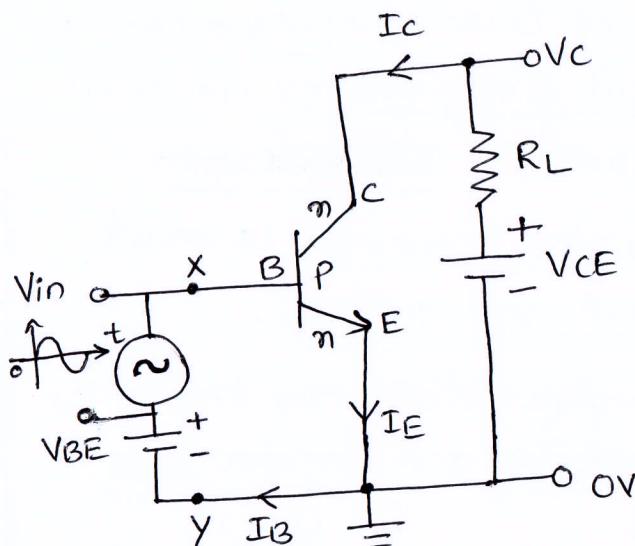
Phase shift is the phase angle between the input and output signal voltages measured in degrees.

→ Note that the difference between the phases of signal input voltage and signal output voltage in conventional single-stage transistor amplifiers is equal to  $180^\circ$ .

## Transistor Amplifiers.

- Regardless of what type of transistor (NPN or PNP) is employed, three basic circuit configurations are used.
- These three circuit configurations depend upon which one of the 3 transistor terminal is made common to both the input and output.
- In case of BJT's, the configurations are known as Common emitter, Common Collector and Common base.
  - (CE)
  - (CC)
  - (CB)
- We all know that gain is the ratio of Output divided by input.
- Therefore CE gain is  $B = \frac{I_C}{I_B}$ , similarly CC gain is  $\beta = \frac{I_E}{I_B}$  and CB gain is  $\alpha = \frac{I_C}{I_E}$ .
- From above gain equations we got to know that CE gain is greater than other two because of  $I_C/I_B$  as  $I_B$  is very negligible in  $I_E = I_C + I_B$  transistor current equation compared to  $I_C & I_E$ .
- Greater the gain, higher the amplification.
- Therefore CE configuration is widely used in case of amplification process.
- Now will see how CE configuration works as an amplifier.

## Common Emitter configuration as an Amplifier.



→ Here emitter is made common bet<sup>n</sup> input (base) and output (collector). Hence the name common emitter.

→ We know that  $[IE = Ic + IB]$ .

→ During positive half cycle of input voltage ( $V_{in}$ ), 'X' takes +ve, with this emitter-base junction becomes forward biased more along with  $V_{BE}$ . So,  $I_E$  increases and also  $I_B$  &  $I_C$  increases in the circuit.

→ Applying KVL to the output circuitry, we get

$$0 + V_{CE} - I_c R_L = V_c \rightarrow (1)$$

→ If  $I_c$  increases,  $V_c$  decreases more negatively.

→ Similarly, during negative half cycle of input voltage ( $V_{in}$ ), 'X' takes -ve, with this emitter-base junction becomes reverse biased. So,  $I_E$  decreases and also  $I_B$  and  $I_C$  decreases.

→ If  $I_c$  decreases,  $V_c$  increases more positively in equation (1)

- With this reason, we see  $180^\circ$  phase shift between input and output signals in CE configuration.
- Due to very high  $R_L$ , we get high amplified output as shown in waveforms above.
- Therefore transistor acts like Amplifier.
- Note: for amplification, emitter-base junction is made forward biased and collector-base junction is made reverse biased as shown in above circuit diagram.

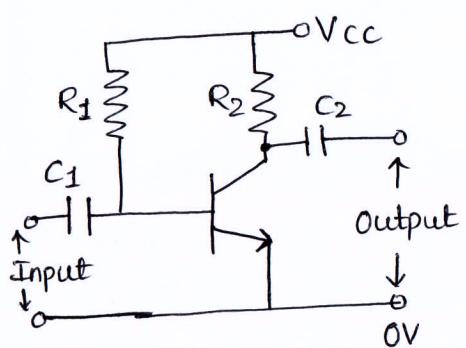
### Bias .

- From the output characteristics of CE configuration, we know that transistor operates in 3 regions irrespective of configurations.
- They are Active region, Saturation region & Cutoff region.
- For amplification, wkt emitter junction is to be forward biased and collector junction is to be reverse biased. which is nothing but transistor has to be operated in Active region only to get maximum amplification.
- For this, the circuit has to be biased properly for the faithful amplification, in the absence of input signal by using external dc voltage source.
- Biassing is the process of applying external dc voltages of correct polarity and magnitude to the two junctions of the transistor.
- Basically there are 3 transistor biasing circuits
  - i) Base Bias (Fixed Bias)
  - ii) Collector to Base Bias
  - iii) Voltage Divider Bias (Self Bias)

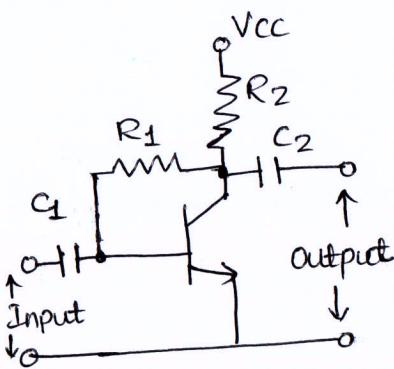
→ Out of these 3 biasing techniques, Voltage Divider Bias (Self Bias) is most commonly used because it provides the better stability of Q point (operating point) which makes transistor to work in Active region (middle of the DC load line) and gives high amplification.

(\*\* Q point (operating point) & DC load line will be explained later.)

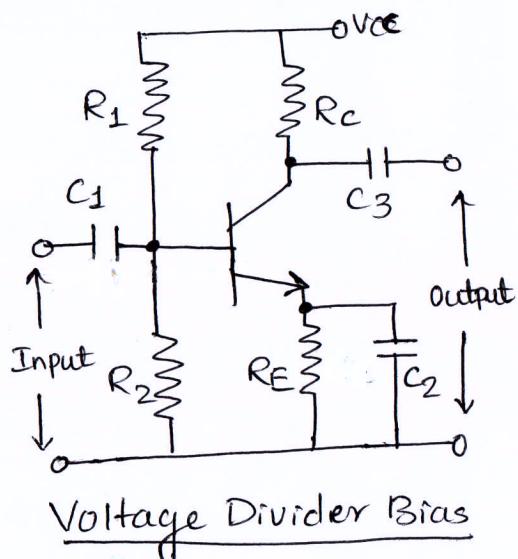
→



Base Bias (Fixed Bias)

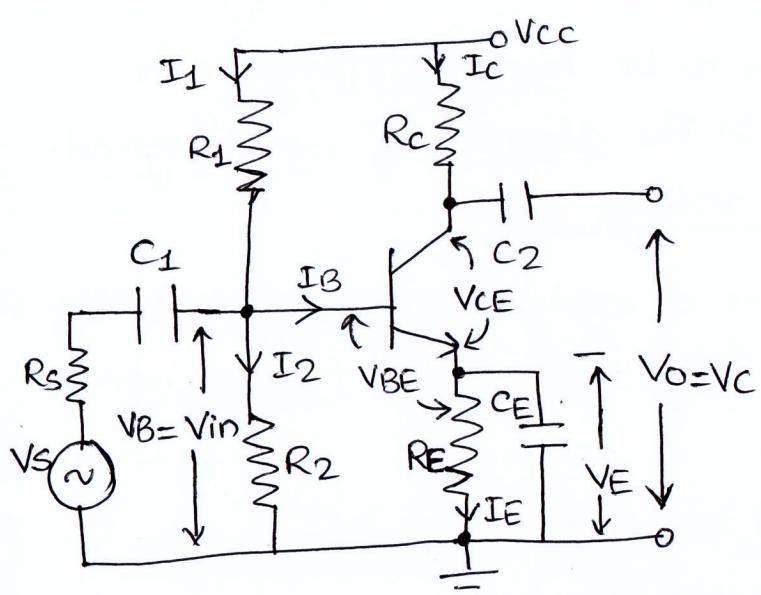


Collector to Base Bias



Voltage Divider Bias

CE Amplifier with effective bias stabilization.



$V_{CC}$  = Supply Voltage

$R_1, R_2 \& R_E$  = Biasing circuit

$C_1$  = Input coupling capacitor

$C_2$  = Output coupling capacitor

$C_E$  = Emitter Bypass Capacitor

$V_E$  = Emitter voltage

$V_C$  = Collector voltage

$V_B$  = Base voltage

$V_{BE}$  = Built in potential

$V_{CE}$  = Junction potential.

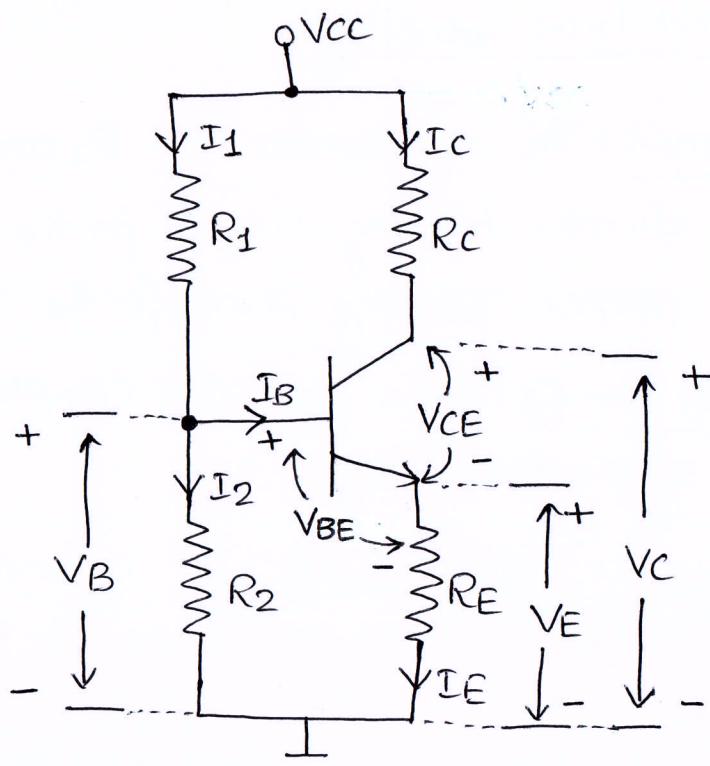
- The above circuit shows the voltage divider bias circuit.
- This is the most widely used biasing circuit and provides good bias stability.
- Biasing Circuit: The resistances  $R_1$ ,  $R_2$  and  $R_E$  forms the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.
- Input Capacitor,  $C_1$ : This capacitor couples the signal to the base of the transistor.
- Emitter Bypass Capacitor,  $C_E$ :  $C_E$  is connected in parallel with the emitter resistance,  $R_E$  to provide a low reactance path to the amplified ac signal. If this is not inserted, the amplified ac signal passing through  $R_E$  will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.
- Output Coupling Capacitor,  $C_2$ : The coupling capacitor  $C_2$  couples the output of the amplifier to the load or to the next stage of the amplifier.

Note: With respect to signal, capacitors  $C_1$ ,  $C_2$  &  $C_E$  acts as Short Circuit.

With respect to DC ( $V_{CC}$ ), all capacitors acts as open circuit.

Thus for dc analysis, we need to consider all capacitors as Open Circuit.

# Voltage Divider Bias DC Analysis.



From above circuit, we get

$$\boxed{V_B = V_{BE} + V_E} \quad \text{OR} \quad \boxed{V_B = I_2 R_2 = \frac{V_{CC} R_2}{R_1 + R_2}} \quad \begin{matrix} \text{by Thumb} \\ \text{Rule.} \\ \text{across } R_2 \end{matrix}$$

$$\therefore \boxed{V_{BE} = V_B - V_E} \quad \rightarrow (1)$$

$$\boxed{V_E = I_E R_E} \quad \rightarrow (2)$$

$$\boxed{I_E = I_C + I_B} \quad \rightarrow (3) \quad \text{OR} \quad \boxed{I_E = \frac{V_E}{R_E}} \quad \text{from eqn (2)}$$

$$\boxed{I_C = \beta I_B} \quad \rightarrow (4) \quad \text{OR} \quad \boxed{I_C \approx I_E} \quad \begin{matrix} \text{so } I_B \text{ is} \\ \text{negligible} \\ \text{from eqn (3).} \end{matrix}$$

$$\boxed{I_B = I_1 - I_2} \quad \rightarrow (5)$$

$$\boxed{V_C = V_{CE} + V_E} \quad \text{OR} \quad \boxed{V_C = V_{CC} - I_C R_C} \quad \begin{matrix} \text{by applying} \\ \text{KVL at O/P circuitry} \end{matrix}$$

$$\therefore \boxed{V_{CE} = V_C - V_E} \quad \rightarrow (6)$$

→ A voltage divider bias circuit is shown above, this is the most widely used biasing circuit and provides good bias stability.

→ The goal of Transistor Biasing is to establish a constant Quiescent Operating Point ( $Q$ -Point) exactly at the centre of DC load line to achieve good and highest amplification (undistorted symmetrical output signal).

→ Constant  $Q$ -point indicates, there should not be any change in the circuit parameters irrespective of change in temperature or  $\beta$  values.

→ Here, two resistors  $R_1$  and  $R_2$  are employed, which are connected to  $V_{CC}$  and provide biasing.

→ The resistor,  $R_E$  employed in the emitter provides stabilization.

→ The name voltage divider comes from the voltage divider formed by  $R_1$  and  $R_2$  which divides the supply voltage  $V_{CC}$ .

→ The voltage drop across  $R_2$  forward biases the base-emitter junction, this causes the base current ( $I_B$ ) and hence collector current ( $I_C$ ) flow in the zero signal conditions (no signal).

→ As base current ( $I_B$ ) is very negligible, therefore it can be assumed that  $I_1 = I_2$  through  $R_2$

$$\text{i.e., } I_B = I_1 - I_2$$

$$0 = I_1 - I_2$$

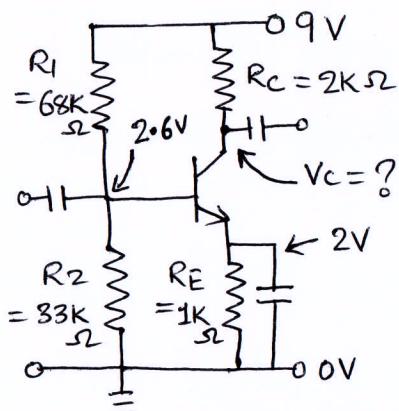
$$\therefore \boxed{I_1 = I_2}$$

→ From the above circuit, excellent bias stability is provided by  $R_E$  as follows:

From the above equations (eqn 1 to eqn 6)

- If  $I_c$  increases due to the rise in temperature,  $I_E$  also increases ( $\because I_E = I_c$ ) causing an increased potential drop across  $R_E$ .
- Therefore  $V_E$  also increases ( $\because V_E = I_E R_E$ ), which in turn decreases the  $V_{BE}$  ( $\because V_{BE} = V_B - V_E$ ).
- This in turn causes  $I_B$  to decrease and hence  $I_c = \beta I_B$ , so  $I_c$  will be restored back to its original value and hence the Q point gets stabilized by  $R_E$ .
- Therefore, we can say that negative feedback exists in the emitter bias circuit.
- This reduction in  $I_c$  compensates for the original change in  $I_c$ .
- Hence we get constant Q-point irrespective of change in temperature or  $\beta$ -value.

Example: Determine the static value of current, gain and collector voltage in the circuit shown.



Sol<sup>n</sup>: Given:  $V_{CC} = 9V$ ,  $R_1 = 68k\Omega$ ,  $R_2 = 33k\Omega$   
 $R_C = 2k\Omega$ ,  $R_E = 1k\Omega$ ,  $V_E$  = Voltage drop across  $R_E$  &  $V_B = 2.6V$   $R_E = 2V$

$I_B = ?$ ,  $I_E = ?$ ,  $I_c = ?$ ,  $V_c = ?$ ,  $\beta = ?$

$$I_E = \frac{V_E}{R_E} = \frac{2V}{1k\Omega} = [2mA]$$

$$I_B = I_1 - I_2, I_1 = \frac{\text{Voltage drop across } R_1}{R_1}$$

$$= \frac{9V - 2.6V}{68k\Omega} = [94.1\mu A]$$

$$I_2 = \frac{\text{Voltage drop across } R_2}{R_2} = \frac{2.6V - 0V}{33k\Omega} = [79\mu A]$$

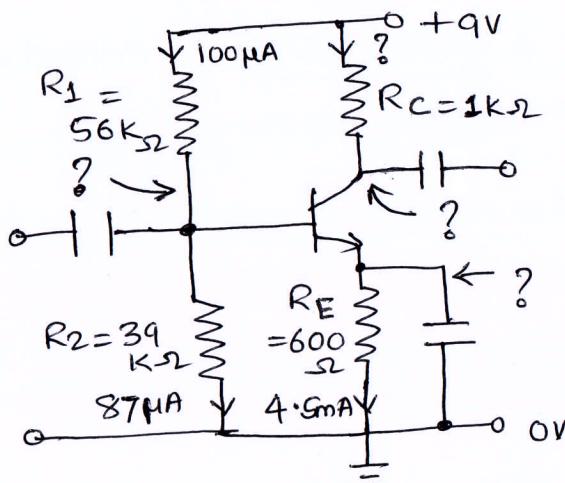
$$\therefore I_B = I_1 - I_2 = 94.1 \mu A - 79 \mu A = [15.1 \mu A]$$

$$I_C = I_E - I_B = 2 \text{ mA} - 15.1 \mu \text{A} = [2.0151 \text{ mA}]$$

$$\beta = \frac{I_C}{I_B} = \frac{2.0151 \text{ mA}}{15.1 \mu \text{A}} = [133.45]$$

$$V_C = V_{CC} - I_C R_C = 9 \text{ V} - (2.0151 \text{ mA} \times 2 \text{ k}\Omega) = [4.96 \text{ V}]$$

2) Determine the unknown current and voltages in fig. given.



Sol<sup>Q</sup>: Given;  $V_{CC} = 9 \text{ V}$ ,  $R_1 = 56 \text{ k}\Omega$ ,  $R_2 = 39 \text{ k}\Omega$ ,  $R_C = 1 \text{ k}\Omega$ ,  $R_E = 600 \Omega$ ,  $I_1 = 100 \mu\text{A}$ ,  $I_2 = 87 \mu\text{A}$ ,  $I_E = 4.5 \text{ mA}$ ,  $I_C = ?$ ,  $V_C = ?$ ,  $V_E = ?$ ,  $V_B = ?$

$$I_B = I_1 - I_2 = 100 \mu\text{A} - 87 \mu\text{A} = [13 \mu\text{A}]$$

$$I_C = I_E - I_B = 4.5 \text{ mA} - 13 \mu\text{A} = [4.487 \text{ mA}]$$

$$V_C = V_{CC} - I_C R_C = 9 \text{ V} - (4.487 \times 10^{-3} \times 1 \times 10^3) \\ = [4.513 \text{ V}]$$

$$V_E = I_E R_E = 4.5 \text{ mA} \times 600 = [2.7 \text{ V}]$$

$$V_B = V_{BE} + V_E = 0.7 + 2.7 = [3.4 \text{ V}]$$

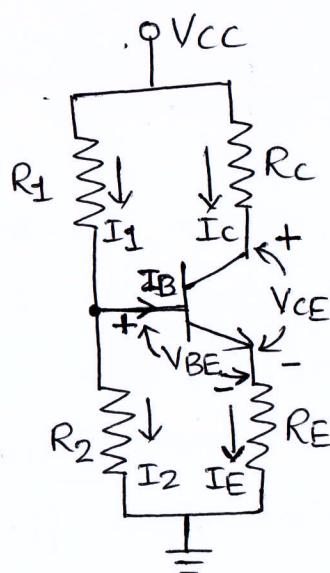
↑  
[ Built in Potential ]  
of Si<sup>o</sup>

## Predicting Amplifier Performance

( DC Load Line & Bias Point/operating Point).

- The DC load line of BJT Biasing circuit is a straight line drawn on the transistor output characteristics by joining two points (Pt. A on x-axis & pt.B on y-axis).
- For a Common-emitter (CE) circuit, the load line is a graph of Collector current ( $I_C$ ) versus Collector-emitter ( $V_{CE}$ ) voltage, for a given value of collector resistance ( $R_C$ ) and a given supply voltage ( $V_{CC}$ ).
- The load line shows all corresponding levels of  $I_C$  and  $V_{CE}$  that can exist in a particular circuit.

→



- Considering the CE circuit shown above, note that the polarities of the transistor terminal voltage are such that the base-emitter junction is forward biased and the collector-emitter junction is reverse biased.
- These are the normal bias polarities for the transistor junctions.
- The DC line for the above circuit is drawn on the device common-emitter O/P characteristics shown below.

→ By Applying KVL at the O/P circuitry of above circuit we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \rightarrow \text{eq } (1)$$

→ We know that, in CE configuration, emitter terminal is made common betw collector and base, so we don't see emitter parameters in the O/P characteristics of CE configuration.

→ Thus  $I_E \approx I_C$ , because of very negligible  $I_B$  in  $I_E = I_C + I_B$

→ With this,  $I_E$  is replaced by  $I_C$  in above equation (1)

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E \rightarrow \text{eq } (2)$$

→ To locate point A of DC load line on x-axis,  $I_C$  should be substituted as zero (0). in eq (2) [∴ current will be zero on x-axis]

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_{CE} = V_{CC} - 0 (R_C + R_E)$$

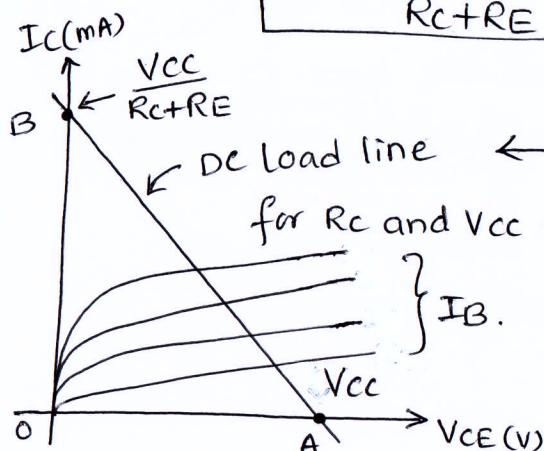
$\therefore V_{CE} = V_{CC}$  → Point A of DC load line on x-axis.

→ Similarly, to locate DC load line point B on y-axis,  $V_{CE}$  should be substituted as zero (0) in eq (2)

$$\therefore V_{CC} = I_C R_C + I_C R_E + 0 \quad [\because \text{voltage will be zero on y-axis}]$$

$$V_{CC} = I_C (R_C + R_E)$$

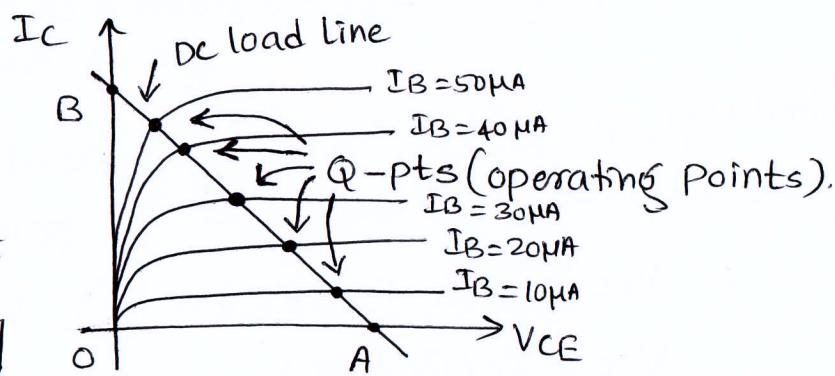
$$\therefore I_C = \frac{V_{CC}}{R_C + R_E} \rightarrow \text{Point B of DC load line on y-axis.}$$



The straight line drawn through points 'A' and 'B' is the dc load line for  $R_C$  and  $V_{CC}$ .

\* If either of these two quantities ( $R_C$  or  $V_{CC}$ ) is changed, a new load line must be drawn.

- As already stated, the dc load line represents all corresponding  $I_C$  and  $V_{CE}$  levels that can exist in the circuit as represented by eq<sup>n</sup>(2).
- Knowing any one of  $I_B$ ,  $I_C$  or  $V_{CE}$  (CE O/P characteristics parameters) it is easy to determine the other two from a dc load line drawn on the device characteristics.
- The dc bias point or quiescent point (Q-point) (also known as the dc operating point) identifies the collector current and collector-emitter voltage of the transistor when there is no input signal at the base terminal.
- In simple words, for different values of constant  $I_B$ , we have different intersection points of the output curve and dc load line in CE O/P characteristics. This point is called Quiescent point (Q-pt) or Operating point as shown below.

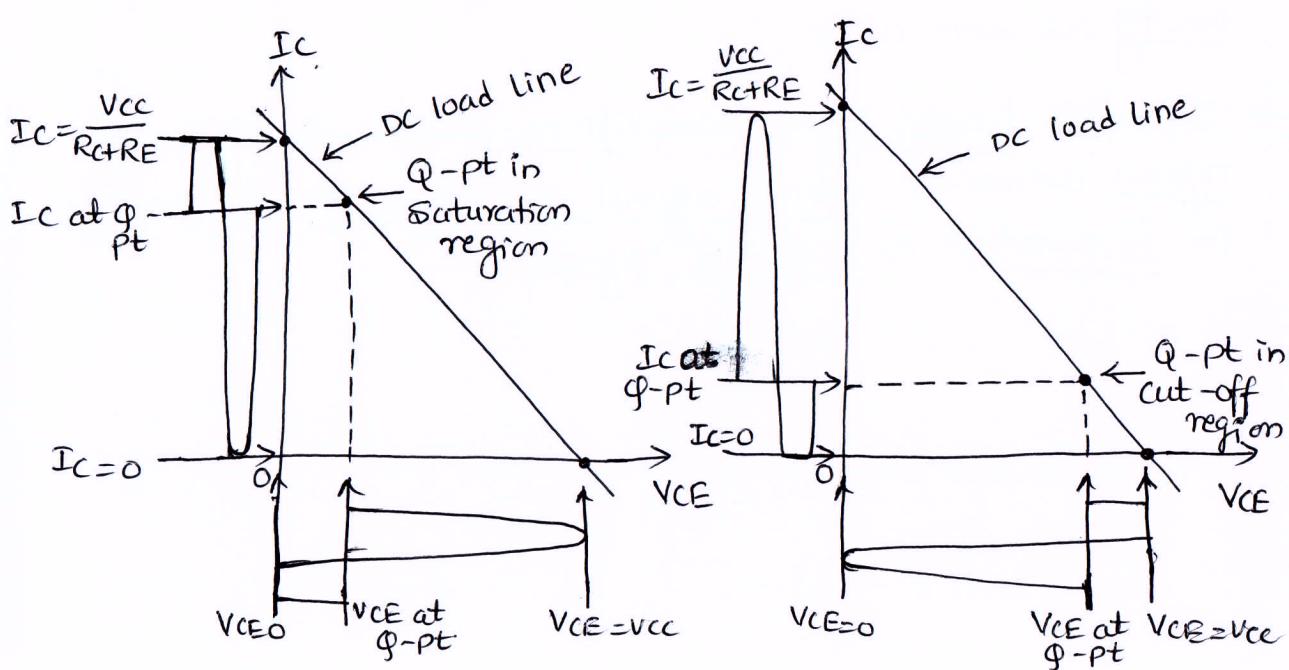
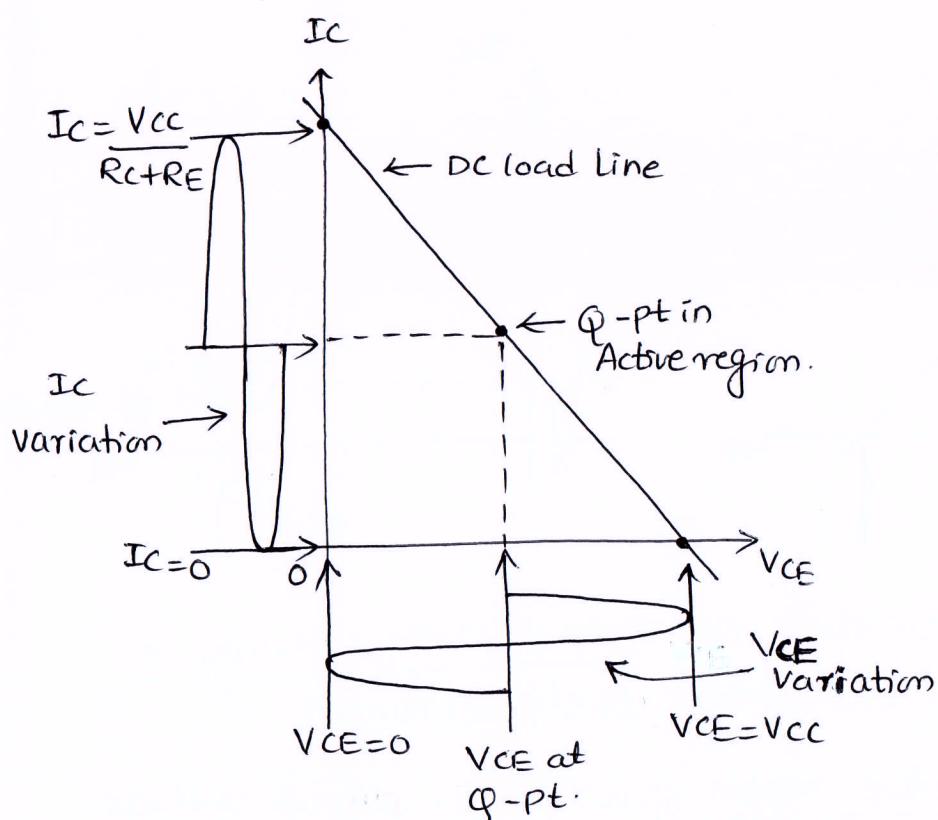


Q-point is the set of  $V_{CE}$  and  $I_C$   
i.e.,  $\boxed{Q(V_{CE}, I_C)}$

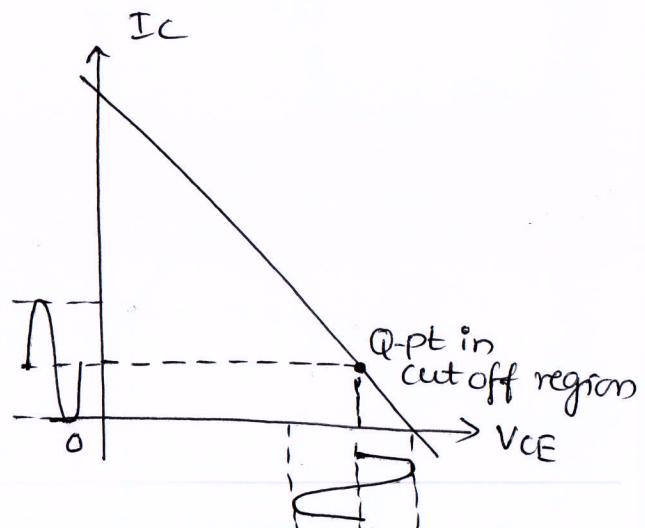
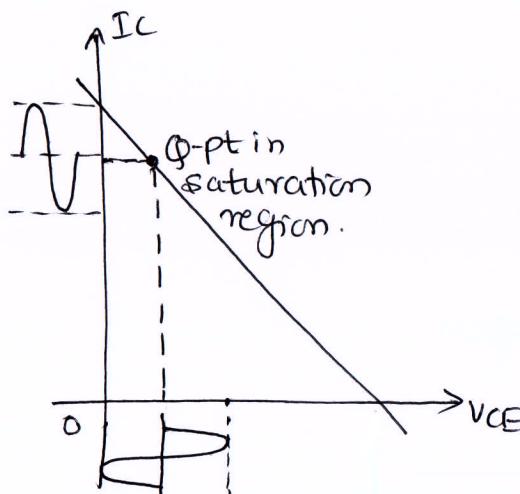
- Each Q-point gives us the combination of  $V_{CE}$  and  $I_C$ .
- Out of which, we need to select the best Q-point for the particular circuit to get the faithful amplification.
- Selection of Q-point depends on the type of application and its requirement.

- The operating point should not get disturbed as it should remain stable to achieve faithful amplification.
- Hence, the Q-point is the value where the Faithful Amplification is achieved.
- Faithful Amplification is the process of obtaining complete portions (symmetrical) of input signal by increasing the signal strength (amplification).

### Selection of Q-point



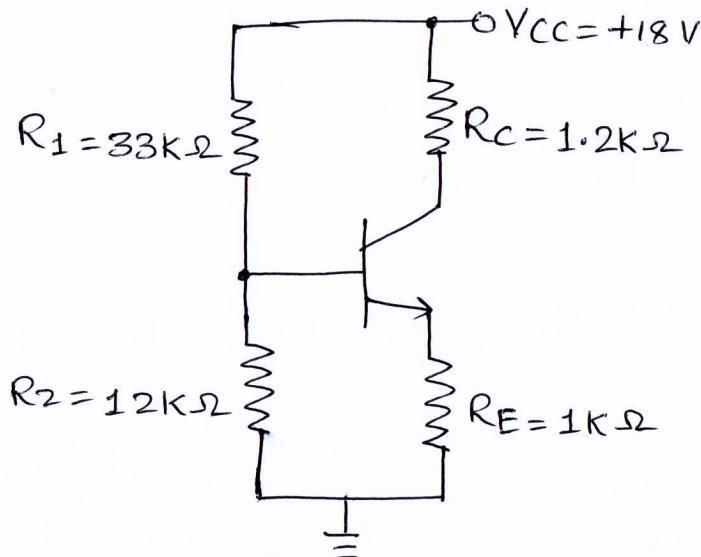
- From the above figures of selection of Q-pt. we can observe that Selecting Q-pt at the exact center of the DC load line (ie; in active region) we get complete portions of the signal without any disturb/distortions.
- Selecting Q-pt near to Saturation or cut-off regions gives asymmetrical swing of signal (distorted portions)
- But, still we can achieve symmetrical swing even though we choose Q-pt in Saturation or Cut-off region, as shown below.



- We can observe that, the output voltage swing is symmetrical but for smaller portions (range)
- Q-point in Active region gives Larger output voltage swing as seen above.
- Therefore Large signal amplifiers prefers Q-pt in Active region whereas Small signal amplifiers prefers Q-pt in Saturation or Cut-off regions.

## Numericals

i) Analyze the voltage divider bias circuit shown, to determine the emitter voltage, collector voltage and collector-emitter voltage. Assuming  $V_{BE} = 0.7V$ .



SOL:

i) Emitter Voltage,  $V_E = V_B - V_{BE}$

$$V_B = \frac{V_{CC}R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 + 12} = [4.8V]$$

$$\therefore V_E = 4.8 - 0.7 = [4.1V]$$

ii) Collector Voltage,  $V_C = V_{CC} - I_C R_C$

$$I_C \approx I_E, \quad I_E = \frac{V_E}{R_E} = \frac{4.1V}{1k\Omega} = [4.1mA]$$

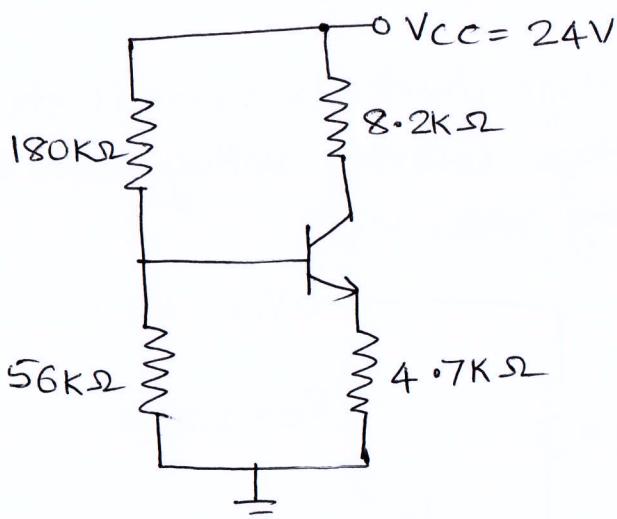
$$\therefore [I_C = 4.1mA]$$

$$\therefore V_C = 18V - 4.1mA \times 1.2k\Omega = [13.1V]$$

iii) Collector-Emitter voltage,  $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

OR  $V_{CE} = V_C - V_E$   $= 13.1V - 4.1V = [9V]$

2) Determine  $I_C$ ,  $V_E$ ,  $V_C$ ,  $V_{CE}$  &  $I_E$  for the circuit shown.



Sol<sup>n</sup>: Given,  $V_{CC} = 24V$ ,  $R_1 = 180k\Omega$ ,  $R_2 = 56k\Omega$ ,  $R_C = 8.2k\Omega$   
 $R_E = 4.7k\Omega$

i)  $I_C \approx I_E$

$$I_E = \frac{V_E}{R_E}, V_E = V_B - V_{BE}, V_B = \frac{V_{CC}R_2}{R_1 + R_2} = \frac{24 \times 56k}{180k + 56k} = 5.69V$$

$$\therefore V_E = 5.69V - 0.7V = 4.99V$$

$$\therefore I_E = \frac{4.99V}{4.7k\Omega} = 1.06mA$$

$$\therefore I_C \approx I_E = 1.06mA$$

ii)  $V_E = 4.99V$

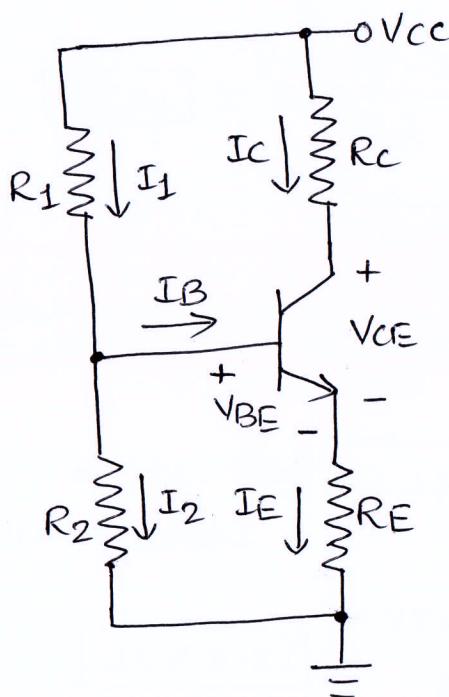
iii)  $V_C = V_{CC} - I_C R_C = 24 - 1.06mA \times 8.2k\Omega = 15.308V$

iv)  $V_{CE} = V_C - V_E = 15.308V - 4.99V = 10.318V$

v)  $I_E = 1.06mA$

## Voltage Divider Bias Circuit Design.

- When one is designing a voltage-divider bias circuit, the voltage-divider current ( $I_2$ ) should be selected to be much larger than the transistor base current ( $I_B$ ).
- This makes the base voltage ( $V_B$ ) a stable quantity largely unaffected by the ' $\beta$ ' value of the transistor.



$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$R_E = \frac{V_E}{I_C} \quad \therefore I_E \approx I_C$$

$$R_2 = \frac{V_B}{I_2}$$

$$I_2 = \frac{I_C}{10}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2}$$

$$V_E \gg V_{BE}$$

- General thumb rule used to select  $I_2$  approximately equal to one-tenth of the transistor collector current,  $I_C$ .
- Next if  $V_E$  is not specified then assume  $V_E \gg V_{BE}$ .
- The reason for selecting  $V_E > V_{BE}$  is that as  $V_{BE}$  generally varies depending on the type of transistor (Germanium/Silicon), and also changes with change in temperature as  $V_E > V_{BE}$  the effect of changes in  $V_{BE}$  does not effect circuit conditions but not greater than  $V_{CE}$ .
- The standard design equations are given above.

## Numericals on Voltage-Divider Design.

MCL

- 1) Design the voltage divider bias circuit to have  $V_{CE} = V_E = 5V$  and  $I_C = 5mA$  when the supply voltage is 15V. Assume the transistor  $\beta$  is 100.

Sol: Given,  $V_{CE} = V_E = 5V$ ,  $I_C = 5mA$ ,  $V_{CC} = 15V$ ,  $\beta = 100$

$$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C} = \frac{5V}{5mA} = [1k\Omega]$$

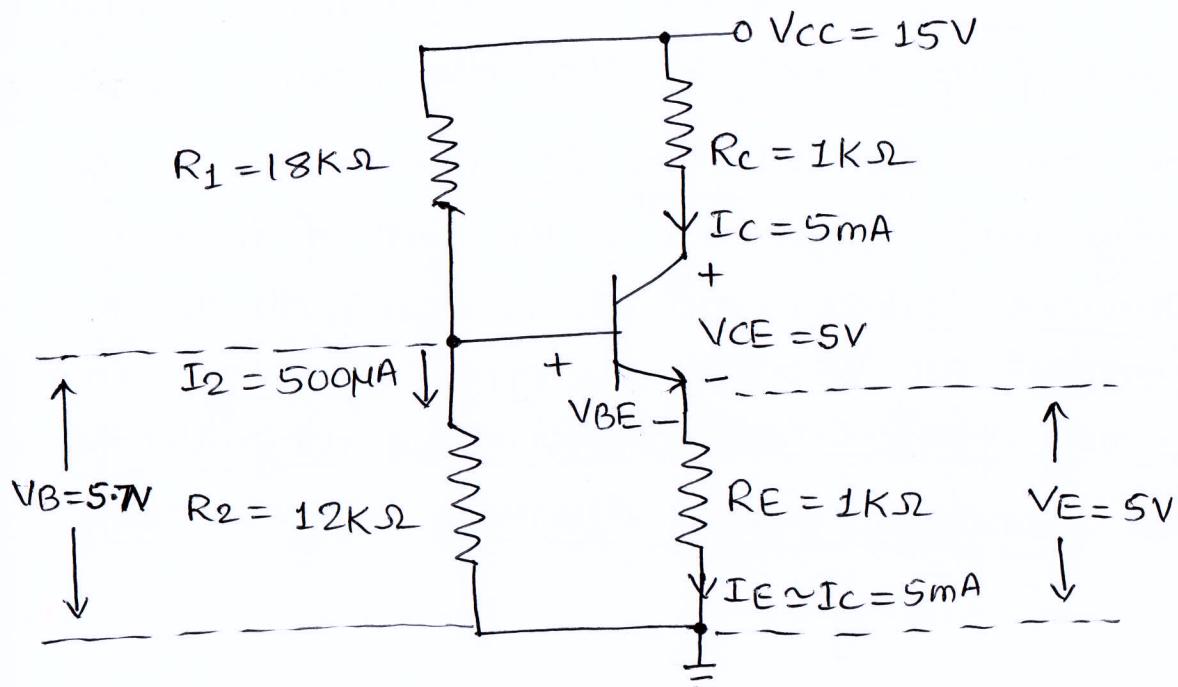
$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{15V - 5V - 5V}{5mA} = [1k\Omega]$$

$$I_2 = \frac{I_C}{10} = \frac{5mA}{10} = [500\mu A]$$

$$V_B = V_E + V_{BE} = 5V + 0.7V = [5.7V]$$

$$R_2 = \frac{V_B}{I_2} = \frac{5.7V}{500\mu A} = [11.4k\Omega] \text{ (use } 12k\Omega \text{ standard value)}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{15V - 5.7V}{500\mu A} = [18.6k\Omega] \text{ (use } 18k\Omega \text{ standard value)}$$



2) Design the voltage divider bias circuit. The circuit have  $V_{CC} = 12V$ ,  $V_{CE} = 5V$ ,  $I_C = 3mA$ . Assume  $\beta = 100$ .

Sol: Given,  $V_{CC} = 12V$ ,  $V_{CE} = 5V$ ,  $I_C = 3mA$ ,  $\beta = 100$

$$I_B = \frac{I_C}{\beta} = \frac{3mA}{100} = [30\mu A]$$

$$I_E = I_C + I_B = 3mA + 30\mu A = [3.03mA]$$

$$R_E \frac{V_E}{I_E} = \frac{3V}{3.03mA} = 990\Omega = 910\Omega \text{ (standard value)}$$

Here  $V_E$  is assumed value, Since  $V_{CE} = 5V$ ,  
so  $V_E$  is assumed less than  $V_{CE}$  i.e,  $[3V]$ .

Practically,  $V_E = I_E \times R_E = 3.03mA \times 910 = [2.757V]$   
 $\approx 3V$ .

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{12V - 5V - 2.757V}{3mA}$$

$$= 1.414k\Omega = [1.2k\Omega] \text{ (standard value)}$$

$$V_B = V_E + V_{BE} = 2.757V + 0.7V = [3.457V]$$

$$I_2 = \frac{I_C}{10} = \frac{3mA}{10} = [300\mu A]$$

$$R_2 = \frac{V_B}{I_2} = \frac{3.457V}{300\mu A} = 11.523k\Omega = [11k\Omega]$$

$$\text{(standard value)}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{12V - 3.457V}{300\mu A} = 24.812k\Omega = [22k\Omega]$$

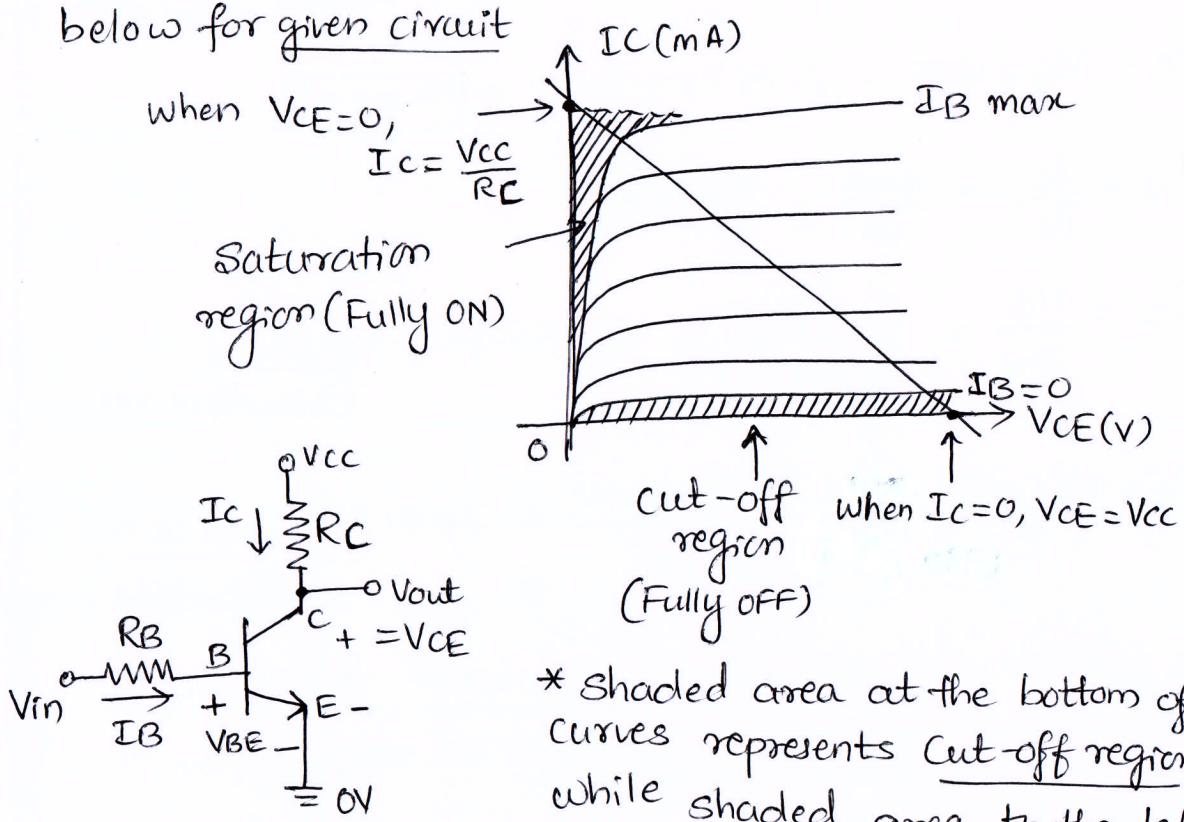
$$\text{(standard value)}$$

\*\* Mention all the above calculated values in  
the voltage-divider circuit as we did in  
previous example.

## CE Configuration as Switch: Cut-off & Saturation modes.

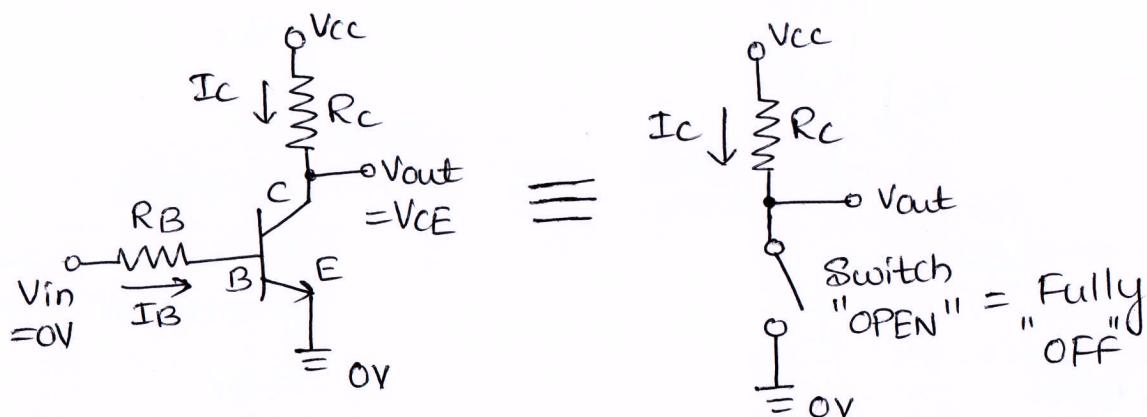
MCL

- BJT's can be used as an amplifier, filter, rectifier, oscillator or even a switch.
- The transistor will operate as an amplifier, if it is baised into the Active region (base-emitter junction forward biased and collector-base junction reverse biased).
- The transistor can be used as a switch if baised in the Saturation and Cut-off regions.
- This means that we can ignore the operating Q-pt biasing and voltage divider circuitry required for amplification, and use the transistor as a switch by driving it back and forth between if "Fully-OFF" (Cut-off) and "Fully-ON" (Saturation) regions as shown below for given circuit



\* Shaded area at the bottom of the curves represents Cut-off region while shaded area to the left represents Saturation region.

## 1) Cut-off Region.



→ In cut-off region, the operating conditions of the transistor are  $I_B = 0$ ,  $I_C = 0$ ,  $V_{CE} = \text{Max} = V_{CC}$  as seen in above characteristics, when  $V_{in} = 0V$

→ Which results in large depletion layer and no current flowing through the device.

→ Therefore the transistor is switched "Fully - OFF".

### \* Cut-off Characteristics

→ When  $V_{in} = 0V$ , Base-Emitter voltage  $V_{BE}$  will be lesser than built-in potential (i.e.,  $V_{BE} < 0.7V$ ).

→ With this BE junction will be reverse biased and also the BC junction is reverse biased. Transistor is fully "OFF". No Collector current ( $I_C = 0$ )

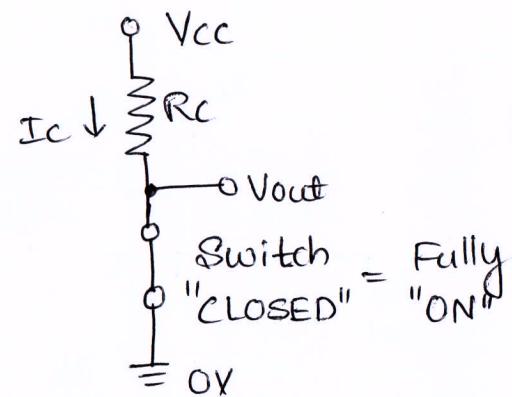
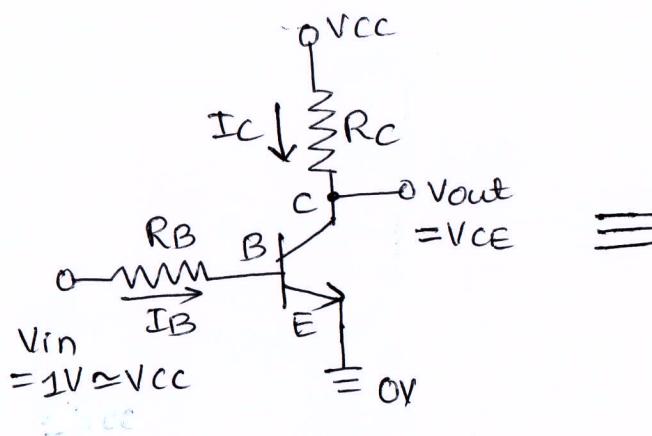
Applying KVL to the above circuit across O/P, we get  $V_{CC} = I_C R_C + V_{CE}$

$$\therefore V_{CE} = V_{CC} - I_C R_C \\ = V_{CC} - 0 \times R_C$$

$\therefore V_{CE} = V_{CC}$  maximum collector-emitter voltage = 1V

→ Therefore transistor operates as an "Open Switch"

## 2) Saturation Region.



→ Here the transistor will be biased so that the maximum amount of base current ( $I_B$ ) is applied (ie,  $I_{B\max}$ ) as seen in characteristics.

→ This resulting in maximum collector current ( $I_c$ ) in turn resulting in the minimum collector-emitter voltage ( $V_{CE}$ ).

→ Which results in the depletion layer being as small as possible and maximum current flowing through the transistor.

→ Therefore the transistor is switched "Fully-ON".

### \* Saturation characteristics.

→ When  $V_{in} = 1V \approx V_{cc}$ ,  $V_{BE}$  will be greater than  $0.7V$  (ie;  $V_{BE} > 0.7V$ ).

→ With this BE junction and BC junction both will be forward biased. Transistor is fully "ON".

→ Maximum Collector Current ( $I_c = V_{cc}/R_c$ )

Applying KVL to the above circuit at o/p circuitry we get,

$$V_{cc} = I_c R_c + V_{CE}$$

$$\therefore V_{CE} = V_{cc} - I_c R_c$$

$$= V_{cc} - \frac{V_{cc}}{R_c} \cdot R_c$$

$$\therefore \boxed{V_{CE} = 0V}$$

→ Minimum collector-emitter voltage across o/p.

→ Therefore transistor operates as a "closed Switch"