

## UNIT IV

### FLIP FLOPS

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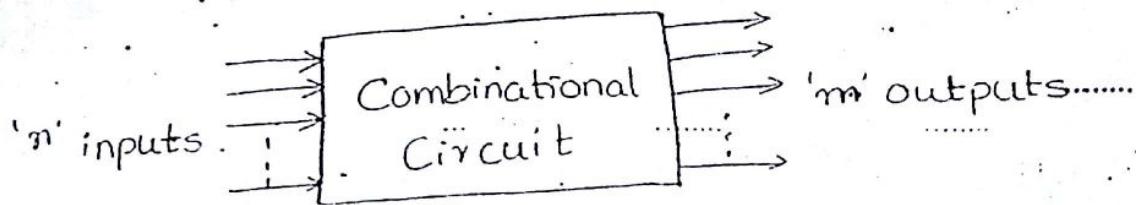
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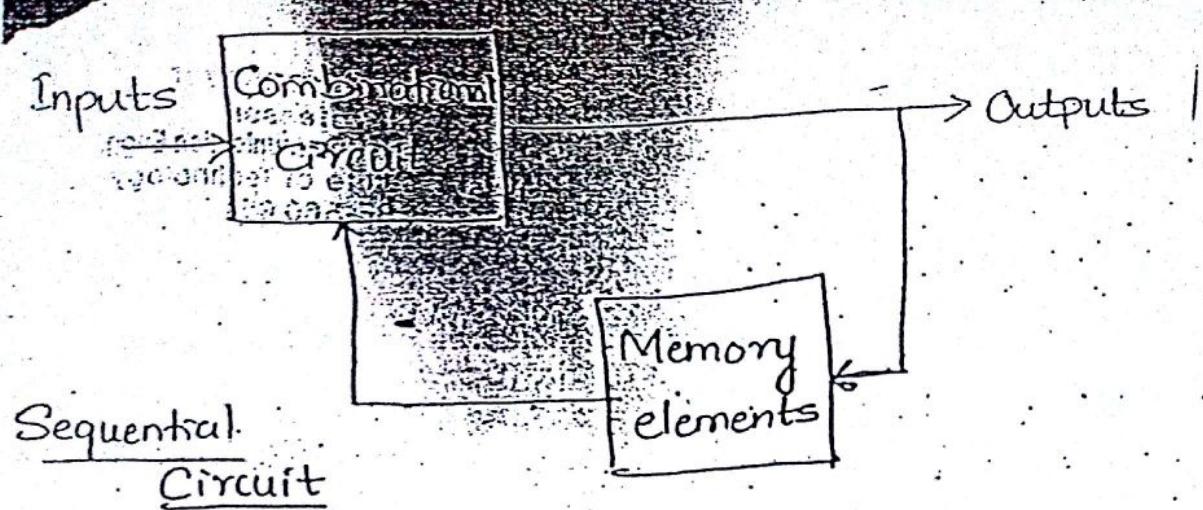
#### Introduction to Flip Flops:

- Logic circuits for digital systems may be combinational or sequential.
- A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs.
- A combinational circuit consists of input states, logic gates, and output variables.



Combinational Circuit

- A sequential circuit consists of combinational circuit, to which storage elements are connected to form a feedback path.
- The storage elements are devices capable of storing binary information.
- A logic circuit designed to produce a specified output for certain combination of input variables with storage facility, the resulting circuit is called Sequential circuit shown below.



→ The outputs to be generated that are not only dependent on the present input combinations or conditions but they also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.

### Comparison between Combinational & Sequential Circuits

#### Combinational Circuits

- 1) The o/p variables dependent only on the combination of i/p variables.
- 2) Memory unit is not required.
- 3) It is faster in speed.
- 4) It is easy to design.
- 5) e.g.: Parallel Adder

#### Sequential circuits

- 1) The o/p variables dependent not only on present i/p variables but also dependent on previous o/p variables.
- 2) Memory unit is required to store previous o/p's.
- 3) It is slower in speed.
- 4) It is harder to design.
- 5) Eg: Serial Adder.

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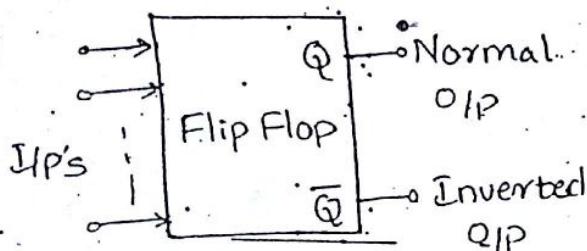
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The storage elements used in sequential circuits are called FLIP FLOPS.

→ A flip-flop is a binary storage device capable of storing one bit of information.

→ A sequential circuit may use many flip flops to store as many bits as necessary.



Flip-Flop Symbol

#### Output States

$Q=1, \bar{Q}=0$  : It is called HIGH state  
also called SET state.

$Q=0, \bar{Q}=1$  : It is called LOW or 0 state  
also called RESET state.

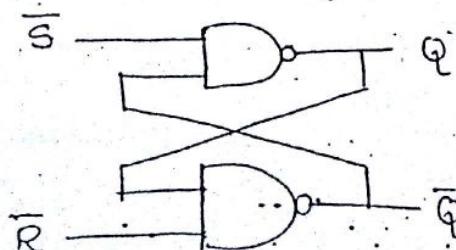
#### Latch

A latch is the most basic type of flip flop circuit. It can be constructed using NAND or NOR gates. According to the latch are of two types:

- 1) NAND gate latch
- 2) NOR gate latch

#### 1) NAND gate latch

→ As NAND gates are called as "Active Low" devices, i.e., it will be active only for low inputs.

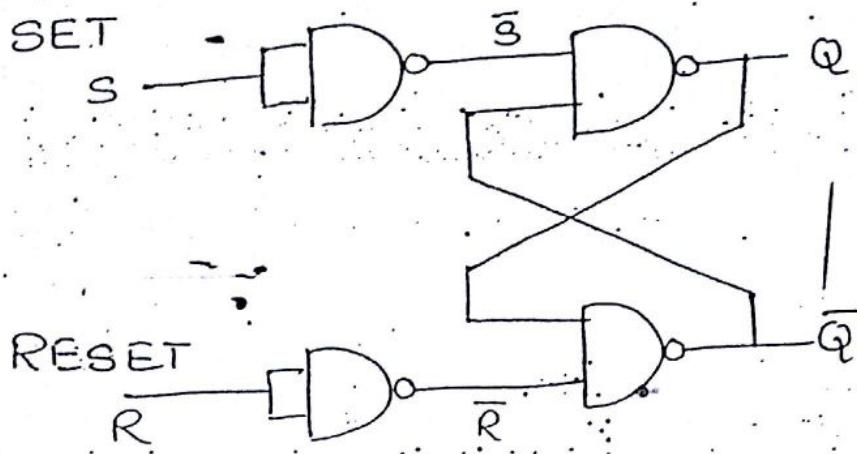


SR Latch

Latch constructed from two cross-coupled NAND Gates

The  $\bar{S}\bar{R}$ -latch is given as shown above.

→ The alternative diagram for  $\bar{S}\bar{R}$  latch can be constructed using true values of 'S' & 'R' as shown below & it is called as S.R. latch.



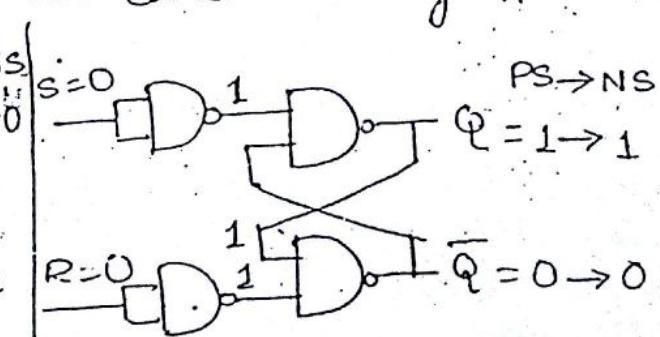
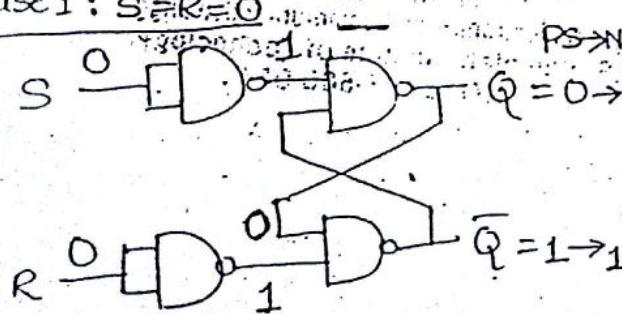
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### SR latch using NAND gates

Now let us see the working operation of SR latch using NAND gates.

→ Let us assume the previous O/p's are  $Q=0$  &  $\bar{Q}=1$ , Simultaneous will see for previous O/p's are  $Q=1$  &  $\bar{Q}=0$  for all combinations of i/p's.

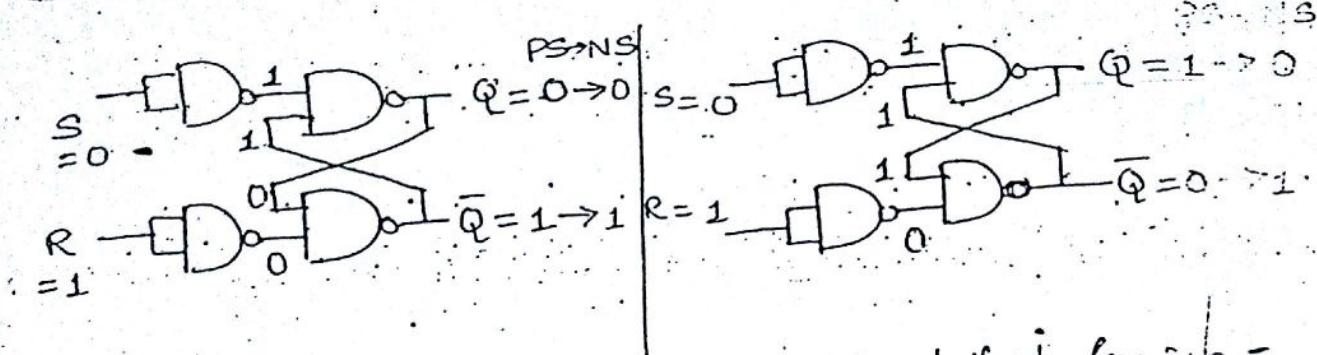
Case 1:  $S=R=0$



From the above diagrams, it is seen that for i/p combination:  $S=0$  &  $R=0$ , there is no change in the O/p's.

→ It means, it is storing the same value of previous O/p's.

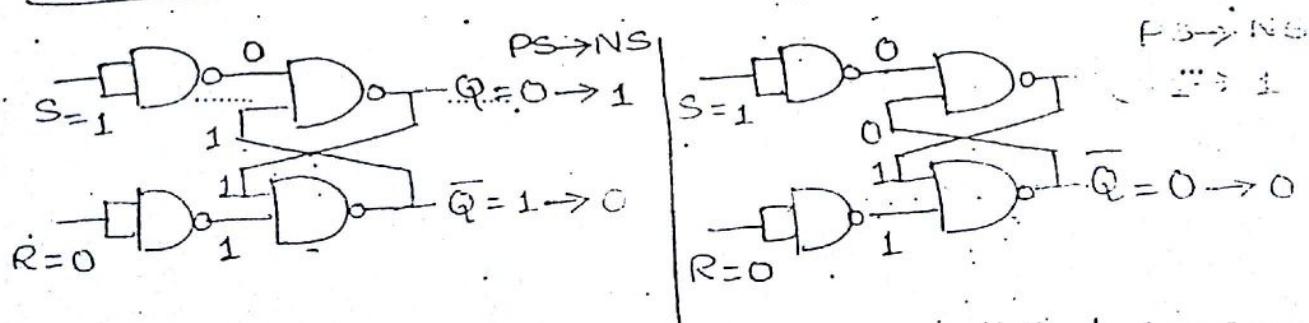
### Case 2: $S=0, R=1$ (Resetting Condition)



From the above diagrams, it is observed that for i/p combination  $S=0$  &  $R=1$  i.e., Resetting the system, if the normal o/p  $Q=0$  remains as  $Q=0$ , while if  $Q=1$  resets to  $Q=0$ . The latch is said to be reset state.

NOTE: for Resetting the latch, start from  $Q$

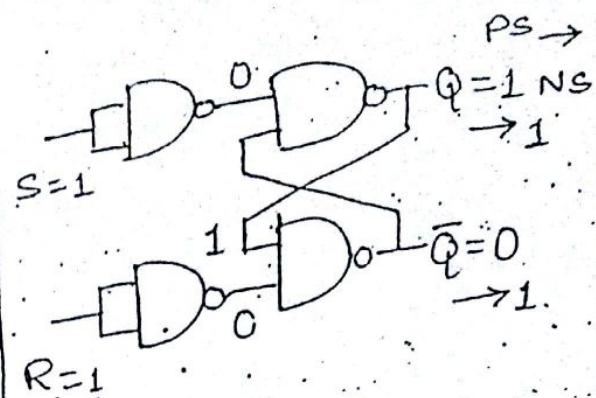
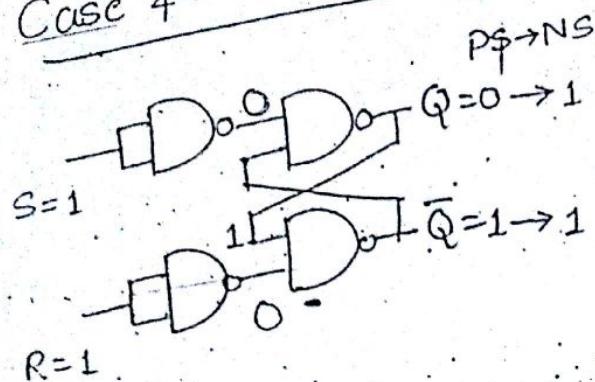
### Case 3: $S=1, R=0$ (Setting Condition)



From the above diagrams, it is observed that for i/p combination  $S=1$  &  $R=0$  i.e., Setting the system, if the normal o/p  $Q=0$  sets to  $Q=1$ , while if  $Q=1$  remains as  $Q=1$ . The latch is said to be in set state.

NOTE: for Setting the latch, start from  $\bar{Q}$

Case 4:  $S=R=1$



From the above diagrams, it is observed that for i/p combination  $S=R=1$ , the o/p's are no longer complements to each other i.e., both  $Q = \bar{Q} = 1$ , which is invalid or indeterminate.

→ All the observations made above for 4 cases are represented in truth table form shown below for SR NAND gate Latch.

S	R	Q	$\bar{Q}$	State
0	0	Q	$\bar{Q}$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	1	1	Invalid

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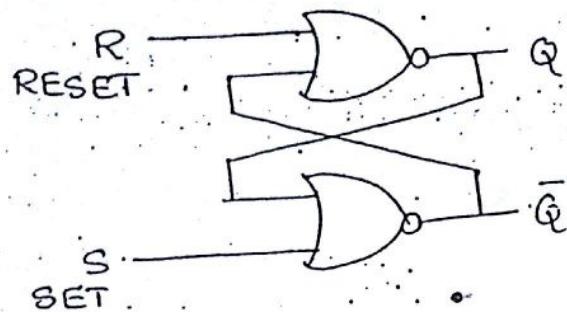
NOTE : 1) The notation  $PS \rightarrow NS$  means that a previous state o/p goes to next state when the i/p is applied.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

## 2) NOR gate latch.

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→ As NOR gates are called as Active High devices i.e., it will be active only for high i/p's.



NOR gate TT

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

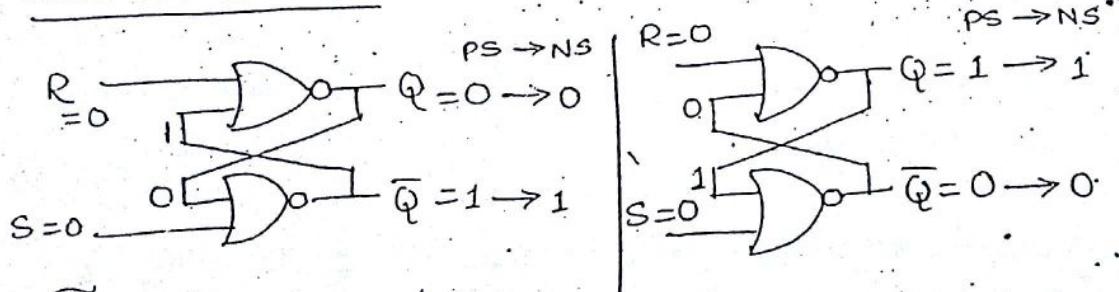
NOR gate latch is constructed from two cross-coupled NOR gates.

The RS latch is as shown above using NOR gates.

Now let us observe the working operation of RS latch using NOR gates.

→ Let us assume the previous o/p's as  $Q=0$  &  $\bar{Q}=1$ , simultaneously will observe for  $Q=1$  &  $\bar{Q}=0$  for all combinations of i/p's.

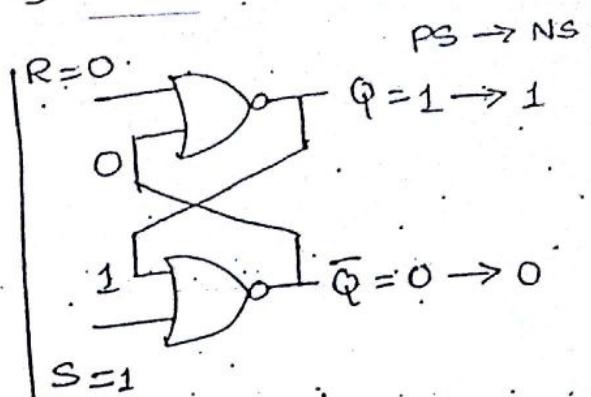
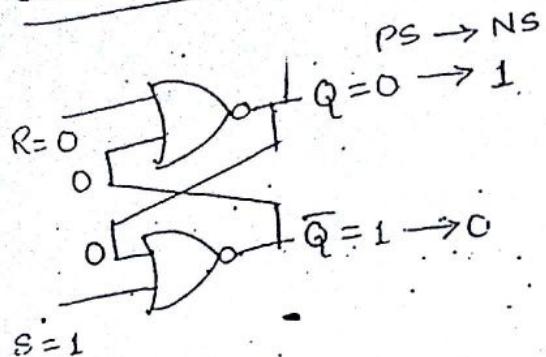
Case 1:  $R=S=0$



From the above diagrams, it is observed that for i/p combination  $S=R=0$ , there is NO change in the o/p's.

→ It means ; it is storing the same value of previous o/p's.

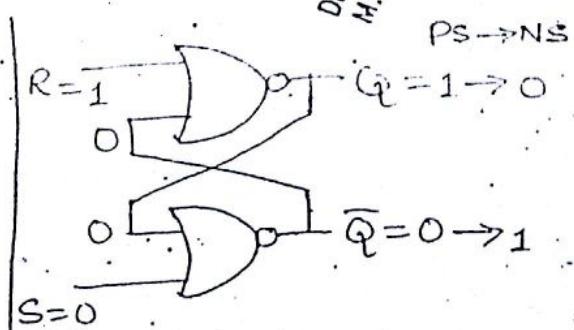
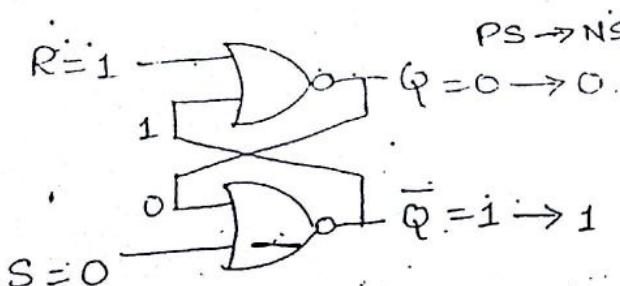
Case 2:  $R=0, S=1$  (Setting condition)



From the above diagrams, it is observed that for i/p combination  $R=0, S=1$  i.e., Setting the system, if the normal o/p  $Q=0$  set to  $Q=1$ , while if  $Q=1$  remains as  $Q=1$ . The latch is said to be in SET state.

NOTE: For setting the latch, start from  $Q$

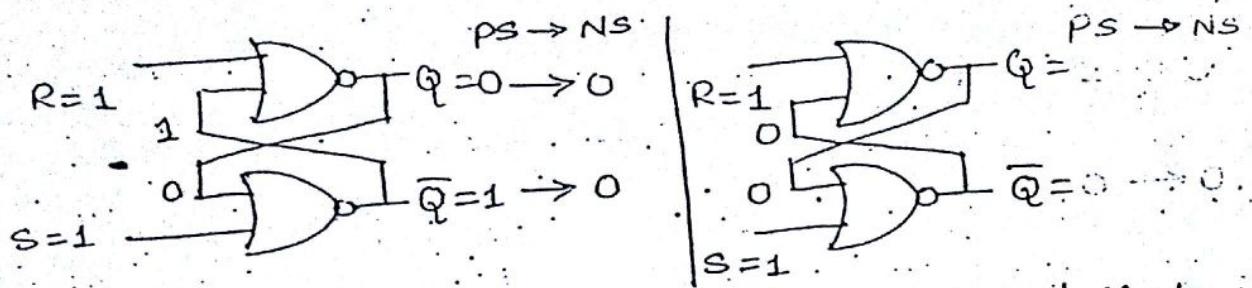
Case 3:  $R=1, S=0$  (Resetting Condition)



From the above diagrams, it is observed that for i/p combination  $R=1 & S=0$  i.e., Resetting the system, if the normal o/p  $Q=0$  remains as  $Q=0$ , while if  $Q=1$  resets to  $Q=0$ . The latch is said to be in RESET state.

NOTE: For resetting the latch, start from  $\bar{Q}$

Case 4:  $R=S=1$



From the above diagrams, it is observed that for typ combination  $R=S=1$ , the outputs are no complements to each other i.e., both  $Q=\bar{Q}=0$ , which is invalid or indeterminate.

→ All the observations made above for 4 are represented in truth table form shown for RS-NOR gate latch

R	S	$Q$	$\bar{Q}$	Status
0	0	$Q$	$\bar{Q}$	No change
0	1	1	0	SET
1	0	0	1	RESET
1	1	0	0	Invalid.

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### Applications of Flip-Flops

- It is used as a memory element
- In digital ckt's, FF's are used to eliminate key debounce.
- Counters & Registers are constructed using FF's.
- In digital logic, FF can be used as a delay element.

- Latches & Flip-Flops are the basic building blocks of most sequential circuits.
- The main difference between latches and FF's is in the method used for changing their state.
- We use the name LATCH for a sequential device that checks all of its inputs continuously and changes its outputs accordingly at any time independent of control signal called enable or clock signal.
- On the other hand, we use the name FLIP-FLOP for a sequential device that normally samples its inputs and changes its outputs only at times determined by control signal called enable or clock signal.

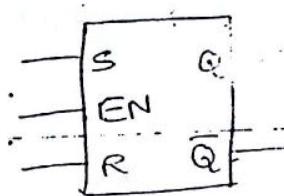
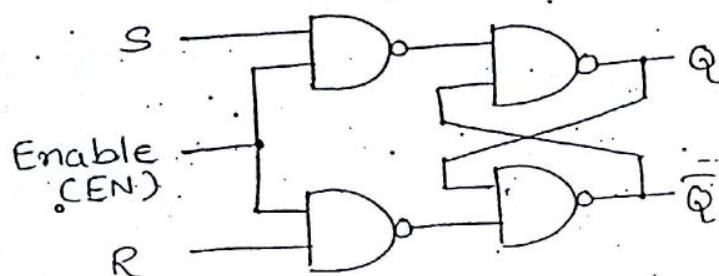
### The Gated SR Flip-Flop

- In the latches discussed so far, the o/p responds immediately to changes in the i/p.
- The inputs of these latches are said to be asynchronous.
- The SR Latch, we have seen, the latch is sensitive to its S & R inputs at all times.

→ However, it can easily be modified to create a Flip-Flop that is sensitive to these i/p's only when an enable i/p is active.

→ Inputs which cause a response only synchronous with an enable i/p are called Synchronous Inputs.

→ Such a latch with enable i/p is known as Gated SR Flip-Flop/Latch. It is shown below.



SR Latch with Enable i/p  
using NAND gates

Logic symbol

EN	S	R	Q	$\bar{Q}$	Status
1	0	0	Q	$\bar{Q}$	NO change
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	1	1	INVALID
0	X	X	Q	$\bar{Q}$	NO change

Truth Table

→ As shown by truth table, the circuit behaves like a SR Latch when EN=1, and retains its previous state when EN=0.

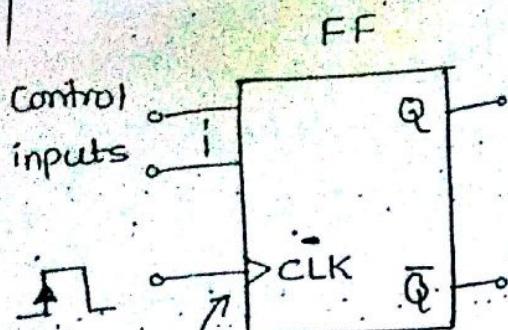
NOTE: When EN=1, it allows S & R values to enter into the ckt & gets o/p.

When EN=0, it stops S & R values to enter into the ckt & o/p will be the previous state o/p.

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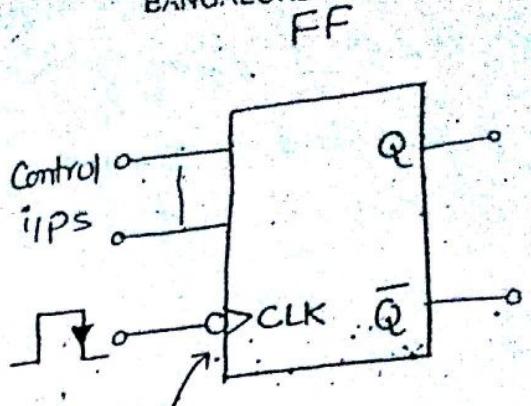
## Clocked Flip-Flops

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CLK is activated  
by a rising edge.

fig. (a)



CLK is activated by a  
falling edge

fig. (b)

The above figures (a) & (b) shows the logic symbols for a typical clocked FF.

→ As seen, a clocked FF has a clock i/p & some control i/p's.

CLK Input : Clocked FF's have a clock input that is labeled as CLK, CK or CP

→ In most clocked FF's, the CLK i/p is edge triggered. This means the CLK i/p is activated by a signal transition.

→ The edge-triggered activation is indicated by the presence of a small triangle on the CLK input.

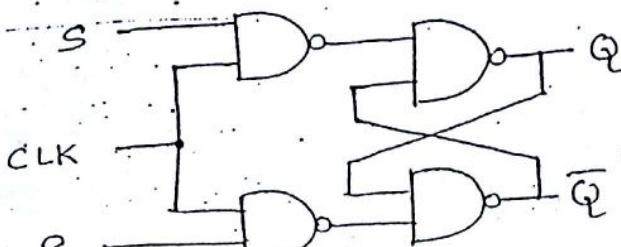
→ Fig (a) shows a FF with a small triangle on its CLK i/p to indicate that the i/p is activated only when a rising edge occurs.

→ Fig(b) shows a FF, which has a bubble (circle) as well as triangle on its CLK i/p. This signifies that CLK i/p is activated only when a falling edge occurs.

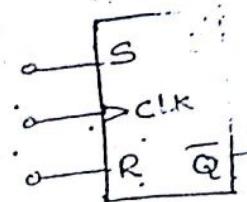
→ Control inputs can have various names depending on their operation. They are also called Input signals.

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### Clocked SR Flip-Flop



Clocked SR FF



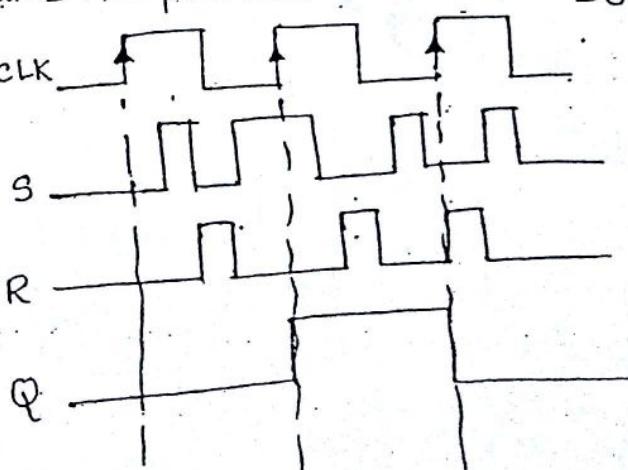
Logic Symbol

→ The circuit shown above is similar to gated SR FF/Latch except Enable signal is replaced by clock pulse/signal (CLK or CP).

→ On the positive edge of the clock signal/pulse, the circuit responds to the S & R inputs & behaves like a SR Latch, & retains its previous state when  $CLK = 0$ .

CLK	S	R	Q	$\bar{Q}$	Status
↑	0	0	0	1	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	1	1	Invalid
0	x	x	Q	$\bar{Q}$	No change

Truth Table



I/P & O/P waveforms

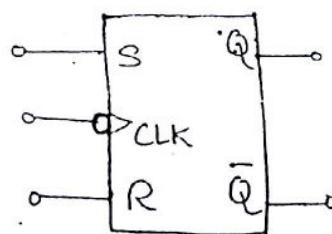
(↑) indicates rising edge of CLK i/p.

NOTE: In the above explanation, it is clearly observed that, the O/P is changing according to the i/p combinations, only at the rising edge of the CLK i/p signal; otherwise the FF retains its previous O/P state.

Therefore this is called: Positive Edge Triggered SR Flip-Flop / Latch.

→ Similarly, we have Negative Edge Triggered SR Flip-Flop / Latch.

→ In which, the O/P is changing according to the i/p combinations, only at the falling edge of the CLK i/p signal, otherwise the FF retains its previous O/P state. as shown below.



Logic Symbol.

CLK	S	R	Q	$\bar{Q}$	Status
↓	0	0	Q	$\bar{Q}$	No change
↓	0	1	0	1	Reset
↓	1	0	1	0	Set
↓	1	1	1	1	Invalid
1	x	x	Q	$\bar{Q}$	No change

Truth Table

(↓) indicates falling edge of clock.

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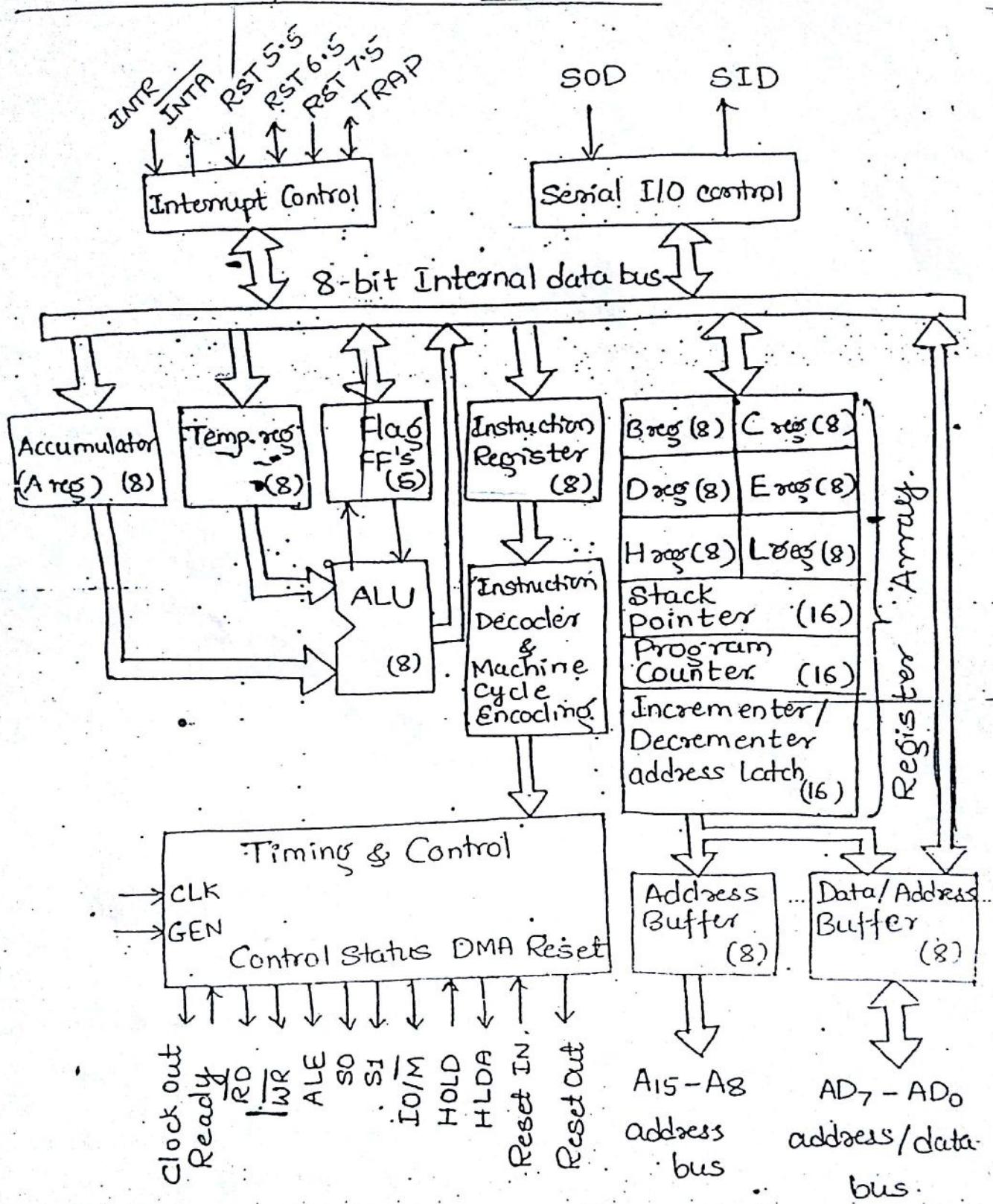
# Microprocessor & Microcontrollers

## Introduction to Microprocessor

- The microprocessor plays a significant role in everyday life where it can be used to control processes or to turn ON/OFF devices.
- The microprocessor is a programmable integrated device that has computing and decision-making capability similar to that of CPU of a computer.
- A microprocessor is a multi purpose, programmable, clock driven, register-based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to these instructions & provides as result.
- The physical components of a programmable machine or systems are called Hardware.
- A set of instructions written for a microprocessor or microcontroller to perform given task is called a Program, and a group of programs is called Software.
- The microprocessor applications are classified primarily into 2 categories are
  - 1) Reprogrammable Systems: possible to change set of instructions stored in memory and can perform any task assigned to system.
  - 2) Embedded Systems.
    - ↓
    - In this case, it is not possible to change set of instructions & embedded system is meant for particular application.

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# 8085 Microprocessor Architecture.



The 8085 Microprocessor Architecture is as shown above.

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## Control Unit:

- It generates signals within microprocessor to carry out the instruction, which has been decoded.
- In reality causes certain connections between the microprocessor to be opened or closed, so that control goes where it is required, and so that ALU operations occur.

## Arithmetic Logic Unit (ALU):

- The ALU performs the actual numerical and logic operation such as 'add', 'subtract', 'AND', 'OR' etc.
- Uses data from memory and from Accumulator to perform arithmetic. Always stores result of operation in Accumulator.

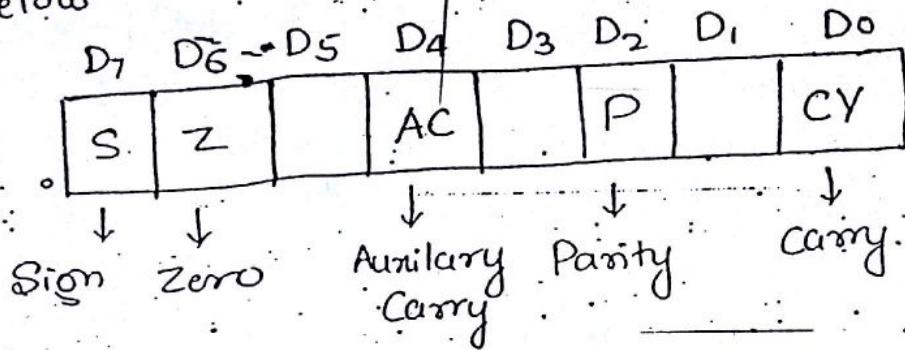
## Registers

- The 8085 programming model includes 6 registers, one accumulator and one flag register as shown above in fig.
- In addition, it has two 16-bit registers: the stack pointer and the program counter.
- 6 general purpose registers to store 8-bit data; these are identified as B, C, D, E, H & L as shown in fig.
- They can be combined as register pairs like BC, DE & HL - to perform some 16-bit operations.
- Accumulator is an 8-bit register that is a part of ALU. This is used to store 8-bit data and to perform arithmetic & logic operations.
- The result of an operation is stored in an accumulator.

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→ The ALU includes 5 flip-flops, which are set or reset after an operation according to the data conditions of the result in the accumulator and other registers. They are called Zero (Z), Carry (CY), Sign (S), Parity (P) & Auxiliary Carry (AC) flags.

→ Their bit positions in the flag register are shown below.



### Program Counter (PC)

- It is 16-bit register deals with sequencing the execution of instructions. This register is a memory pointer.
- The function of PC is to point to the memory address from which the next byte is to be fetched.
- When a byte is being fetched, the PC is incremented by one to point to the next memory location.

### Stack Pointer (SP)

- It is also a 16-bit register used as a memory pointer.
- It points to a memory location in R/W memory, called the Stack.

## Instruction Register / Decoder.

- Temporary store for the current instruction of a program.
- Latest instruction sent here from memory prior to execution..
- Decoder then takes instruction and decodes, or interprets the instruction.
- Decoded instruction then passed to next stage

## 8085 System Bus.

- Typical system uses a no. of buses, collection wires; which transmit binary nos., one bit per wire.
- A typical microprocessor communicates with memory and other devices using 3 buses: Address Bus, Data Bus & Control Bus.

- ### Data Bus & Control Bus.
- Address Bus consists of 16 wires; therefore 16 bits ie; one wire for each bit.
  - Data Bus carries 'data' in binary form, between microprocessor & other external units such as memory. Typical size is 8 or 16 bits.
  - Control Bus are various lines which have specific functions for co-ordinating and controlling microprocessor operations.

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# 8085 Pin Description

$x_1$	1.	40	VCC
$x_2$	2	39	HOLD
Reset Out	3	38	HLDA
SOD	4	31	CLK(OUT)
SID	5	86	Reset In
TRAP	6	35	Ready
RST 7.5	7	34	E0/M
RST 6.5	8	33	S.L
RST 5.5	9	32	RD
INTR	10	31	WR
INTA	11	30	ALE
AD0	12	29	SO
AD1	13	28	A15
AD2	14	27	A14
AD3	15	26	A13
AD4	16	25	A12
AD5	17	24	A11
AD6	18	23	A10
AD7	19	22	A9
Vss	20	21	A8

8085

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## Working of Microprocessor

- A program is a sequence of instructions written to perform specific function.
- The instructions are selected from the instruction set of a microprocessor.
- When the microprocessor is given a command to execute the program, it reads and executes one instruction at a time and finally sends the result to the 7-segment LED's for the display.

→ Let us consider a simple example, adding two hexa decimal numbers 32H & 48H.

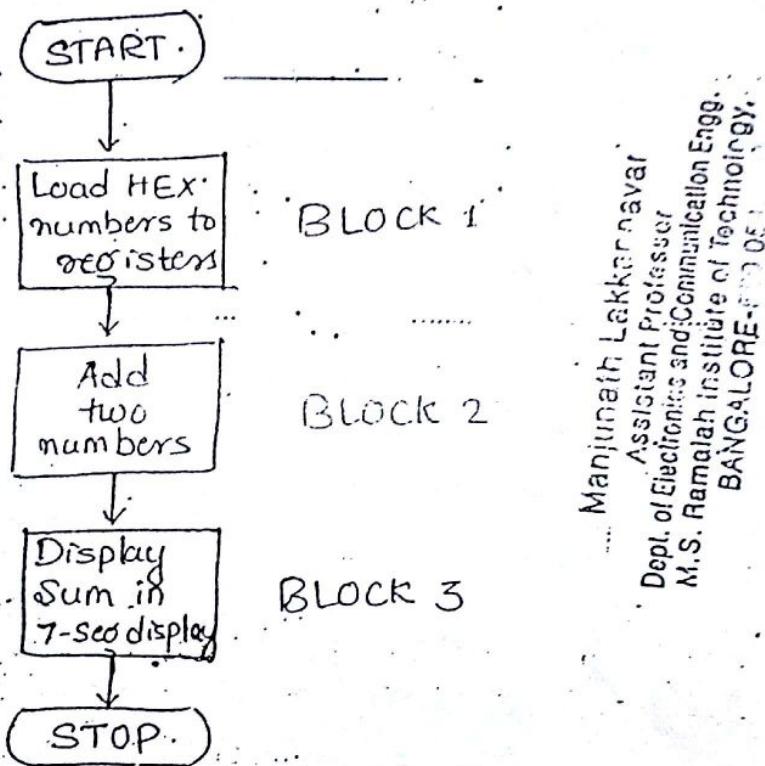
→ To add the above two no.s, the following procedure is to be followed.

1) Load the numbers into the registers.

2) Add the numbers.

3) Display the sum at the O/P port 1.

The above procedure can be represented in flowchart as shown below.



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BLOCK 1: MVI A, 32H → Load 'A' with 32H.

MVI B, 48H → Load 'B' with 48H

BLOCK 2: ADD B → Add content of 'B' with 'A'

& sum is stored in 'A'

BLOCK 3: OUT 01H → Display accumulator content at port 01H

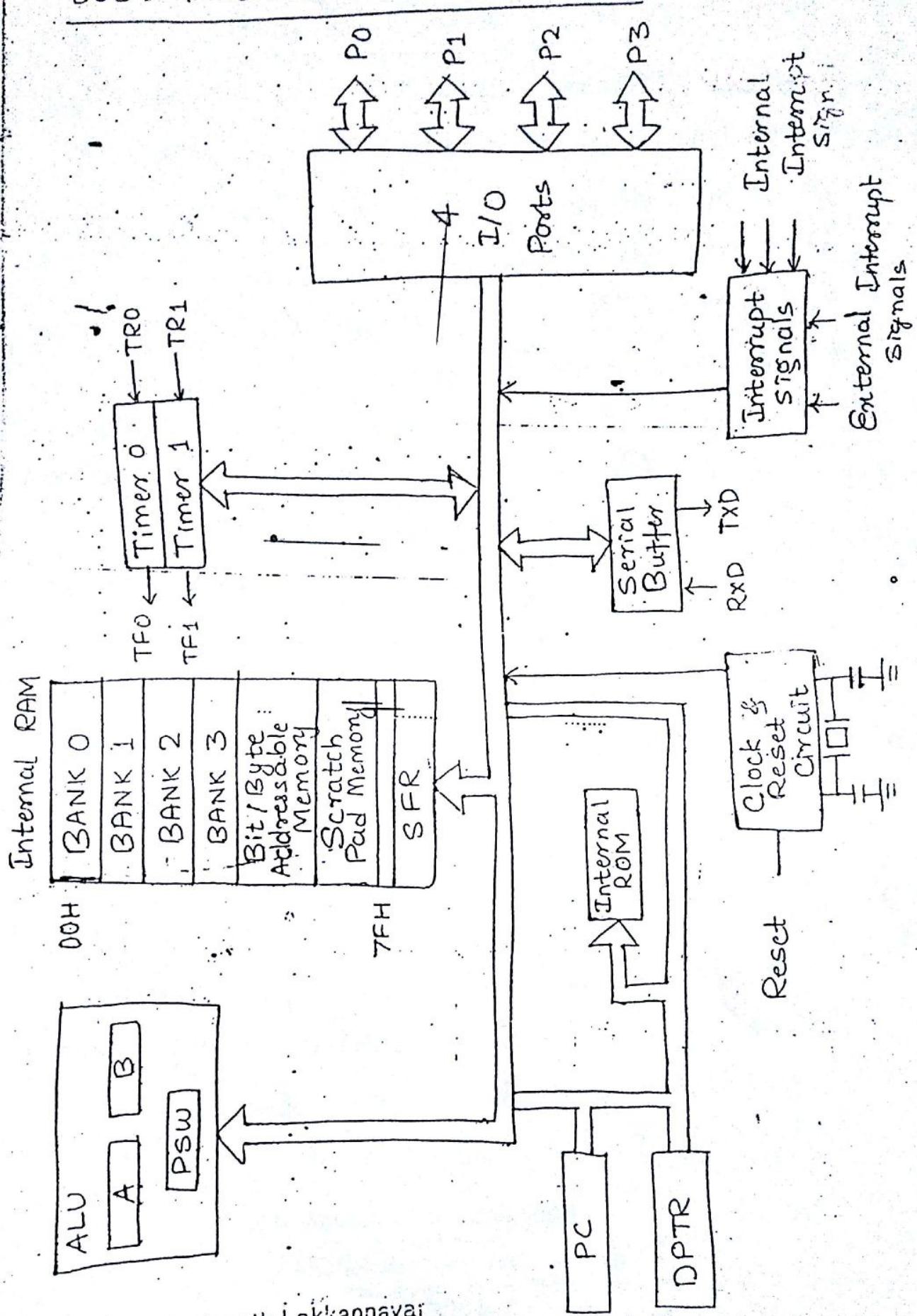
HLT → END.

## Introduction to Microcontroller

- A typical microcontroller, which is a true computer on a chip
- The design incorporates all of the features found in a microprocessor CPU: ALU, PC, SP and registers.
- It also has added the other features needed to make a complete computer: ROM, RAM, parallel I/O, serial I/O, counters and a clock circuit.
- Like the microprocessor, a microcontroller is a general purpose device, but one that is meant to read data, perform limited calculations on that data, and control its environment based on those calculations.
- The prime use of a microcontroller is to control the operation of a machine using a fixed program that is stored in ROM and that does not change over the lifetime of the system.
- Microcontroller can be classified on the basis of their bits processed like 8 bit MC, 16 bit MC.

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# 8051 Microcontroller Architecture.



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→ 8-bit Microcontroller called 8051 is as shown above.

→ The main features of 8051 is as follows.

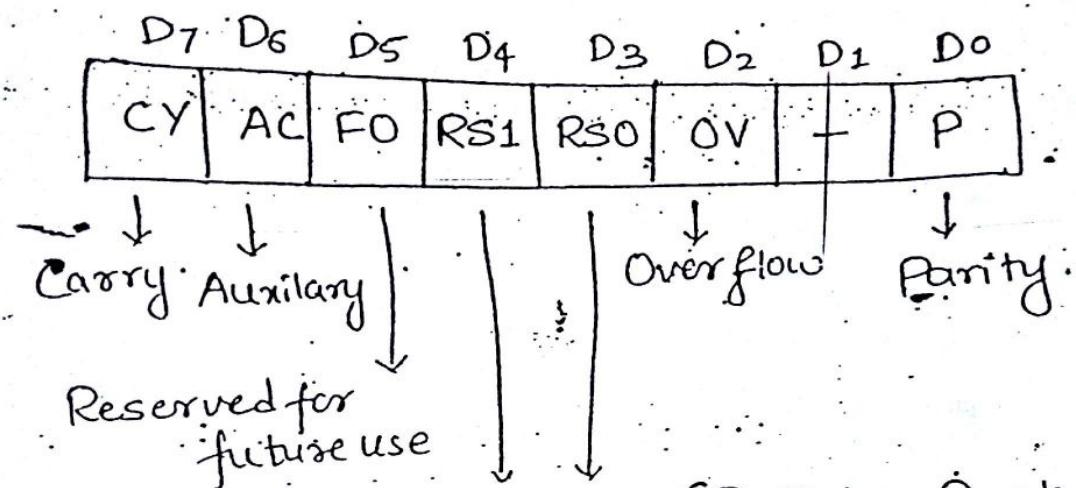
- 1) 8-bit CPU with registers A & B, both are 8 bits
- 2) 16 bit Program Counter & Data Pointer (DPTR).
- 3) 8 bit Program Status Word (PSW.)
- 4) 8 bit Stack Pointer (SP)
- 5) Internal ROM of 4KB and RAM of 128 bytes.
- 6) Internal RAM of 128 bytes is divided into
  - a) 4 register banks, each containing 8 reg's.
  - b) 16 bytes of memory which is bit addressable
  - c) 80 bytes of scratch pad memory.
- 7) 32 I/O pins arranged as 4 8-bit ports P0-P3.
- 8) Two 16-bit Timer/Counters T0 & T1
- 9) Full duplex serial data receiver/transmitter.
- 10) Control Registers : TCON (Timer Control)  
                        TMOD (Timer Mode)  
                        SCON (Serial Control)  
                        PCON (Power Control)  
                        IP (Interrupt Priority)  
                        IE (Interrupt Enable)

- ii) Two external & Three internal interrupt sources
- 12) Oscillator & clock.
- 13) Special Function Registers (SFR).

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## Flag Register

Flags are 1-bit registers provided to store results of instruction.



RS<sub>1</sub> RS<sub>0</sub> (Register Bank Select bits)

0 0 → Select Bank 0.

0 1 → Select Bank 1

1 0 → Select Bank 2

1 1 → Select Bank 3.

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