# 1. Hardware architecture

## Key features

Low supply-voltage range: 1.8 – 3.6 V

Ultra-low lower consumption

* Active mode 230uA at 1 MHz, 2.2 V
* Standby Mode 0.5 uA
* Off Mode (RAM retention) 0.1 uA

Five power-saving modes

Ultra-fast wake up from standby mode in less than 1 ms

16 bit RIS architecture, 62.5 ns Instruction Cycle Time

Basic clock module configuration

* Internal Frequencies up to 16 MHZ with four Calibrated Frequency
* Internal very-low-power low-frequency oscillator
* 32 kHz Crystal
* External Digital clock source

Two 16-Bit timer\_A with Three capture/compare resgister

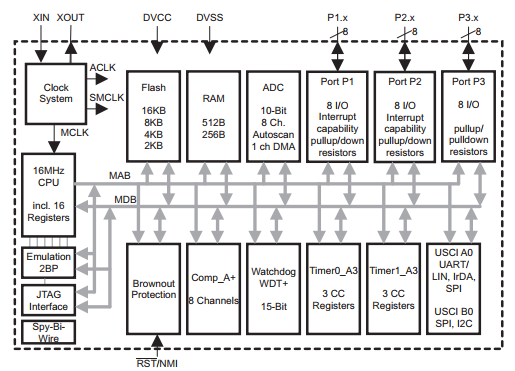
Up to 24 touch-sense-enable I/O Pins

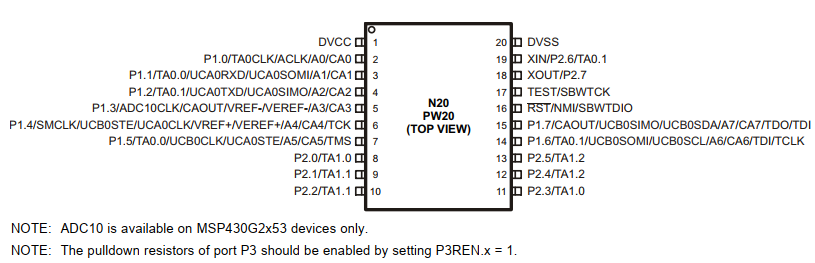
Universal Serial Communication Interface (USCI)

* Enhanced UART supporting Auto Baudrate Detection (LIN)
* IrDA encoder and decoder
* Synchronous SPI
* I2C

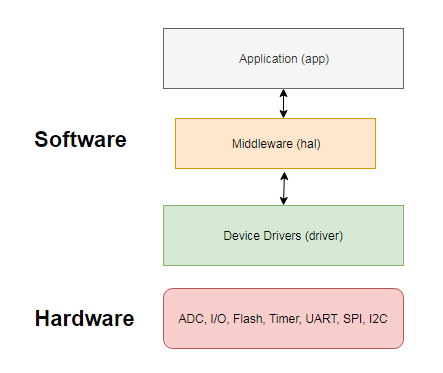
On-Chip comparators for Analog digital compare function and slope analog-to-digital conversion

10-Bit 200-ksps Analog-to-Digital Converter with internal reference, sample-and-hold and autoscan

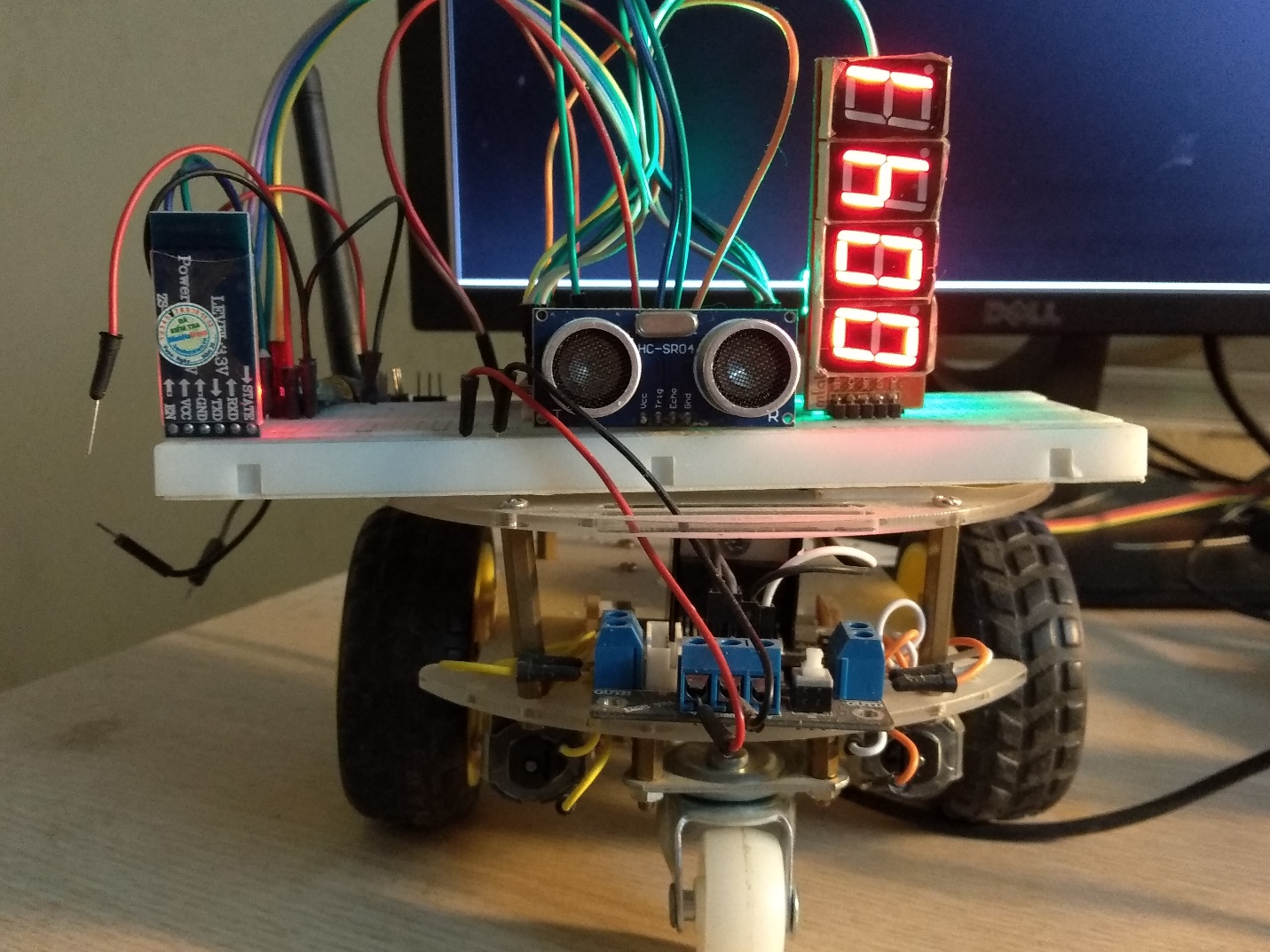




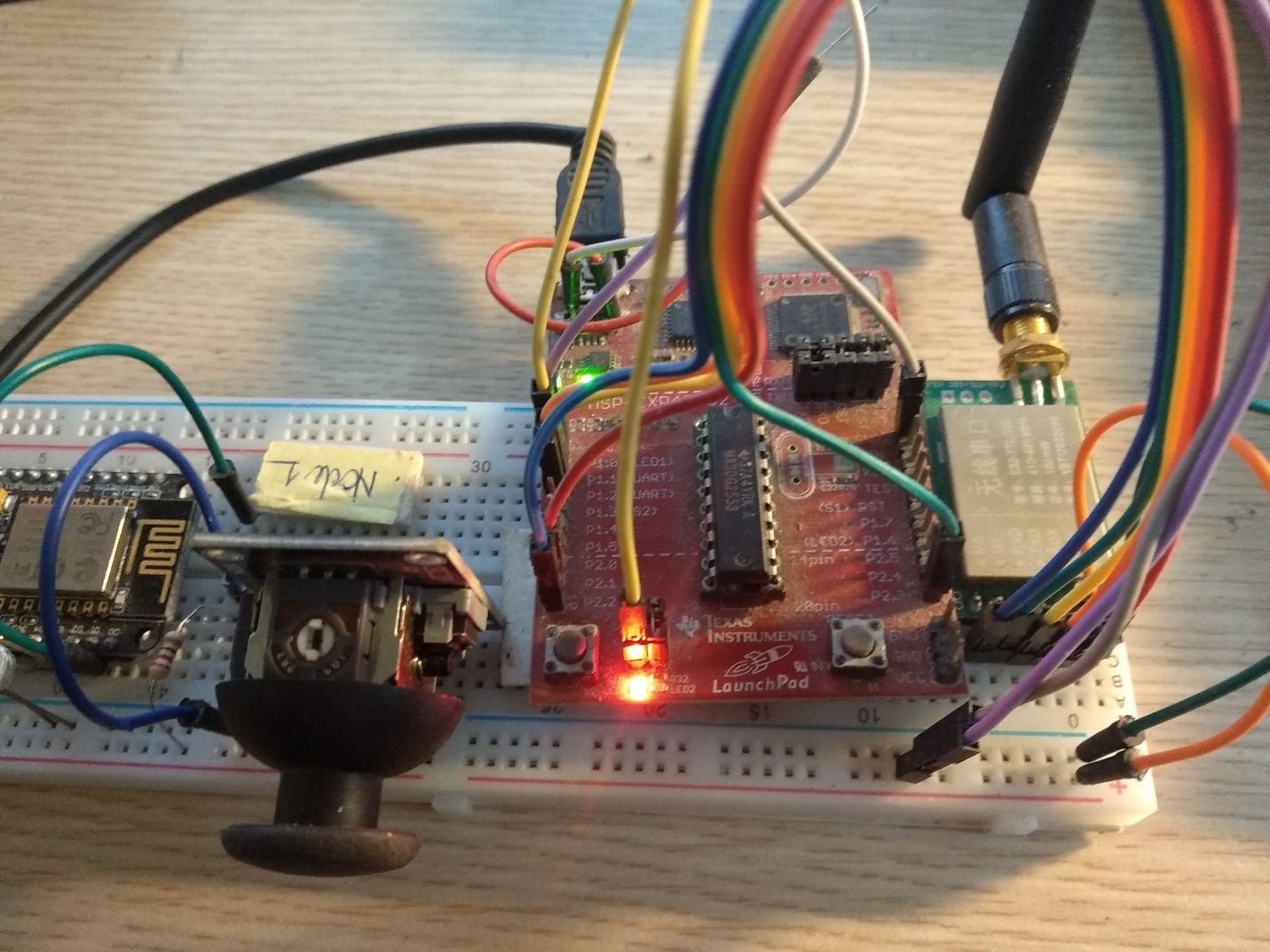
# 2. Software architecture



Result:



Master Board



Slave Board