GIC600AE¹ Fault Management Unit (FMU)

Jimmy Brisson

July 30, 2020

Overview

Differences with GIC600

New Registers Global Error Records

TF-A Impact
RAS & SDEI
Testing
Options & Challenges

Differences with GIC600

- ► GIC features compatible with GIC600
- Unit to collect errors (FMU)
- Duplicated logic in GIC structures
- ECC in RAMs
- Store correctable and uncorrectable errors
- Dedicated bus for error reporting

FMU Registers

Offset	Width	Description
$0 \times 000 + 64n$	4×u64	Error Records, Details on next slide
0×E00	u64	Error Present, 1 bit for each record
0×EA0	u32	Lock, writing key enables a write
0xEB4	u32	Safety Mechanism Enable, on at boot
0×EC0	u32	Error Injection
0×F00	u32	FMU Idle Status
0×FC8	u32	Number of Error Records

FMU Error Records

Offset	Width	Description
0x00	u64	Present: Fault & Recovery Interrupts & Logging
0×08	u64	Control: Fault & Recovery Interrupts & Logging
0×10	u64	Status: Valid, Code, Overflow, Correctable etc.
0×18	u64	Unspecified: Probably Read as Zero

RAS & SDEI Integration

- Define a dispatcher for the GIC600AE FMU
- ► Encode Error records as SDEI_EXPLICIT_EVENT
- Dispatch Correctable errors through SDEI
- ► Panic on Uncorrectable errors

TFTF Testing

For each error type

- ► Register with SDEI
- Cause an interrupt w/ Error Injection Reg
- Handle Error by setting flag
- Assert flag was set

Implementation Options & Challenges

- Correctable Errors
 - ► Treat as Uncorrectable?
 - Dispatch every?
 - Dispatch on overflow?
- ► Report Uncorrectable Errors to BMC/SCP?
- Disable Safety Mechanism before enable interrupts?