1)

Q1.1

Mem 2MB = 2^21
Cache size = 64*32 = 2^11
Block size = 32
Offset: 32 bytes (each block) = 2^5
Line: 64 in cache 2^6
Tag: 21- 5 - 6 = 10

Tag = 10 bit. Line = 6 bit. Offset = 5 bit.

Q1.2

000 10 0100 0111 010011 00011

tag: 0x 247

line: 0x 13

offset: 0x 03

Q2.1

Offset 32 = 2^5
Tag 21-5 = 16 bit

Tag = 16bits, Offset = 5 bits

Q2.2

000 1001 0001 110 10011 00011

Tag: 0x 91D3
Offset: 0x 03

Q3.1

Tag = 12bits, Set = 4bits, Offset = 5bits

Q3.2

Tag: 0x 91D
Set: 0x 3
Offset: 0x 03

2)

Q1.1

Memory address	Tag	Row	Offset	
	4 bits	2 bits	2 bits	
91	1001	00	01	miss
A8	1010	10	00	miss
A9	1010	10	01	hit
AB	1010	10	11	hit
AD	1010	11	01	miss
93	1001	00	11	hit
6E	0110	11	10	miss
B9	1011	10	01	miss
17	0001	01	11	hit
E2	1110	00	10	miss
4E	0100	11	10	miss
4F	0100	11	11	hit
50	0101	00	00	miss
A4	1010	01	00	miss

hits/ total mem *100%

5 Hits / 14 Total memory x 100% = 35.71%

Q1.2

Tag (binary)	Block #	offset 0	offset 1	offset 2	offset 3
0101	0	**50**	51	52	53
1010	1	**A4**	A5	A6	A7
1011	2	B8	**B9**	BA	BB

0100	3	4C	4D	4E	**4F**

3)

Q1.1

Virtual 256K
Physical 128K

Virtual Address: log2(256 * 1024) = 18 bits

Each Page is 32K bytes, so page offset is: log2(32*1024)=15 bits.

Virtual address: 18−15 = 3 bits

Physical Address: (log2(128 * 1024) = 17 bits) = 17 bits

With same page size Physical address: 17−15 = 2 bits for addressing.

Q1.2

Tag: 128/2 = 64 = 2^6
Or, 6 bits

Row: 2/256 = 8 = 2^3
Or, 3 bits

Offset: 256 = 2^8
Or, 8 bits

Q1.3

It is a Page fault because the virtual address 0x32764 is outside the scope of the mapping provided in the TLB/Page Table entries.
No direct mapping for this address is given so, we need a procedure to handle the page fault.

Virtual address:
110 **|** 010 0111 0110 0100
Page 110 is page 6, where no physical page in page table is available for virtual page 6.

Q2.1

TLB	Virtual page #	Physical page #	Valid
	6	1	1
	0	2	1

TLB LRU stack

6
0

Page Table

Virtual page #	Physical page #	Valid
0	2	1
1	-	0
2	-	0
3	-	0

4	0	1
5	3	1
6	1	1
7	-	0

Mem LRU stack

6
0
5
4

3)

Q1.1

Cache

Line #	Tag	Data
0	10	*
1	0A	*

2	3C	*
3	14	*
4	28	*
5	04	*
6	37	*
7	13	*

The cache is the same as the address was a TLB hit.