改进RISC-V的代码生成

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自我介绍

- Phabricator https://reviews.llvm.org/p/liaolucy/
- github https://github.com/ChunyuLiao

简介

- 仓库：https://github.com/llvm/llvm-project
- review代码：https://reviews.llvm.org
- 各种讨论/通知：https://llvm.discourse.group
- 手册：https://llvm.org/docs/DeveloperPolicy.html
- 针对RISCV的代码实现：
  https://github.com/llvm/llvm-project/tree/main/llvm/lib/Target/RISCV

简介

- 针对RISCV的代码实现：
  https://github.com/llvm/llvm-project/tree/main/llvm/lib/Target/RISCV

```
AsmParser                          RISCVInstrFormatsV.td              RISCVInstrInfoZicbo.td             RISCVRegisterInfo.h
CMakeLists.txt                     RISCVInstrInfoA.td                 RISCVInstrInfoZicond.td            RISCVRegisterInfo.td
Disassembler                       RISCVInstrInfo.cpp                 RISCVInstrInfoZihintntl.td         RISCVRVVInitUndef.cpp
GISel                              RISCVInstrInfoC.td                 RISCVInstrInfoZk.td                RISCVSchedRocket.td
MCA                                RISCVInstrInfoD.td                 RISCVInstrInfoZvk.td               RISCVSchedSiFive7.td
MCTargetDesc                       RISCVInstrInfoF.td                 RISCVISelDAGToDAG.cpp              RISCVSchedSyntacoreSCR1.td
RISCVAsmPrinter.cpp                RISCVInstrInfo.h                   RISCVISelDAGToDAG.h                RISCVSchedule.td
RISCVCallingConv.td                RISCVInstrInfoM.td                 RISCVISelLowering.cpp              RISCVScheduleV.td
RISCVCodeGenPrepare.cpp            RISCVInstrInfo.td                  RISCVISelLowering.h                RISCVScheduleZb.td
RISCVExpandAtomicPseudoInsts.cpp   RISCVInstrInfoVPseudos.td          RISCVMachineFunctionInfo.cpp       RISCVSubtarget.cpp
RISCVExpandPseudoInsts.cpp         RISCVInstrInfoVSDPatterns.td       RISCVMachineFunctionInfo.h         RISCVSubtarget.h
RISCVFeatures.td                   RISCVInstrInfoV.td                 RISCVMacroFusion.cpp               RISCVSystemOperands.td
RISCVFrameLowering.cpp             RISCVInstrInfoVVLPatterns.td       RISCVMacroFusion.h                 RISCVTargetMachine.cpp
RISCVFrameLowering.h               RISCVInstrInfoXSf.td               RISCVMakeCompressible.cpp          RISCVTargetMachine.h
RISCVGatherScatterLowering.cpp     RISCVInstrInfoXTHead.td            RISCVMCInstLower.cpp               RISCVTargetObjectFile.cpp
RISCV.h                            RISCVInstrInfoXVentana.td          RISCVMergeBaseOffset.cpp           RISCVTargetObjectFile.h
RISCVInsertNTLHInsts.cpp           RISCVInstrInfoZb.td                RISCVOptWInstrs.cpp                RISCVTargetTransformInfo.cpp
RISCVInsertVSETVLI.cpp             RISCVInstrInfoZc.td                RISCVProcessors.td                 RISCVTargetTransformInfo.h
RISCVInstrFormatsC.td              RISCVInstrInfoZfa.td               RISCVRedundantCopyElimination.cpp  RISCV.td
RISCVInstrFormats.td               RISCVInstrInfoZfh.td               RISCVRegisterInfo.cpp              TargetInfo
```

概述

- 个人发现的改进机会
- Craig Topper, RISC-V Sign Extension Optimizations
- 开发过程中遇到的一些问题/故事

改进机会

- 主要集中在指令选择和指令生成阶段
- 更好的使用RISCV ISA 和 psABI 规范
- 对比借鉴gcc的优化

尽量使用0比较

- RISCV有针对0比较的特殊指令
  - beqz/bnez, It expands to beq rs1, x0, offset.
  - seqz/snez, SLTIU rd, rs1, 1 sets rd to 1 if rs1 equals zero, otherwise sets rd to 0 (assembler pseudoinstruction SEQZ rd, rs).

- [RISCV] Enable preferZeroCompareBranch to optimize branch on zero in codegenprepare : https://reviews.llvm.org/D142071

imm立即数优化

- [RISCV]Preserve (and X, 0xffff) in targetShrinkDemandedConstant
  https://reviews.llvm.org/D134155

- 对比 https://llvm.godbolt.org/z/d1a9oTGcM

减少分支指令数

- [RISCV] Branchless lowering for (select (x < 0), TrueConstant, FalseConstant) and (select (x >= 0), TrueConstant, FalseConstant) https://reviews.llvm.org/D137949
- [RISCV]Keep (select c, 0/-1, X) during PerformDAGCombine https://reviews.llvm.org/D139272

- 对比：https://llvm.godbolt.org/z/rYezq7743

tail-call 优化

- RISCV psABI https://github.com/riscv-non-isa/riscv-elf-psabi-doc
- [RISCV] Permit tail call to an externally-defined function with weak linkage https://reviews.llvm.org/D143137

- 推荐大佬们的blog, 比如MaskRay的blog https://maskray.me https://maskray.me/blog/2021-04-25-weak-symbol

钩子函数

- [RISCV]Enable isIntDivCheap when attribute is minsize
  https://reviews.llvm.org/D130543
- [RISCV] Return false from shouldFormOverflowOp when type is i8 and i16
  https://reviews.llvm.org/D143646

- 对比：https://llvm.godbolt.org/z/c5Toh6TEa

常见/其他架构已有优化

- [RISCV] Add more patterns for FNMADD https://reviews.llvm.org/D126852
- [RISCV] Optimize 2x SELECT for floating-point types
- https://reviews.llvm.org/D127871

针对RV32的优化

- [LegalizeTypes][RISCV] Add a special case for (add X, -1) to ExpandIntRes_ADDSUB https://reviews.llvm.org/D146635

捡漏

- [RISCV] Use hasAllWUsers to recover XORI/ORI
  https://reviews.llvm.org/D135538

RISC-V Sign Extension Optimizations

- https://llvm.org/devmtg/2022-11/slides/TechTalk21-RISC-VSignExtensionOptimizations.pdf

开发过程中遇到的一些问题/故事

- 兼顾不同架构
  - [SelectionDAG][RISCV][X86][AArch64][AMDGPU][PowerPC] Improve SimplifyDemandedBits for SHL with NUW/NSW flags. https://reviews.llvm.org/D140665
- 兼顾不同模块
  - [CodeGenPrepare][RISCV] Reverse transform in CGP to use zero-compare branch https://reviews.llvm.org/D147789
- 兼顾不同的代码形似
  - [DAGCombiner][VP] Add DAGCombine for VP_MUL. https://reviews.llvm.org/D121187

开发过程中遇到的一些问题/故事

- 虽然有一些困难，但是也有很大收获
- 大佬与我们同在

- [LegalizeTypes][RISCV] Add a special case to ExpandIntRes_UADDSUBO for (uaddo X, 1). https://reviews.llvm.org/D144614

欢迎交流，一起发掘更多优化机会