高等數位積體電路設計 Final Project

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一、 規格

	Parameter	RTL	Mix-Signal
1	Target Process	NaN	L18U18V_TT
2	Reference Clock(MHz)	79.36MHz~555.56MHz	
3	Programmable Input and Feedback Divider	M=1~7	
4	Output Clock(MHz)	理論 555.56MHz	
	Output Clock mean(ns)	554.27	556.213
	Output Clock RMS(ns)	554.69	556.615
5	Lock-in Time(# cycle)	89 Cycle	89 Cycle
6	Jitter		
	Period jitter mean(ns)	0.007	0.00054
	Period jitter RMS(ns)	0.073	0.07
	Cycle-to-Cycle jitter mean(ns)	-0.0002	0.00005
	Cycle-to-Cycle jitter RMS(ns)	0.0099	0.003
	N-Cycle jitter mean(ns)	48.4	44.45
	N-Cycle jitter RMS(ns)	48.74	45.06
7	Output Phase Drift(ns)	0.06ns	0.06ns
8	Max Power Consumption(mW)	NaN	24.6mW
9	Average Power Consumption(mW)	NaN	6.47mW

二、 路徑

Demo1：

```
cad1 [adic19/lab04c(PLL)]%
```

Demo2：

```
cad19 [adic19/lab06d(PLL)]%
```

Demo1 數據：

```
cad1 [adic19/lab04c(PLL)]% /data.csv
```

Demo2 數據：

```
cad19 [adic19/lab06d(PLL)]% /data.csv
```

後面的數據圖都是從 freq_lock 之後才開始畫

三、 Demo1 – Ncverilog RTL

用 NcVerilog 跑 RTL 確定電路是否做動，之後確認各項數據是否正確。

Demo1 的 Output Clock(MHz)：

Output Clock mean: 554.2724258277233

Output Clock RMS: 554.6933742750609

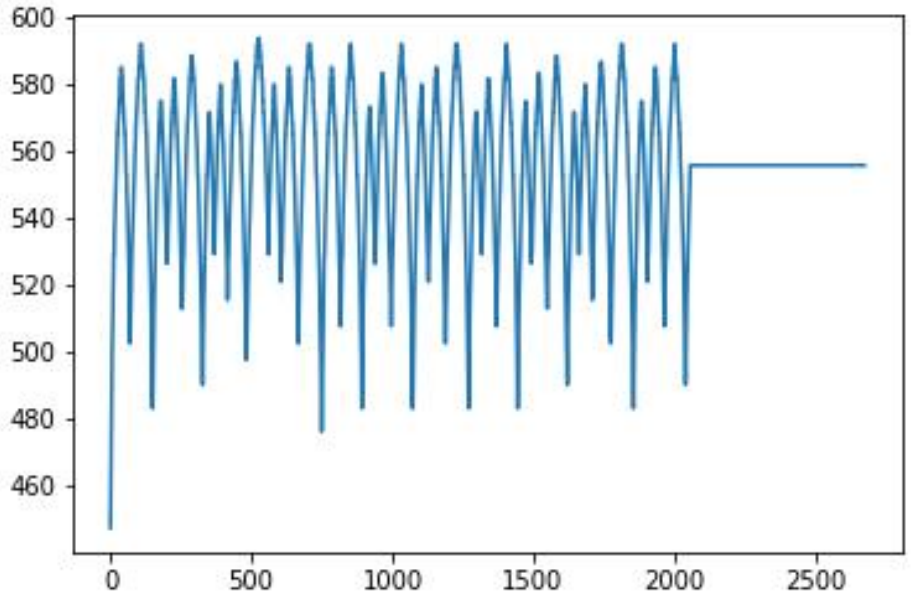

圖 1 Demo1 的 Output Clock

Demo1 的 Period jitter(ns)：

Period jitter mean: 0.007014200298952932

Period jitter RMS: 0.07351494362185784

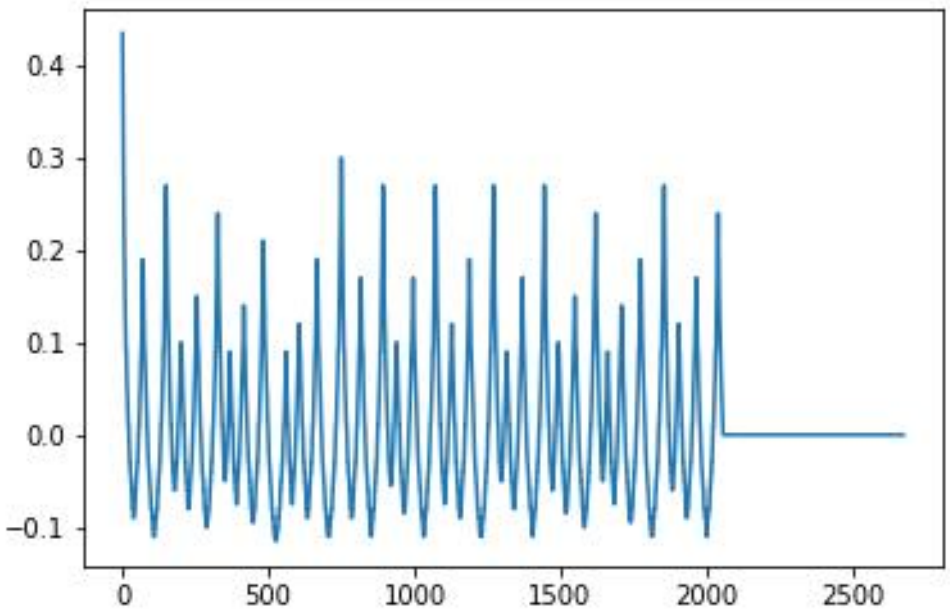

圖 2 Demo1 的 Period jitter

Demo1 的 Cycle-to-Cycle jitter(ns)：

Cycle-to-Cycle jitter mean: -0.00019431988042007423

Cycle-to-Cycle jitter RMS: 0.009919330827518962

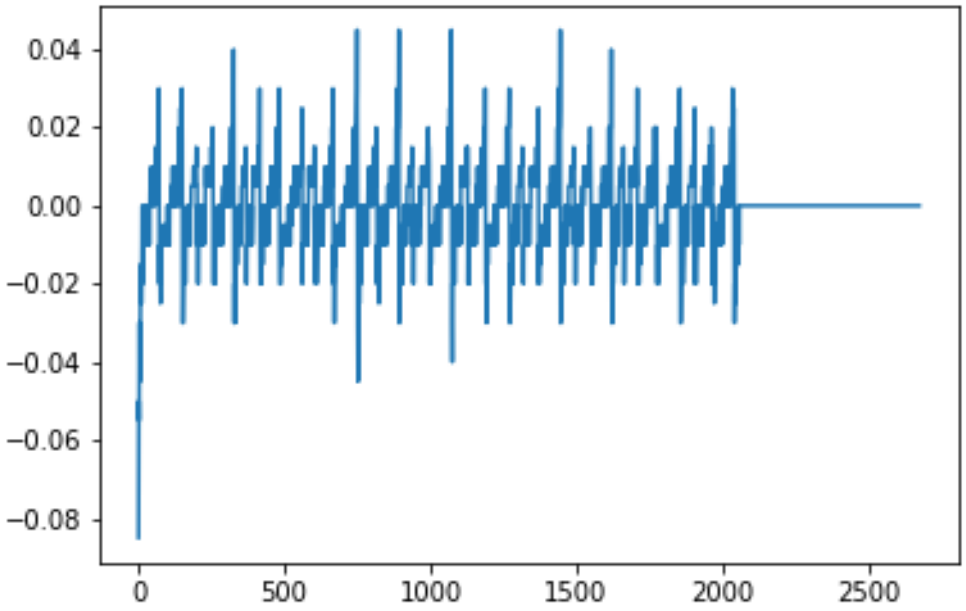

圖 3 Demo1 的 Cycle-to-Cycle jitter

Demo1 的 N-Cycle jitter(ns)：

N-Cycle jitter mean: 48.40111733931173

N-Cycle jitter RMS: 48.74551944474464

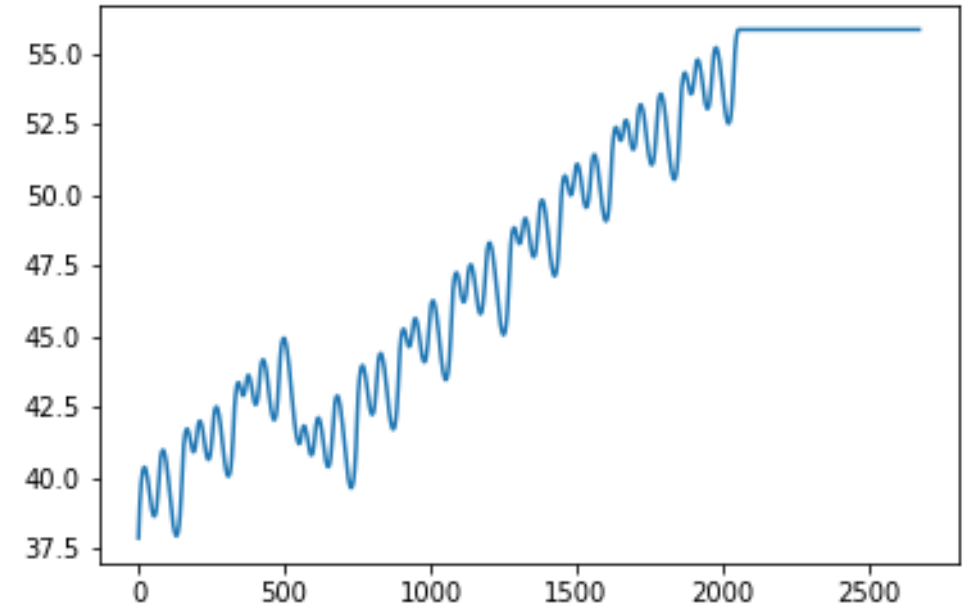

圖 4 Demo1 的 N-Cycle jitter

四、 Demo2 – UltraSim AMS

用 Lab06d-Demo4 的方法跑 AMS，將.v 檔以.sp 檔下去跑。

Demo2 的 Output Clock(MHz)：

Output Clock mean: 556.2132041287808

Output Clock RMS: 556.6152228800275

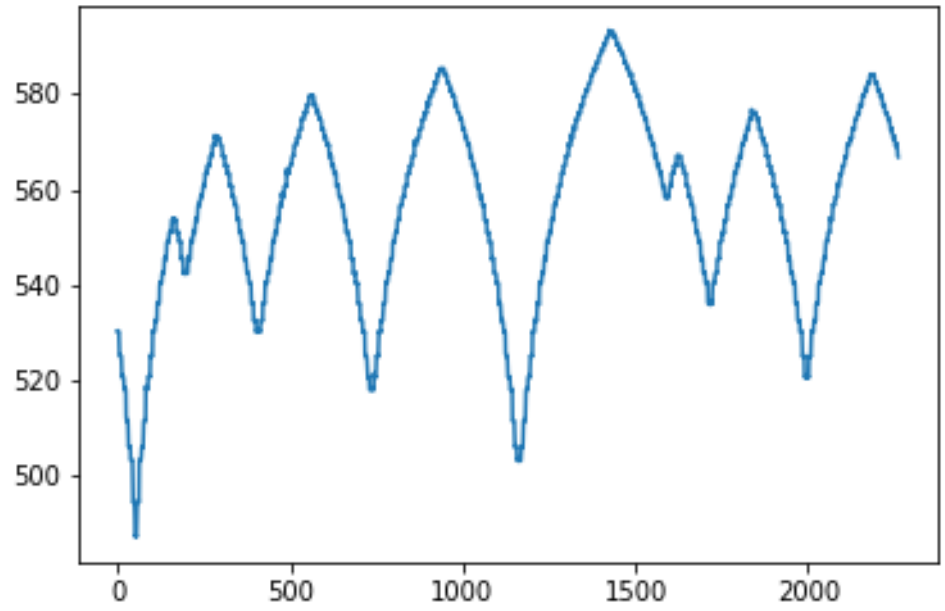

圖 5　Demo2 的 Output Clock

Demo2 的 Period jitter(ns)：

Period jitter mean: 0.0005478519009726101

Period jitter RMS: 0.07046034354653895

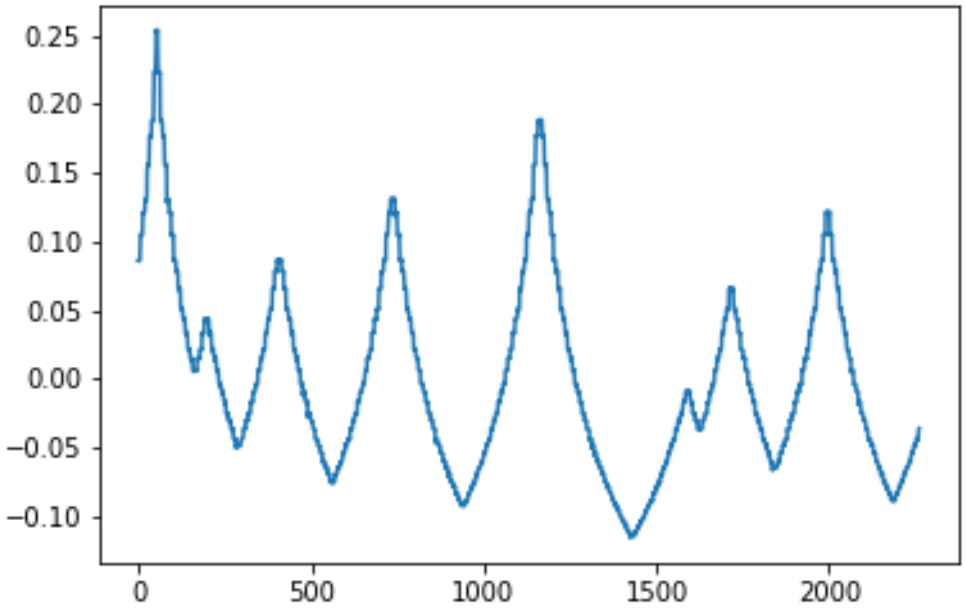

圖 6　Demo2 的 Period jitter

Demo2 的 Cycle-to-Cycle jitter(ns)：

Cycle-to-Cycle jitter mean: -5.3956675508600794e-05

Cycle-to-Cycle jitter RMS: 0.003177258546855014

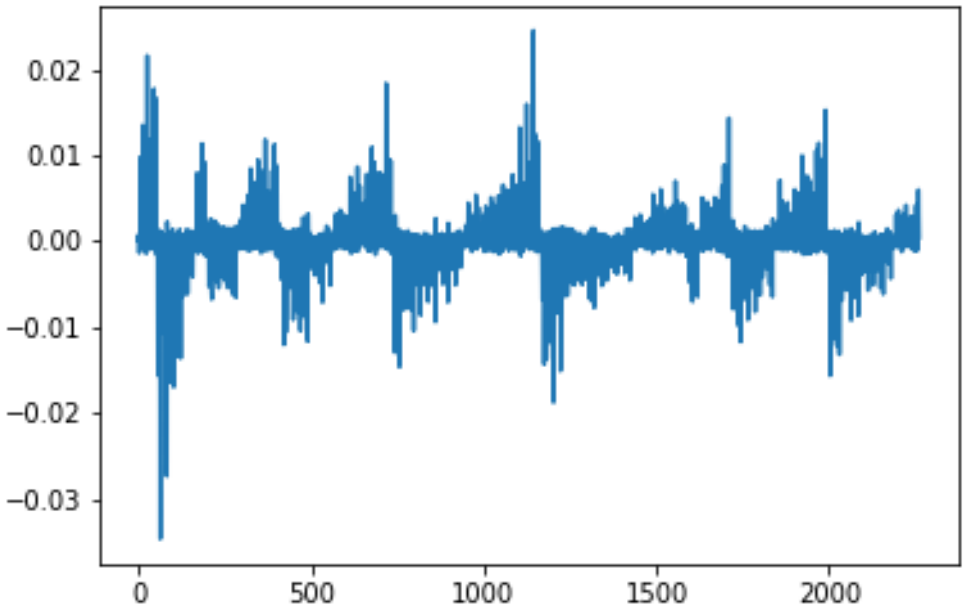

圖 7　Demo2 的 Cycle-to-Cycle jitter

Demo2 的 N-Cycle jitter(ns)：

N-Cycle jitter mean: 44.45022296684342

N-Cycle jitter RMS: 45.05773723665143

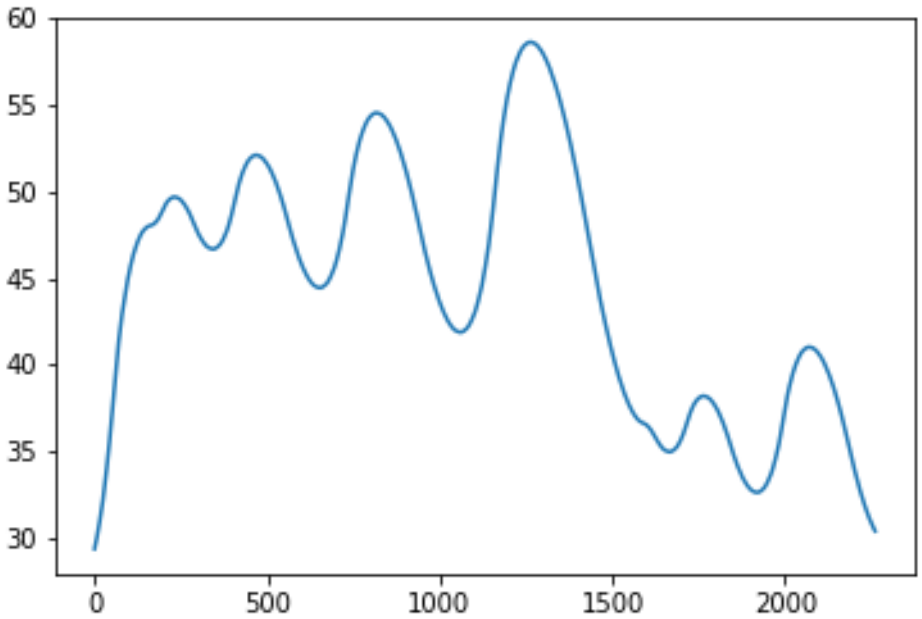

圖 8　Demo2 的 N-Cycle jitter