前瞻類比積體電路佈局設計

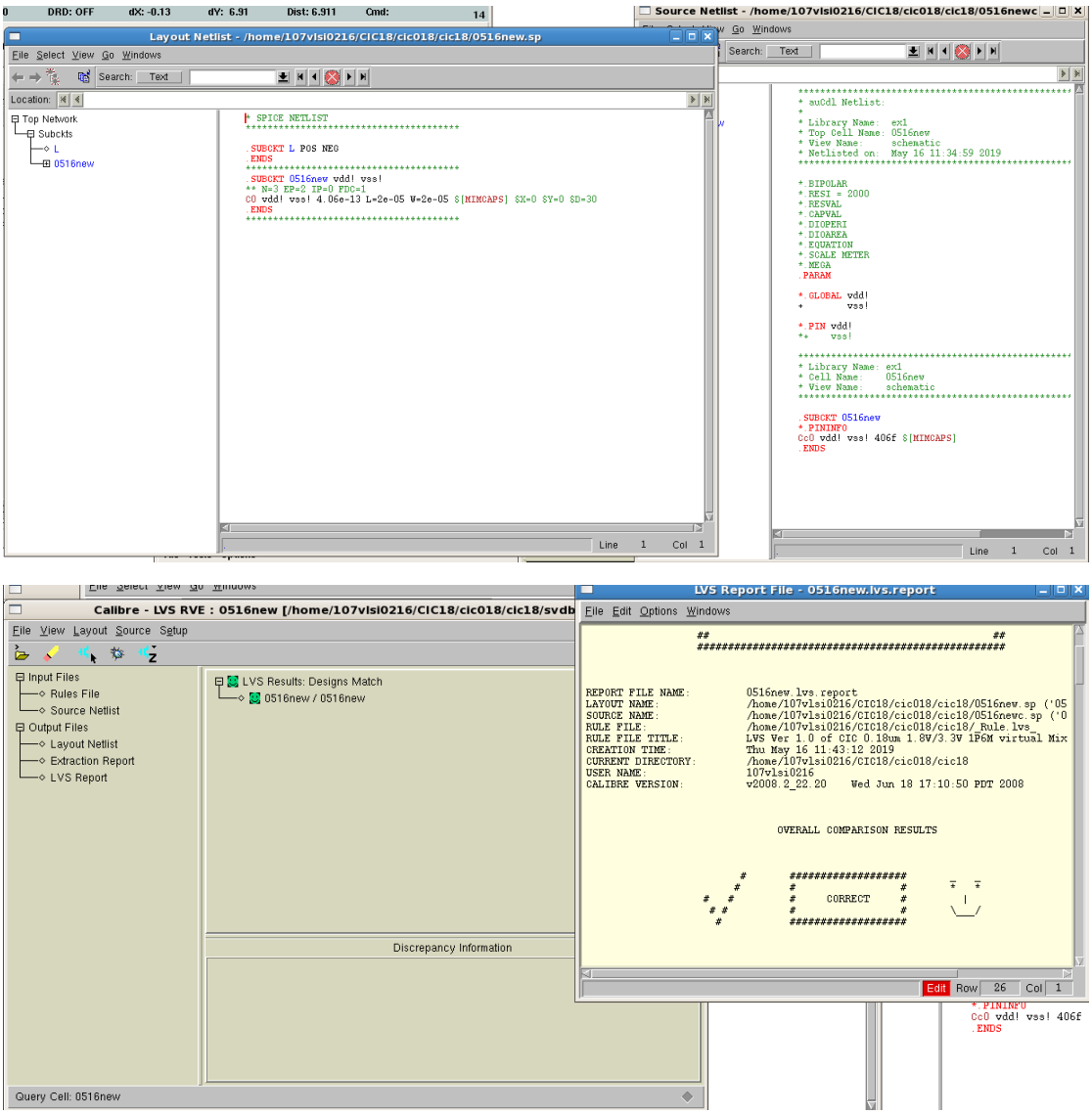
作業 八

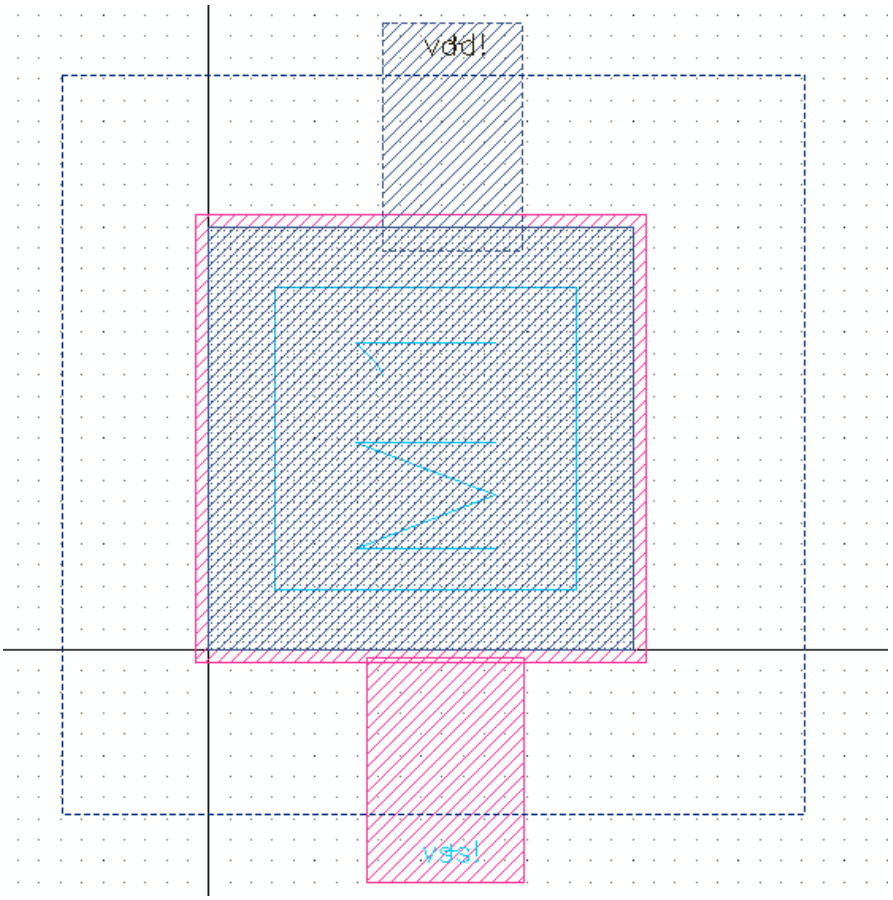
班級： 電 三 乙

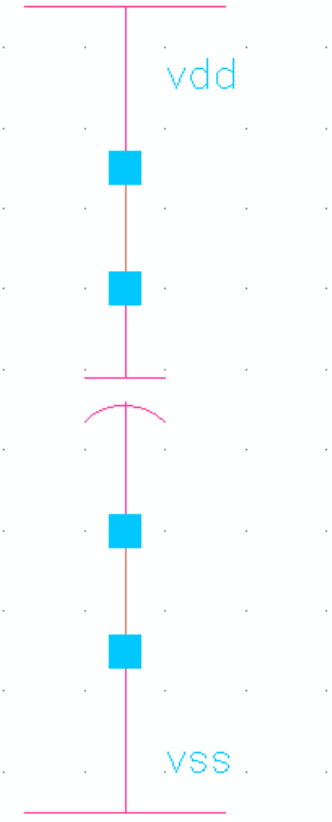
姓名： 蔡承宏

學號： 110510216

老師： 陳俊達


DRD: OFF
dX: -0.13
dY: 6.91
Dist: 6.911
Cmd:
Layout Netlist - /home/107vlsi0216/CIC18/cic018/cic18/0516new.sp
File Select View Go Windows
Search: Text
Location:
Top Network
Subckts
L
0516new
* SPICE NETLIST
.SUBCKT L POS NEG
.ENDS
.SUBCKT 0516new vdd! vss!
** N=3 EP=2 IP=0 FDC=1
C0 vdd! vss! 4.06e-13 L=2e-05 W=2e-05 $[MIMCAPS] $X=0 $Y=0 $D=30
.ENDS
Line 1 Col 1
Source Netlist - /home/107vlsi0216/CIC18/cic018/cic18/0516newc
Go Windows
Search: Text
* auCdl Netlist:
* Library Name: ex1
* Top Cell Name: 0516new
* View Name: schematic
* Netlisted on: May 16 11:34:59 2019
* BIPOLAR
* RESI = 2000
* RESVAL
* CAPVAL
* DIOPERI
* DIOAREA
* EQUATION
* SCALE METER
* MEGA
.PARAM
* GLOBAL vdd!
+ vss!
* PIN vdd!
*+ vss!
* Library Name: ex1
* Cell Name: 0516new
* View Name: schematic
.SUBCKT 0516new
* PININFO
CC0 vdd! vss! 406f $[MIMCAPS]
.ENDS
Line 1 Col 1
Calibre - LVS RVE : 0516new [/home/107vlsi0216/CIC18/cic018/cic18/svdb
File View Layout Source Setup
Input Files
Rules File
Source Netlist
Output Files
Layout Netlist
Extraction Report
LVS Report
LVS Results: Designs Match
0516new / 0516new
Discrepancy Information
Query Cell: 0516new
LVS Report File - 0516new.lvs.report
File Edit Options Windows
REPORT FILE NAME: 0516new.lvs.report
LAYOUT NAME: /home/107vlsi0216/CIC18/cic018/cic18/0516new.sp ('05
SOURCE NAME: /home/107vlsi0216/CIC18/cic018/cic18/0516newc.sp ('0
RULE FILE: /home/107vlsi0216/CIC18/cic018/cic18/_Rule.lvs_
RULE FILE TITLE: LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mix
CREATION TIME: Thu May 16 11:43:12 2019
CURRENT DIRECTORY: /home/107vlsi0216/CIC18/cic018/cic18
USER NAME: 107vlsi0216
CALIBRE VERSION: v2008.2_22.20 Wed Jun 18 17:10:50 PDT 2008
OVERALL COMPARISON RESULTS
CORRECT
Edit Row 26 Col 1
* PININFO
CC0 vdd! vss! 406f
.ENDS


vdd!
vss!


vdd
vss