KuoWei Tseng

Electrical Engineering Student | Automation | AI & ML | Digital & Analog Systems |
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EDUCATION

UNIVERSITY Of CALGARY **Calgary, CA**
Bachelor of Science in Electrical Engineering (Digital Engineering Minor) CGPA: 3.3/4.0
Expected Graduation: Apr 2026

CERTIFICATE & PROFESSIONAL DEVELOPMENT

PLC Technician Certificate I (In progress)

George Brown College, Toronto, ON (Online) Expected completion: April 2026

- Ladder Logic programming fundamentals for industrial control system.
- PLC hardware fundamentals: CPU, power supply, digital and analog I/O interface.
- Timers, counters, sequencing logic, and state-based control.
- Basic HMI integration and PLC troubleshooting practices.
- Introduction to HMI concepts and control panel integration.

SKILLS

Programming:
Machine Learning, Model Optimization, Python (Numpy, Pandas, Matplotlib, Pytorch, Tensorflow, fastai), Java, C, System Verilog, VHDL, Git.

Embedded & Control System:
PLC programming, Raspberry Pi, Arduino, PIC Microcontroller.

Hardware & Simulation:
Cadence Virtuoso, LTspice, Fusion 360.

WORK EXPERIENCE

Lision Technology Inc.
Taoyuan, Taiwan
R&D Assistant intern
06/2024 – 08/2024

- Tested and characterized discrete semiconductor devices including PN diodes, Zener, Schottky, TVS, and power MOSFETs.
- Analyzed I-V characteristics, forward/reverse bias behavior, breakdown voltage, leakage current, and recovery time.
- Studied component packaging standards including DO, SOD, SMA/SMB/SMC, SOT, TO, and axial lead.
- Evaluated thermal performance trade-offs between flat-lead and bent-lead packages, solder bonding vs wire bonding, and power-density optimization.
- Gained exposure to semiconductor packaging manufacturing flow.
- Collected and analyzed electrical measurement data using Python and Excel to support device validation.
- Assisted in verifying IC performance against design specifications and datasheets.

ACADEMIC PROJECTS

Project Name: ZEROG COATING SYSTEM—Capstone Project (https://www.zerogcoating.com**)**

- In progress (Expected completion April, 2026)
- Leveraged pretrained ResNet-18 as a backbone and fine-tuned final layers for task-specific adaptation.
- Implemented centroid-distance classification in feature space to enhance generalization and robustness to unknown inputs.
- Optimized model size and latency through compression techniques for edge devices.
- Integrated LiDAR sensing and wheel encoders on Raspberry Pi 5 for obstacle-aware navigation.
- Implementing PID-based closed-loop motion control using wheel encoder and IMU feedback to improve positioning accuracy.
- Diagnosed serial communication delays and implemented robust timeout and buffer-management logic.
- Designed autonomous preset-path coverage algorithm to ensure full surface inspection using LiDAR and wheel encoder feedback.
- Designed return-to-base strategy using vision-based homing (arUco).

Project Name: TrashAuto—Autonomous Garbage Collection Rover

- Trained and developed a two-stage CNN pipeline (YOLO and ResNet34) to classify garbage versus non-garbage objects.
- Designed and built an autonomous rover integrating LiDAR, ultrasonic sensors, IMU, wheel encoders, and camera.
- Implemented sensor-based object detection and distance tracking for navigation and obstacle avoidance using LiDAR.
- Optimized real-time inference on Raspberry Pi by event-driven triggering to reduce computation load.

Project Name: FPGA Design

- Designed a modular FPGA system using SystemVerilog, structured around a top-level FSM coordinating game logic, LED control, and display output.
- Implemented FSM logic to manage game states via multiplexers.
- Developed hardware debouncing circuits for push-button inputs to ensure reliability.
- Designed a clock divider module to generate multiple timing domains for LED animation, display multiplexing, and gameplay difficulty control.
- Created a testbench for verification of RTL modules, including FSM state transitions, clock dividers, and multiplexed display logic.

Project Name: DISCIPLINE AND FOCUS ALARM—Embedded System Design

- Designed an embedded alarm system using AVR128DB28 microcontroller programmed in C.
- Integrated real-time clock, audio amplification, and MOSFET-based power control.
- Designed a custom enclosure using Fusion 360.

PUBLICATION

1. Feasibility of recent peptide therapy for ischemic stroke. K.-F. Tseng, **K.-W. Tseng**, et al. Journal of Pharmacological Sciences, 2026. (Contribution: Data analysis and computational methodology)