Project 2

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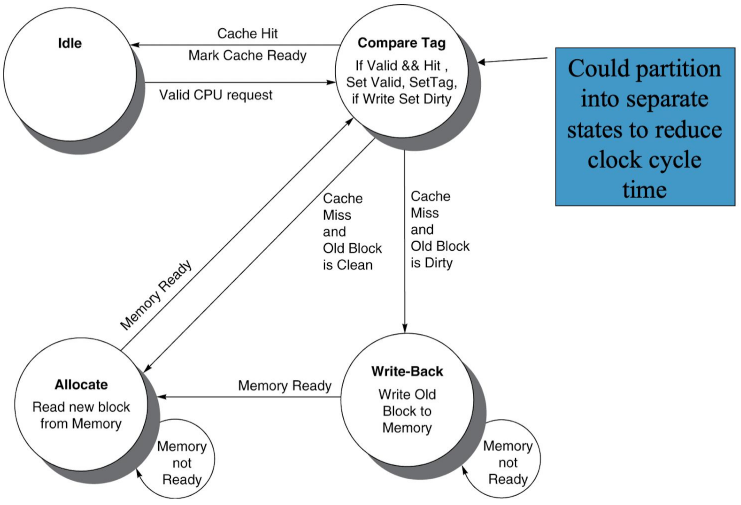
Division of labor:

曾民君（50%）	Change CPU.v , Pipeline Registers , and Debug
徐浩翔（50%）	Implement L1 Cache and Debug

Implementation:

Modules name	Description
CPU.v	Almost the same as Project_1. We add stall signal to all pipeline registers and PC
Pipeline Registers.v	Add stall signal, if stall signal is arise then do nothing when the clock is at postedge
dcatch_top.v	Implement as the following graph:  01. tag comparator: 比較 sram_tag與p1_tag 如果相等且sram_valid為1 return 1否則return 0 02. r_hit_data將它設為將它設為sram_cache_data 03. 根據p1_offset將r_hit_data的資料assign給p1_data，其中p1_offset有五個bit只取最高位的3個bit，這邊我們用了8個if去決定應該要拿r_hit_data的第幾個bit到第幾個bit，因為一開始我並不知道verilog可以宣告integer去算index但後來會的時候發現本來這樣也沒錯所以就沒改了

	04. w_hit_data 中放的是cpu要存入memory中的資料所以也要根據p1_offset放入對應的位置 05. 最後是controller的實作在state_miss中因為一定是cache miss所以必定要從memory搬資料上來，將mem_enable設成1，再來如果sram_dirty是1代表cache中的資料有被寫過需要write back回memory，所以mem_write、write_back設成1，否則兩個都還是零，state_readimss中等待資料從memory搬至cache當收到mem_ack時表示mem_data已經到了，將cache_we(write enable)設成1並跳到state_readmissok，state_readmissok這個state已經將memory的資料寫入cache所以cache_we設成0並回到state_idle，而state_write是從state_miss且dirty bit 為1時跳過來的等待mem_ack訊號如果收到時代表資料已寫回memory故將write_back及mem_write設成0也就是圖片右下角。

Difficulties encountered and solutions of this projects:

1. We had a bug at HazardDetection, it will cause a data hazard when the ID.rt == EX.writeAddr but load word commend does not have rt register so we should skip checking ID.rt == EX.writeAddr when the current command is load word.