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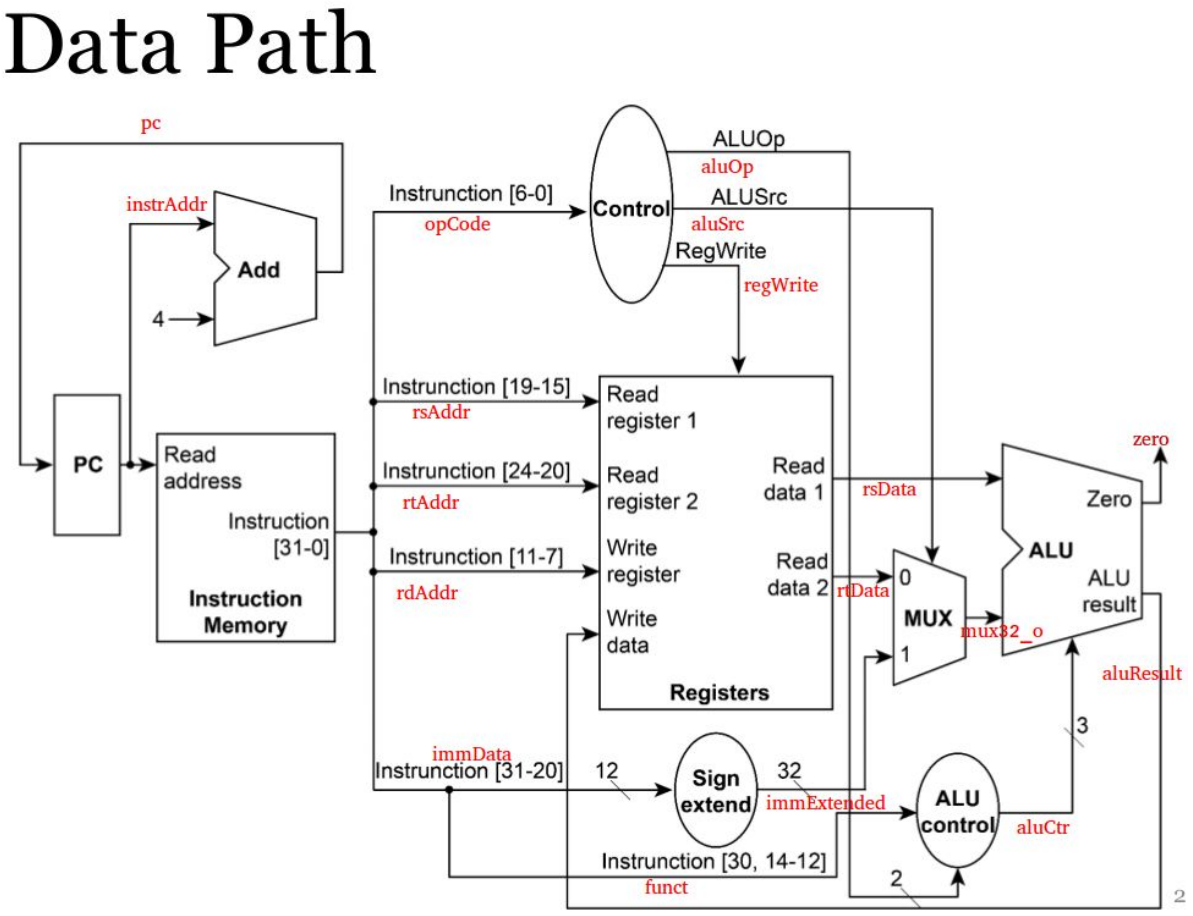
Environment: Ubuntu 16.04

1. CPU.v: wires named as



2. Adder.v: pc = instAddr + four

3. Control.v: use opCode[5] to decide aluSrc ans aluOp, let both regDst and regWrite are 1

4. ALU_Control.v: set aluCtrl based on funct as

```
case(funct_i)
    10'b0000000111: ALUCtrl_o = 3'b000;
    10'b0000000110: ALUCtrl_o = 3'b001;
    10'b0000000000: ALUCtrl_o = 3'b010;
    10'b0100000000: ALUCtrl_o = 3'b110;
    10'b0000001000: ALUCtrl_o = 3'b011;
endcase
```

but if aluOp is 01 then set aluCtrl to 3'b010

5. Sign_Extend.v: concat 20 immData[11] letf to immData[11:0]

6. ALU.v: set aluResult = rsData {+, -, *, &, |} mux32_o

7. MUX32.v: mux32_o = if aluSrc ==0: rtData? immExtented

8. MUX5.v: design logic is same as MUX32, but it doesn’t play a role in this homework