A 10-bit 40MS/s 2 Channel Time-Interleaved SAR ADC with Merged Capacitor Switching Procedure

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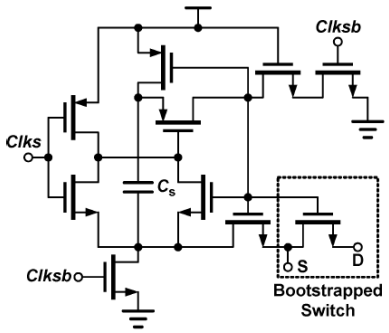
***Abstract* – This report is about the design of A 10-bit 40MS/s 2 Channel Time-Interleaved SAR ADC with a Merged capacitor switching procedure, containing schematics and layout. The content of this report includes how we design each block, the difficulties we encountered during the process, and also explanation of our solution.**

I. Introduction

The introduction will explain how we design this Time-Interleaved SAR ADC, and we will separate this Time-Interleaved SAR ADC into several subcircuits, and explain their function individually.

A. Sample and Hold circuit

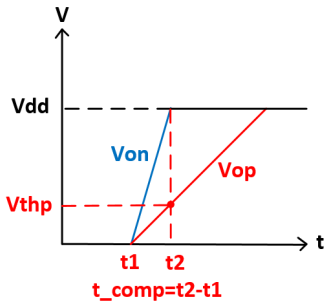
The purpose of the sample and hold circuit is to sample the input signal and hold the value of the sampled data when the sampling ends, and data will be provided to the comparator for comparison. Another purpose of this design is to reduce the Ron of the bootstrapped switch because the C_s (Fig.1) capacitor can maintain the V_{gs} of the bootstrapped switch at V_{dd} when the bootstrapped switch is turned on, therefore reducing its R_{on} to improve linearity. The capacitor size of C_s is 500f, and we use MIM capacitor to implement C_s in the layout. The ENOB of this sample and hold circuit can reach 15 bits in pre-sim when the sampling frequency is 40MHz.



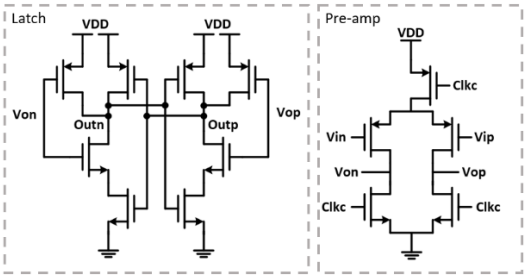
(Fig. 1)

B. Comparator

The two-stage dynamic comparator is used here, and its architecture can be divided into a pre-amplifier and latch. The differential input signal will enter the pre-amplifier first, and the output of the pre-amplifier is reset to 0, when the comparator starts operation, the speed of V_{op} and V_{on} rises differently due to the difference in input pair, resulting in different charging currents between V_{op} and V_{on} (Fig. 2). Then when a critical value is reached, the latch circuit on the right activates (Fig. 3), fixing one end at 0V and the other at 1.8V. The comparator used in this chip architecture expects that its noise can be less than 0.25 LSB in order to reduce the impact of noise.



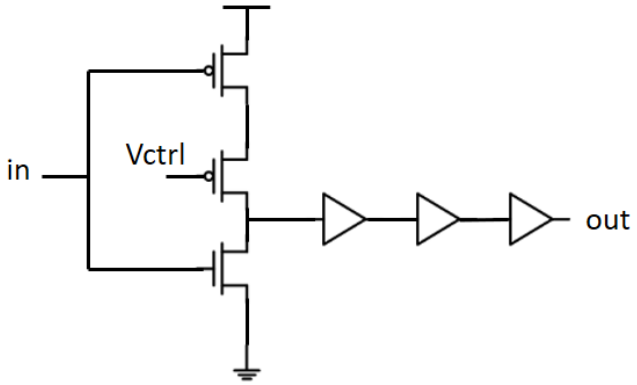
(Fig. 2)



(Fig. 3)

C. VCDL (Voltage Controlled Delay Line)

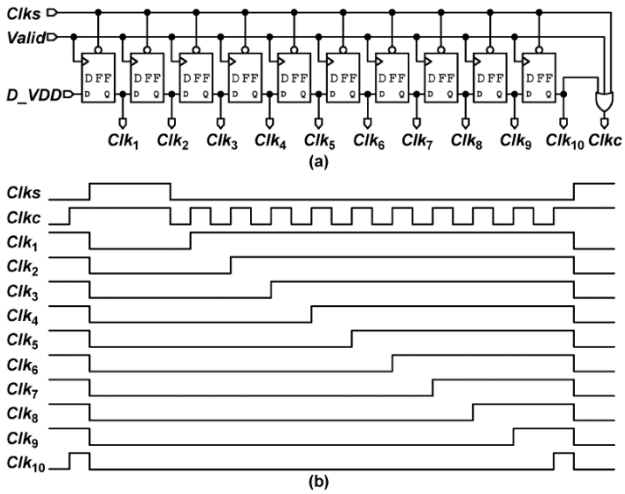
The purpose of this circuit architecture is to optimize the Clkc, because the clock's high level is too short can cause the voltage settling time to be insufficient after switching the capacitor, so through the VCDL (Fig. 4), the time of the low level can stay unchanged, but the time of high level is increased, so that the subsequent dac control settling and comparator reset can have more time. The principle of VCDL is to change the charging speed by adjusting the voltage of V_{ctrl}. In different corners, different V_{ctrl} will be used to optimize Clkc.



(Fig. 4)

D. SAR Logic

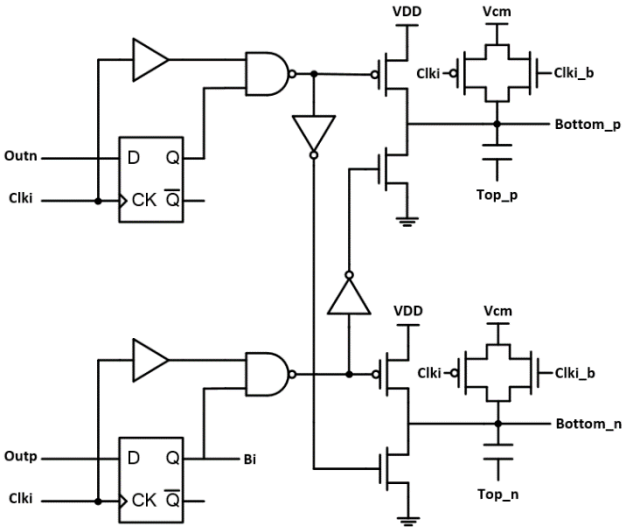
Connecting tspc d-flip-flop in series (Fig.5), will determine when to send clk_1~clk_{10} to dac-control and later determine the voltage switching result according to the validity signal sent from the comparator.



(Fig. 5)

E. DAC control

Dac control (Fig. 6) will receive clk_i (i = 1~10 from SAR logic and also comparator output_p and output_n signals. From those signals, the dac control can decide whether to switch the bottom plate which was originally in $V_{cm}(0.9V)$ to $V_{dd}(1.8V)$ or $gnd(0V)$. If the output_p is larger than the output_n, dac control will switch the positive end of the bottom plate to gnd and the negative end of the bottom plate to V_{dd}. Conversely, if the output_n is larger than the output_p, the dac control will switch negative end of the bottom plate to gnd and the positive end of bottom plate to V_{dd}.



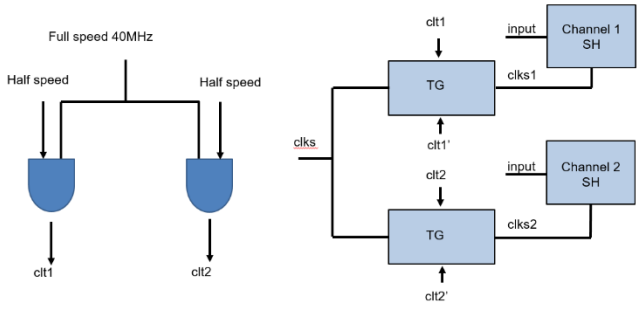
(Fig. 6)

F. CDAC layout

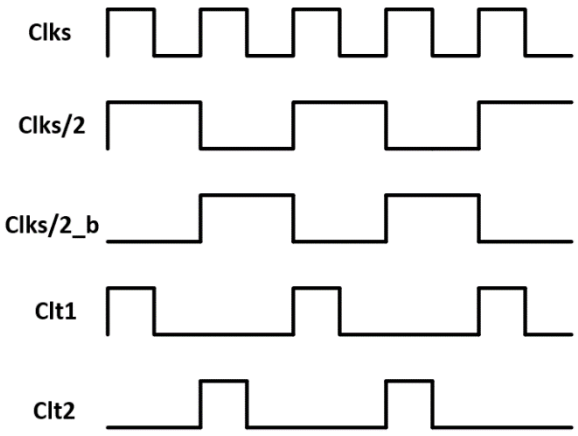
CDAC is achieved by the parasitic capacitance between metal wires. The practical implementation is about using a symmetrical MOM layout plus a guard ring, under this method, it can achieve 10^{-6} level of accuracy. The top plate can change the voltage according to the ratio of capacitance in the DAC each time, and switch successively to complete the 10-bit output result.

G. Clock generator

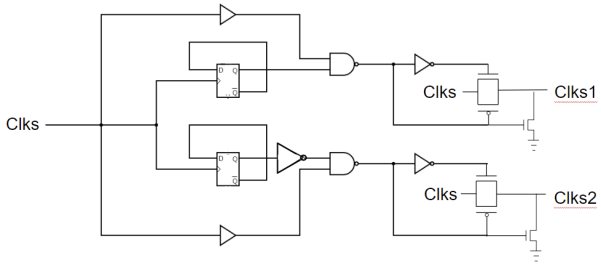
The Clks is divided by tspc d-flip-flop, and the control signals clt1 and clt2 (Fig. 7) are created by and gate to control the transmission gate, then clks1 and clks2 (Fig. 8) are obtained and sent to each channel. Adding nmos (Fig. 8) can remove the coupling effect of input on clks1 and clks2, which is generated from the sample and hold circuit. Hence, the voltage of clks1 and clks2 can keep in gnd, avoiding floating and also current leakage.



(Fig. 7)



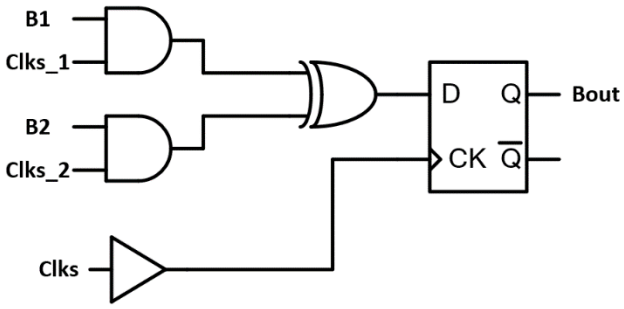
(Fig. 8)



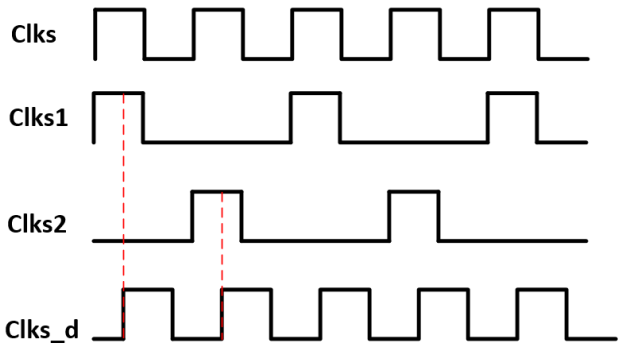
(Fig. 9)

H. Mux and Latch

Use clks1 and clks2 (Fig. 10) as signals to control mux and select output codes for different channels, but the output code can only have data when clks1 or clks2 is at a high level. Therefore, generating clks_d (Fig. 11) can help d-flip-flop to latch the data and maintain it for a full period.



(Fig. 10)



(Fig. 11)

II. SCHEMATIC

A. Concept and Design of Clock generator

Since we need control signals for SH circuit in each channel, we use logic gates to generate the clock we need. However, the clock must be accurate and cannot allow timing skew, which will significantly influence the performance of ADC. In our design, we use two control signals to control the switch, producing two sampling clocks for channels and ensuring their phase difference is constant. What's more, when one switch is turned off and the other is turned on, it will cause floating in one end. Hence, we add a switch at the output of the switch to avoid this situation.

B. Schematic and pre-sim figure

We use composer to build up our circuit (as in Fig. 2.) and convert it into spi file to run pre-sim.

Pre-sim results

Corner	ENOB
TT	10.045
SF	10.054
FS	10.038
FF	9.973
SS	10.003

We can see from the pre-sim result that FF corner has the worst ENOB, because in "Fast nmos, Fast pmos", the dac control don't have enough to switch and settle voltage, therefore having a worser performance.

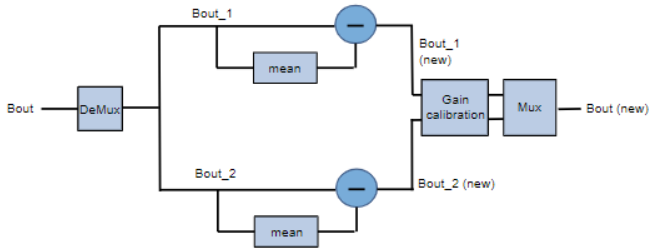
C. Data latch solution

At first, we observe the data generated from the SAR ADC will only exist when the clock in that channel is high, which cannot latch for the whole period. Therefore, additional d-flip-flops are added to make data can be latched for whole period, making following DSP become easier.

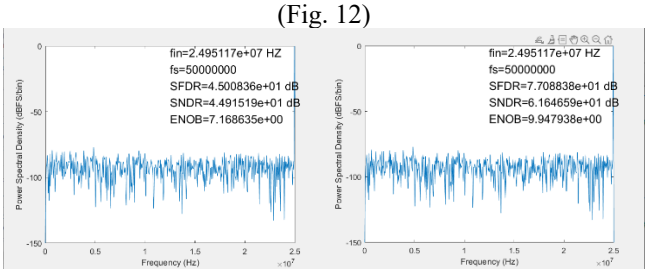
D. Off-chip offset calibration

Since the architecture of TI SAR will exist offset, which will significantly degrade the circuit performance. Therefore, we propose the off-chip offset calibration to reduce this side effect. The schematic of the calibration is shown in Fig. 12,

which will be executed in MATLAB, and the dc offset on the channel will be canceled. To figure out the effect of calibration, we add 30mV offset to channel_1 and 20mV to channel_2, and the result of calibration can be seen in Fig.13.



(Fig. 12)



(Fig. 13, left is before calibration, and the right is after calibration)

III. LAYOUT

What we need to notice when drawing layout is that we need to carefully select the layer of metal when drawing metal lines. The metal used on analog wires and digital wires should be specified, in order to keep the signal clean and avoid coupling.

Density is another issue. After we finish the main chip, we still need to satisfy the density rule in order to pass the DRC rule. Therefore, we use moscap to fill up the remaining space.

The location of each block is also important. For example, we cannot keep two CDAC too close, or they may influence each other when switching voltage. Also, recognition layers are important to distinguish whether the power type belongs to analog or digital.

After finishing the layout, we measured that the overall area is 1200×1100 μm^2.

IV. POST-SIM RESULT

We run post-sim (with R-C-CC extraction) at TT 25°C, and the result is as follows.

post-sim results

Corner	ENOB
TT	9.559
SF	9.66
FS	9.7
FF	9.645
SS	9.703

Specification	Spec.	Pre-sim (TT)	Post-sim (TT)
Power supply (V)	1.8V	1.8V	1.8V
Power Consumption	2mW	1.32mW	1.68mW
Sampling frequency	40MHz	40MHz	40MHz
ENOB	> 9.5	10.045	9.559

From the post-sim result, we can see that ENOB in each corner is lower than the pre-sim result, because lots of parasitic capacitances are generated after layout, and we cannot perfectly simulate those side-effects during pre-sim. Due to that parasitic capacitance, each block will need extra time to finish its task and therefore decrease overall performance.

Also, we use lots of metal wires in the layout, and those metal wires will create lots of resistance and capacitance in our design. Therefore, we have adjusted the direction and width of metal wires in order to lower side effects as much as possible.

V. IMPROVEMENTS AND SUGGESTIONS

In order to optimize our design, we may try to decrease the parasitic capacitance first. After analyzing, we found that digital blocks, such as d-flip-flips and delay chains, cause lots of parasitic capacitance. Therefore, we can try to re-design those digital blocks because they are used frequently in each block.

Also, we can use off-chip calibrations to diminish the gain mismatch or other non-ideal effects, thus can improve the quality of digital outputs.

VI. DIAGRAMS

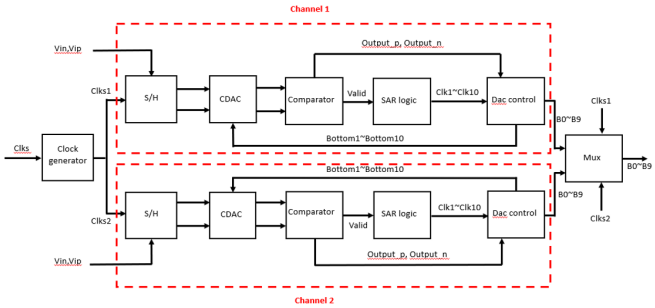


Fig. 14
Schematic of total circuit

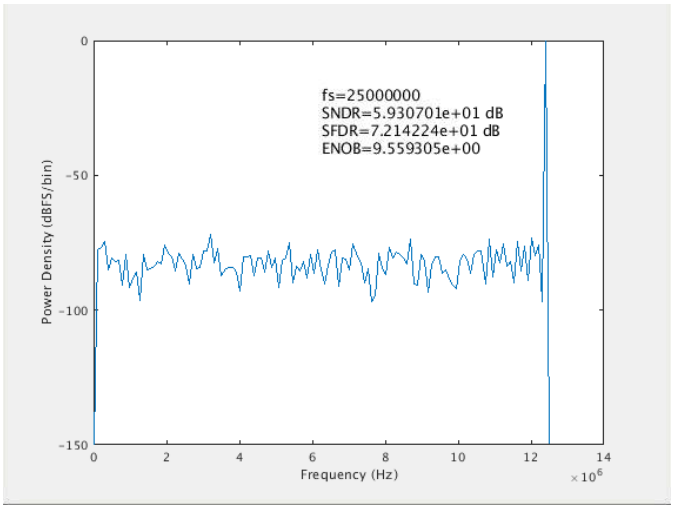


Fig. 15
Post-sim matlab result(25℃, TT corner)

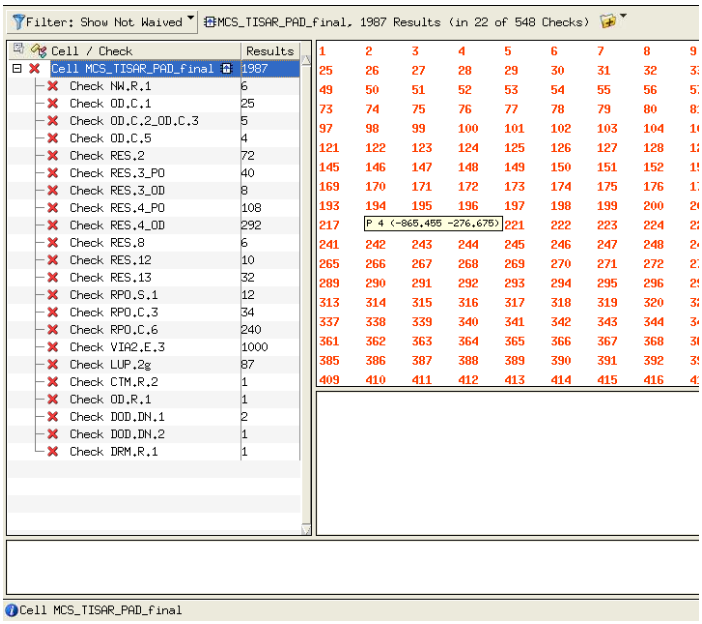


Fig. 16
DRC Result (all errors are tolerable)

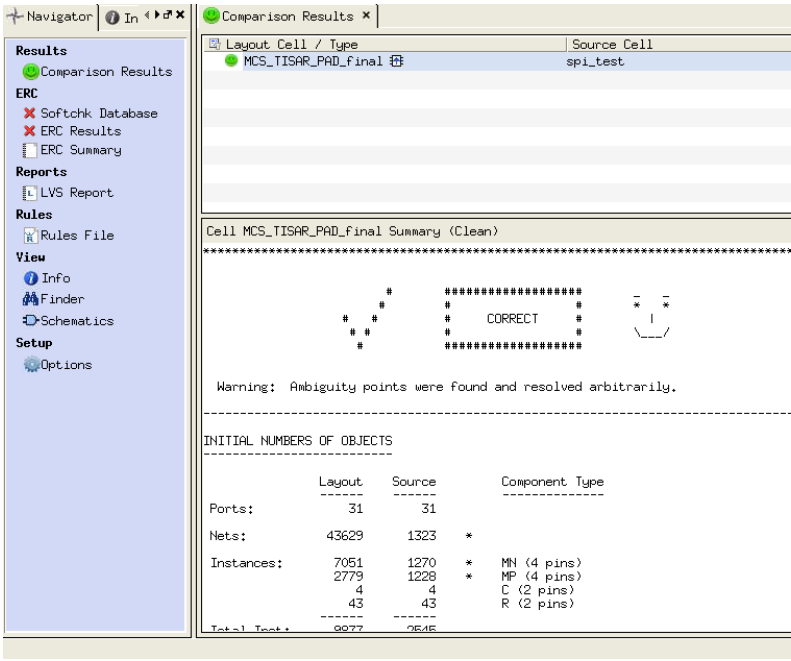


Fig. 17
LVS Result

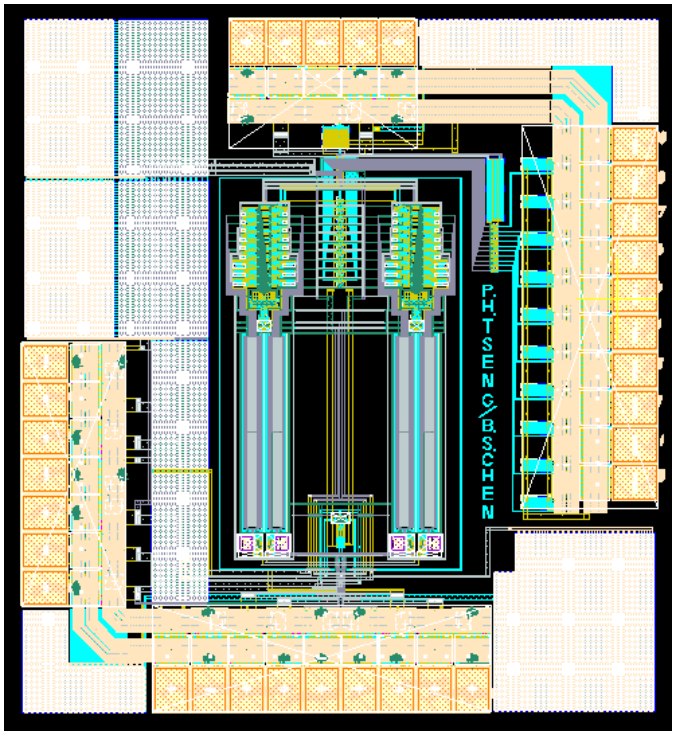


Fig. 18
Layout

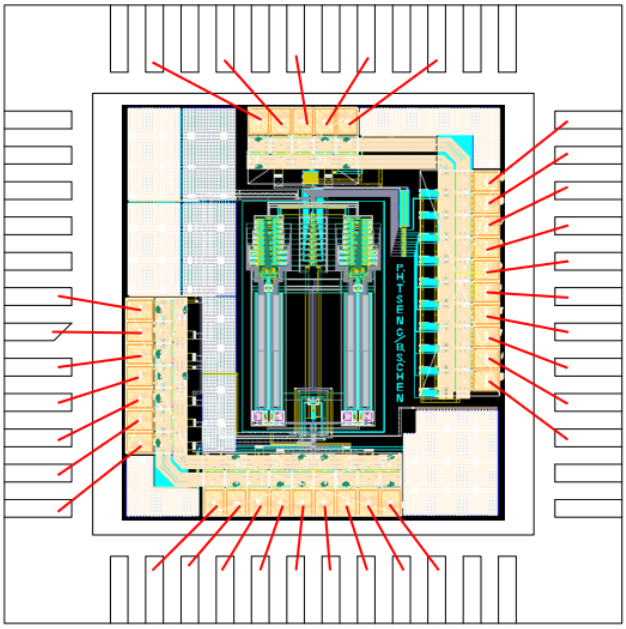


Fig. 19
Wire bonding diagram

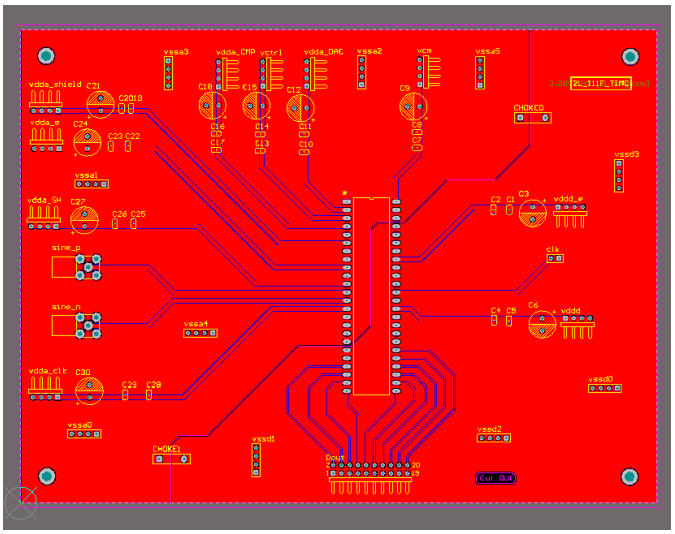


Fig. 20
PCB layout