**2-Bit Binary Adder**

Group Members:

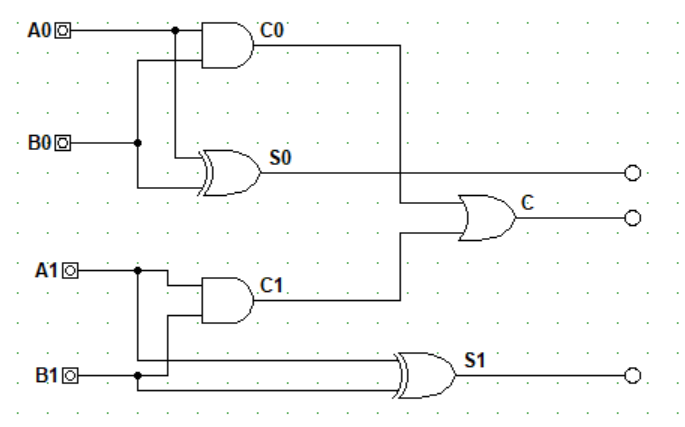
* Rethabile Matela (202202297)
* Keabetsoe Williams (202201059)
* Tsita Makhele (202201268)
* Boitumelo Lekau (202202277)
* Liteboho Ntene (202100018)
* Mpho Malebelle (202100008)
* Puseletso Rakhoabe (202201180)

**OBJECTIVE**

To construct a functional two bit binary adder.

A two bit adder is a circuit to add 2-bit numbers together. The first number, A, is represented by bits a1 and a0, while the second number, B, is represented similarly. The result of the addition includes the sum, shown by two bits (s1 and s0), along with an extra carry bit (c ).

**CIRCUIT WITH TWO HALF ADDERS(Circuit A)**

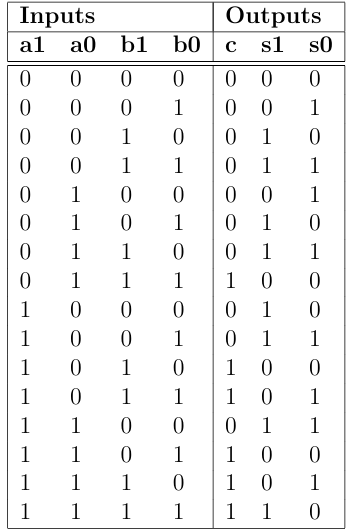


According to the instructions, we constructed this circuit but its outputs do not correspond to the expected outputs of the 2 bit half adder truth table.

**Truth table of this circuit**

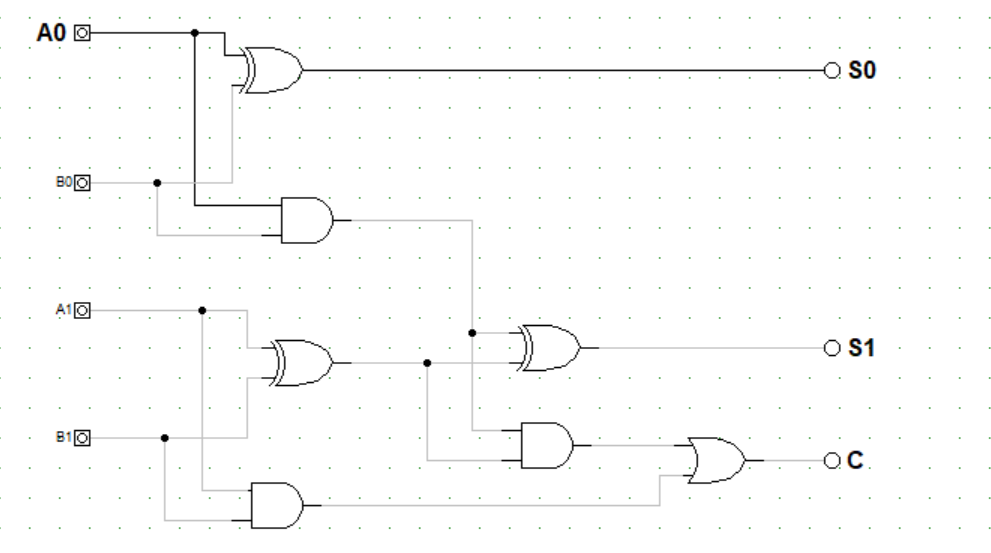
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | **OUTPUTS** | | |
| A1 | A0 | B1 | B0 | C | S1 | S0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |

**Truth table of a two bit binary Adder**

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**THE REDESIGNED CIRCUIT.(Circuit B)**



We then designed this two bit binary adder using three half adders. Three half adders are needed to manage the sums and carry bits correctly. The first half adder processes the least significant bits, the second half adder handles the most significant bits along with the carry from the first, and the third half adder manages the final carry-out bit.

**TESTING PROCESS AND VERIFICATION**

We used digital works software for both circuits to test all 16 possible outcomes.

**Circuit A**

From the two bit binary adder with two half adders, when Testing all possible inputs, some of the outputs were incorrect when compared to that of a 2 bit binary adders correct truth table.

**Circuit B**

From the two bit binary adder with three half adders, when Testing all possible inputs, all expected outputs were aligned with the outputs of the constructed truth table. This was confirmed by manually adding binary numbers and constructing a correct truth table of a 2 bit adder.

**Simulation process and Test Results**

Circuit A:

<https://youtu.be/gk3Zb1XeWGg?si=yfiSSdja7SnN_pqp>

Circuit B:

<https://youtu.be/lO9-MeABEIQ?si=ICONcG-s_O9DoNyY>

We demonstrated both circuits on the links of the videos above.

**CHALLENGES ENCOUNTERED**

We encountered a challenge in circuit A since Two bit half adders are not sufficient for a two-bit binary adder, they cannot handle carry propagation between bits. Each half adder only adds two single-bit numbers and does not carry over any carry bits to next stage. Therefore circuit A did not give expected outputs.

**SOLUTION**

We added a third half adder in order to make a full adder that accounts for a carry bit.

**Conclusion**

Circuit A does not result to the expected outputs and Circuit B does, therefore we concluded that circuit B is the correct circuit for a two bit binary adder.