COMPUTER ORGANIZATION

Lecture 1
Course Information

2025 Spring

baiyh@sustech.edu.cn

Course Information

- Course website: Blackboard
- Instructor:
  - Dr. Yuhui BAI (baiyh@sustech.edu.cn)
  - Office: 411 College of Engineering South
  - Office hour: Thursday 14:00-16:00 (by appointment)
- Lecture
  - 10:20-12:10 Mon., 108, Lecture Hall #1
- Lab
  - 14:00 -15:50 Mon., 503, Lecture Hall #3 (BAI Yuhui)
  - 14:00 -15:50 Mon., 502, Lecture Hall #3 (WANG Qing)
  - 14:00 -15:50 Wed., 509, Lecture Hall #3 (WANG Qing)

Grading Policy

- 30% Mid-term examination
  - tentatively scheduled at week 8 weekend
- 30% Final examination
- 30% Lab
  - 5% Attendance and Lab practices
  - 10% Lab assignments - OJ
  - 15% Lab Project
    - In groups of 2~3. Please team up as soon as possible.
- 5~10% Homework
- 5~0% Lecture Attendance

- Note:
  - Submit the **commitment letter** on Blackboard system before Monday of week 4, end of day (请务必于第4周前签署承诺书)

Honor policy

- All course work should be completed entirely on your own. You are encouraged to discuss general concepts and ideas in homework or lab assignments.
- Students who commit an act of academic dishonesty may receive a zero on the assignment (first conduct) or in the course (multiple conducts).
- Unless otherwise noted, exams and individual assignments will be pledged that you have neither given nor received unauthorized help.
- If you have questions on what is allowable, ask!

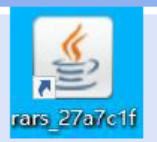
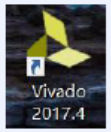
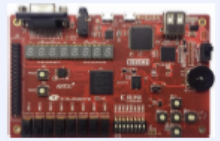
Course Schedule

WEEK	LECTURE	LECTURE TOPIC	LAB CONTENT
1	Lecture #1	Introductions	Environment Setup
2	Lecture #2	RISC-V ISAs: Basics	Assembly Practice 1
3	Lecture #3	RISC-V ISAs: Procedure Call	Assembly Practice 2
4	Lecture #4	RISC-V ISAs: Addressing	Assembly Practice 3
5	Lecture #5	Performance	Assembly Practice 4
6	Lecture #6	Arithmetic	Assembly Practice 5
7	Lecture #7	Floating Point Arithmetic	Assembly Practice 6
8	Lecture #8	The Processor (**Midterm in weekend**)	Verilog:EDA tools
9	Lecture #9	The Pipeline	CPU Design 1
10	Lecture #10	Instruction-Level Parallelism	CPU Design 2
11	Lecture #11	Memory Hierarchy	CPU Design 3
12	Holiday	/	CPU Design 4
13	Lecture #12	Memory Hierarchy(cont.)	CPU Design 5
14	Lecture #13	Memory Hierarchy(cont.)	CPU Design 6
15	Lecture #14	Parallel Processors	Project Inspection
16	Holiday	/	Project Inspection

Lab Setup

- Labs are a key portion of the class
- Highly recommended to find your partner as soon as possible.

Toolkits used in our Labs

Task	Tool kits
Learn and practice **RISC-V**(a type of Assemblly language)	➢ **Rars (rars_27a7c1f)** 
Design and implement an **CPU**	➢ **Vivado**  ➢ **FPGA based Development Board EGO1** 
Test the **CPU** with **program(s)**, both of which are based on **RISC-V**	➢ **Assembler (Rars)** ➢ **Uart Tools** ➢ **Vivado** ➢ **FPGA based Development Board(EGO1)**

Textbooks

- Textbook:
  - Computer Organization & Design, the Hardware/Software Interface, RISC-V edition. D. A. Patterson and J. L. Hennessy
    - The Textbook uses RV64, in class we learn RV32
- Reference book:
  - Computer Architecture - a quantitative approach, Hennessy and Patterson, 5th edition