Pin Name	LQFP100 Pin	Smoothie Board Reserved	Reconfigurable?	ADC Input	I2C	SPI
TDO/SWO	1	1				
TDI	2	1				
TMS/SWDIO	3	1				
TRST	4	1				
TCK/SWDCLK	5	1				
P0[26]/AD0[3]/AOUT/RXD3	6		1	1		
P0[25]/AD0[2]/I2SRX_SDA/TXD3	7		1	1		
P0[24]/AD0[1]/I2SRX_WS/CAP3[1]	8		1	1		
P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]	9		1	1		
V_{DDA}	10	1				
V_{SSA}	11	1				
VREFP	12	1				
n.c.	13	1				
RSTOUT	14	1				
VREFN	15	1				
RTCX1	16	1				
RESET	17	1				
RTCX2	18	1				
VBAT	19	1				
P1[31]/SCK1/AD0[5]	20		1	1		
P1[30]/V_{BUS}/AD0[4]	21		1	1		
XTAL1	22	1				
XTAL2	23	1				
P0[28]/SCL0/USB_SCL	24	1				
P0[27]/SDA0/USB_SDA	25	1				
P3[26]/STCLK/MAT0[1]/PWM1[3]	26		1			
P3[25]/MAT0[0]/PWM1[2]	27		1			
$V_{DD(3V3)}$	28	1				
P0[29]/USB_D+	29	1				
P0[30]/USB_D	30	1				
V_{SS}	31	1				
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]	32		1			

P1[19]/MCOA0/USB_PPWR/CAP1[1]	33		1		
P1[20]/MCI0/PWM1[2]/SCK0	34		1		
P1[21]/MCABORT/PWM1[3]/SSEL0	35		1		
P1[22]/MCOB0/USB_PWRD/MAT1[0]	36		1		
P1[23]/MCI1/PWM1[4]/MISO0	37		1		1
P1[24]/MCI2/PWM1[5]/MOSI0	38		1		1
P1[25]/MCOA1/MAT1[1]	39		1		
P1[26]/MCOB1/PWM1[6]/CAP0[0]	40		1		
V_{SS}	41	1			
$V_{DD(REG)(3V3)}$***	42	1			
P1[27]/CLKOUT/USB_OVRCR/CAP0[1]	43		1		
P1[28]/MCOA2/PCAP1[0]/MAT0[0]	44		1		
P1[29]/MCOB2/PCAP1[1]/MAT0[1]	45		1		
P0[0]/RD1/TXD3/SDA1	46		1	1	
P0[1]/TD1/RXD3/SCL1	47		1	1	
P0[10]/TXD2/SDA2/MAT3[0]	48		1	1	
P0[11]/RXD2/SCL2/MAT3[1]	49		1	1	
P2[13]/EINT3/I2STX_SDA	50		1		
P2[12]/EINT2/I2STX_WS	51		1		
P2[11]/EINT1/I2STX_CLK	52		1		
P2[10]/EINT0/NMI	53		1		
$V_{DD(3V3)}$	54	1			
V_{SS}	55	1			
P0[22]/RTS1/TD1	56		1		
P0[21]/RI1/RD1	57		1		
P0[20]/DTR1/SCL1	58		1	1	
P0[19]/DSR1/SDA1	59		1	1	
P0[18]/DCD1/MOSI0/MOSI	60		1		1
P0[17]/CTS1/MISO0/MISO	61		1		1
P0[15]/TXD1/SCK0/SCK	62		1		1
P0[16]/RXD1/SSEL0/SSEL	63		1		1
P2[9]/USB_CONNECT/RXD2	64		1		
P2[8]/TD2/TXD2	65		1		
P2[7]/RD2/RTS1	66		1		
P2[6]/PCAP1[0]/RI1/TRACECLK	67		1		
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]	68		1		
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]	69		1		
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]	70		1		
$V_{DD(3V3)}$	71	1			
V_{SS}	72	1			
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]	73		1		
P2[1]/PWM1[2]/RXD1	74		1		
P2[0]/PWM1[1]/TXD1	75		1		

P0[9]/I2STX_SDA/MOSI1/MAT2[3]	76	1		
P0[8]/I2STX_WS/MISO1/MAT2[2]	77	1		
P0[7]/I2STX_CLK/SCK1/MAT2[1]	78	1		
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]	79	1		
P0[5]/I2SRX_WS/TD2/CAP2[1]	80		1	
P0[4]/I2SRX_CLK/RD2/CAP2[0]	81		1	
P4[28]/RX_MCLK/MAT2[0]/TXD3	82		1	
V_{SS}	83	1		
$V_{DD(REG)(3V3)}$	84	1		
P4[29]/TX_MCLK/MAT2[1]/RXD3	85		1	
P1[17]/ENET_MDIO	86	1		
P1[16]/ENET_MDC	87	1		
P1[15]/ENET_REF_CLK	88	1		
P1[14]/ENET_RX_ER	89	1		
P1[10]/ENET_RXD1	90	1		
P1[9]/ENET_RXD0	91	1		
P1[8]/ENET_CRS	92	1		
P1[4]/ENET_TX_EN	93	1		
P1[1]/ENET_TXD1	94	1		
P1[0]/ENET_TXD0	95	1		
$V_{DD(3V3)}$	96	1		
V_{SS}	97	1		
P0[2]/TXD0/AD0[7]	98		1	1
P0[3]/RXD0/AD0[6]	99		1	1
RTCK	100	1		

Smoothie Function	Notes
NC-JTAG	
NC-JTAG	
NC-JTAG	
NC-JTAG	
NC-JTAG	
TH4	
TH3	
TH2	
TH1	
3.3V	
GND	
3.3V	
NC	
doesn’t exist in symbol	
GND	
NC	
Reset button	
NC	
3.3V	
P1_31	
P1_30	
Crystal	
Crystal	
I2C	Verify firmware
I2C	Verify firmware
P3_26	
P3_25	
3.3V	
USB	
USB	
GND	
LED1	

LED2	
LED3	
LED4	
P1_22	
P1_23	
X_MIN	
X_MAX	
Y_MIN	
GND	
3.3V	
Y_MAX	
Z_MIN	
Z_MAX	
POT_SDA	should be, check firmware option ability
POT_SCL	should be, check firmware option ability
EN2	
DIR2	
DIR5	
PLAY/P2_12	
P2_11	
ISP_BOOT/P2_10	
3.3V	
GND	
DIR4	
EN4	
DIR3	
EN3	
Panel SPI	
Panel SPI	
Panel SPI	
Panel SPI	
P2_9	
STP5	
P2_7	
P2_6	
P2_5	
P2_4	
ST4	
3.3V	
GND	
ST3	
ST2	
ST1	

SPI_SD	
SPI_SD	
SPI_SD	
SPI_SD	
DIR1	
EN1	
PLAY_LED	
GND	
3.3V	
EN5	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
Ethernet	
3.3V	
GND	
TX_0	not sure
RX_0	not sure
NC	

Pin Name	LQFP100 Pin	Smoothie Board Reserved?	Reconfigurable?	ADC Input	I2C	SPI	Smoothie Function	F1	F2	F3	F4	PEX Group	Func	Net Name
P0[9]/I2STX_SDA/MOSI1/MAT2[3]	76	1					SPI_SD	P0[9]	I2STX_SDA	MOSI1	MAT2[3]	0.11	SPI1	J01.PX1.A12
P0[8]/I2STX_WS/MISO1/MAT2[2]	77	1					SPI_SD	P0[8]	I2STX_WS	MISO1	MAT2[2]	0.12	SPI1	J01.PX2.A13
P0[7]/I2STX_CLK/SCK1/MAT2[1]	78	1					SPI_SD	P0[7]	I2STX_CLK	SCK1	MAT2[1]	0.13	SPI1	J01.PX4.A15
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]	79	1					SPI_SD	P0[6]	I2SRX_SDA	SSEL1	MAT2[0]	0.14	SPI1	J01.PX3.A14
P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]	9		1	1			TH1	P0[23]	AD0[0]			1.11	ADC/UART	J02.PX1.A12
P0[24]/AD0[1]/I2SRX_WS/CAP3[1]	8		1	1			TH2	P0[24]	AD0[1]			1.12	ADC/UART	J02.PX2.A13
P0[26]/AD0[3]/AOUT/RXD3	6		1	1			TH4	P0[26]	AD0[3]	AOUT	RXD3	1.13	ADC/UART	J02.PX3.A14
P0[25]/AD0[2]/I2SRX_SDA/TXD3	7		1	1			TH3	P0[25]	AD0[2]		TXD3	1.14	ADC/UART	J02.PX4.A15
P1[31]/SCK1/AD0[5]	20		1	1			P1_31	P1[31]	SCK1	AD0[5]		1.21	ADC/UART	J03.PX1.A12
P1[30]/VBUS/AD0[4]	21		1	1			P1_30	P1[30]	VBUS	AD0[4]		1.22	ADC/UART	J03.PX2.A13
P0[3]/RXD0/AD0[6]	99		1	1			RX_0	P0[3]	RXD0	AD0[6]		1.23	ADC/UART	J03.PX3.A14
P0[2]/TXD0/AD0[7]	98		1	1			TX_0	P0[2]	TXD0	AD0[7]		1.24	ADC/UART	J03.PX4.A15
P2[7]/RD2/RTS1	66		1				P2_7	P2[7]				1.31	UART	J04.PX1.A12
P2[6]/PCAP1[0]/RI1/TRACECLK	67		1				P2_6	P2[6]				1.32	UART	J04.PX2.A13
P2[9]/USB_CONNECT/RXD2	64		1				P2_9	P2[9]		RXD2		1.33	UART	J04.PX3.A14
P2[8]/TD2/TXD2	65		1				STP5	P2[8]		TXD2		1.34	UART	J04.PX4.A15
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]	70		1				ST4	P2[3]	PWM1[4]			1.41	UART/PWM	J05.PX1.A12
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]	73		1				ST3	P2[2]	PWM1[3]			1.42	UART/PWM	J05.PX2.A13
P2[1]/PWM1[2]/RXD1	74		1				ST2	P2[1]	PWM1[2]	RXD1		1.43	UART/PWM	J05.PX3.A14
P2[0]/PWM1[1]/TXD1	75		1				ST1	P2[0]	PWM1[1]	TXD1		1.44	UART/PWM	J05.PX4.A15
P0[4]/I2SRX_CLK/RD2/CAP2[0]	81		1				EN1	P0[4]				1.51	UART/CAN	J06.PX1.A12
P0[5]/I2SRX_WS/TD2/CAP2[1]	80		1				DIR1	P0[5]				1.52	UART/CAN	J06.PX2.A13
P4[29]/TX_MCLK/MAT2[1]/RXD3	85		1				EN5	P4[29]			RXD3	1.53	UART/CAN	J06.PX3.A14
P4[28]/RX_MCLK/MAT2[0]/TXD3	82		1				PLAY_LED	P4[28]			TXD3	1.54	UART/CAN	J06.PX4.A15
P0[18]/DCD1/MOSI0/MOSI	60		1			1	Panel SPI	P0[18]		MOSI0		2.11	SPI0	J07.PX1.A12
P0[17]/CTS1/MISO0/MISO	61		1			1	Panel SPI	P0[17]		MISO0		2.12	SPI0	J07.PX2.A13
P0[15]/TXD1/SCK0/SCK	62		1			1	Panel SPI	P0[15]		SCK0		2.13	SPI0	J07.PX4.A15
P0[16]/RXD1/SSEL0/SSEL	63		1			1	Panel SPI	P0[16]		SSEL0	SSEL	2.14	SPI0	J07.PX3.A14
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]	32		1				LED1	P1[18]		PWM1[1]		3.11	PWM	J08.PX1.A12
P1[20]/MCI0/PWM1[2]/SCK0	34		1				LED3	P1[20]		PWM1[2]		3.12	PWM	J08.PX2.A13
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]	68		1				P2_5	P2[5]	PWM1[6]			3.13	PWM	J08.PX3.A14
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]	69		1				P2_4	P2[4]	PWM1[5]			3.14	PWM	J08.PX4.A15
P0[22]/RTS1/TD1	56		1				DIR4	P0[22]				4.11	I2C/CAN	J09.PX1.A12
P0[21]/RI1/RD1	57		1				EN4	P0[21]				4.12	I2C/CAN	J09.PX2.A13
P0[20]/DTR1/SCL1	58		1		1		DIR3	P0[20]		SCL1		4.13	I2C/CAN	J09.PX3.A14
P0[19]/DSR1/SDA1	59		1		1		EN3	P0[19]		SDA1		4.14	I2C/CAN	J09.PX4.A15
P0[0]/RD1/TXD3/SDA1	46		1		1		POT_SDA	P0[0]				4.21	I2C	J10.PX1.A12
P0[1]/TD1/RXD3/SCL1	47		1		1		POT_SCL	P0[1]				4.22	I2C	J10.PX2.A13
P0[11]/RXD2/SCL2/MAT3[1]	49		1		1		DIR2	P0[11]	RXD2	SCL2		4.23	I2C	J10.PX3.A14
P0[10]/TXD2/SDA2/MAT3[0]	48		1		1		EN2	P0[10]	TXD2	SDA2		4.24	I2C	J10.PX4.A15
P2[13]/EINT3/I2STX_SDA	50		1				DIR5	P2[13]				5.11	GPIO	J11.PX1.A12
P2[12]/EINT2/I2STX_WS	51		1				PLAY/P2_12	P2[12]				5.12	GPIO	J11.PX2.A13
P2[11]/EINT1/I2STX_CLK	52		1				P2_11	P2[11]				5.13	GPIO	J11.PX3.A14
P2[10]/EINT0/NMI	53		1				ISP_BOOT/P2_10	P2[10]				5.14	GPIO	J11.PX4.A15
P3[26]/STCLK/MAT0[1]/PWM1[3]	26		1				P3_26	P3[26]				5.21	GPIO	J12.PX1.A12
P3[25]/MAT0[0]/PWM1[2]	27		1				P3_25	P3[25]				5.22	GPIO	J12.PX2.A13
P1[19]/MCOA0/USB_PPWR/CAP1[1]	33		1				LED2	P1[19]				5.23	GPIO	J12.PX3.A14
P1[21]/MCABORT/PWM1[3]/SSEL0	35		1				LED4	P1[21]				5.24	GPIO	J12.PX4.A15
P1[22]/MCOB0/USB_PWRD/MAT1[0]	36		1				P1_22	P1[22]				5.31	GPIO	J13.PX1.A12
P1[23]/MCI1/PWM1[4]/MISO0	37		1			1	P1_23	P1[23]				5.32	GPIO	J13.PX2.A13
P1[24]/MCI2/PWM1[5]/MOSI0	38		1			1	X_MIN	P1[24]				5.33	GPIO	J13.PX3.A14
P1[25]/MCOA1/MAT1[1]	39		1				X_MAX	P1[25]				5.34	GPIO	J13.PX4.A15
P1[26]/MCOB1/PWM1[6]/CAP0[0]	40		1				Y_MIN	P1[26]				5.41	GPIO	J14.PX1.A12
P1[27]/CLKOUT/USB_OVRCR/CAP0[1]	43		1				Y_MAX	P1[27]				5.42	GPIO	J14.PX2.A13
P1[28]/MCOA2/PCAP1[0]/MAT0[0]	44		1				Z_MIN	P1[28]				5.43	GPIO	J14.PX3.A14
P1[29]/MCOB2/PCAP1[1]/MAT0[1]	45		1				Z_MAX	P1[29]				5.44	GPIO	J14.PX4.A15
P1[17]/ENET_MDIO	86	1					Ethernet	P1[17]	ENET_MDIO			6.11	GPIO	J15.PX1.A12
P1[16]/ENET_MDC	87	1					Ethernet	P1[16]	ENET_MDC			6.12	GPIO	J15.PX2.A13
P1[15]/ENET_REF_CLK	88	1					Ethernet	P1[15]	ENET_REF_CLK			6.13	GPIO	J15.PX3.A14
P1[14]/ENET_RX_ER	89	1					Ethernet	P1[14]	ENET_RX_ER			6.14	GPIO	J15.PX4.A15
P1[10]/ENET_RXD1	90	1					Ethernet	P1[10]	ENET_RXD1			6.21	GPIO	J16.PX1.A12
P1[9]/ENET_RXD0	91	1					Ethernet	P1[9]	ENET_RXD0			6.22	GPIO	J16.PX2.A13
P1[8]/ENET_CRS	92	1					Ethernet	P1[8]	ENET_CRS			6.23	GPIO	J16.PX3.A14
P1[4]/ENET_TX_EN	93	1					Ethernet	P1[4]	ENET_TX_EN			6.24	GPIO	J16.PX4.A15
TDO/SWO	1	1					NC-JTAG	TDO	SWO					
TDI	2	1					NC-JTAG	TDI						
TMS/SWDIO	3	1					NC-JTAG	TMS	SWDIO					
TRST	4	1					NC-JTAG	TRST						
TCK/SWDCLK	5	1					NC-JTAG	TCK	SWDCLK					
VDDA	10	1					3.3V	VDDA						
VSSA	11	1					GND	VSSA						
VREFP	12	1					3.3V	VREFP						
n.c.	13	1					NC	n.c.						
RSTOUT	14	1					NC	RSTOUT						
VREFN	15	1					GND	VREFN						
RTCX1	16	1					NC	RTCX1						
RESET	17	1					Reset button	RESET						
RTCX2	18	1					NC	RTCX2						
VBAT	19	1					3.3V	VBAT						
XTAL1	22	1					Crystal	XTAL1						
XTAL2	23	1					Crystal	XTAL2						
P0[28]/SCL0/USB_SCL	24	1					I2C	P0[28]	SCL0	USB_SCL				
P0[27]/SDA0/USB_SDA	25	1					I2C	P0[27]	SDA0	USB_SDA				
VDD(3V3)	28	1					3.3V	VDD(3V3)						
P0[29]/USB_D+	29	1					USB	P0[29]	USB_D+					
P0[30]/USB_D	30	1					USB	P0[30]	USB_D					
VSS	31	1					GND	VSS						
VSS	41	1					GND	VSS						
VDD(REG)(3V3)***	42	1					3.3V	VDD(REG)(3V3)***						
VDD(3V3)	54	1					3.3V	VDD(3V3)						
VSS	55	1					GND	VSS						
VDD(3V3)	71	1					3.3V	VDD(3V3)						
VSS	72	1					GND	VSS						
VSS	83	1					GND	VSS						
VDD(REG)(3V3)	84	1					3.3V	VDD(REG)(3V3)						
P1[1]/ENET_TXD1	94	1					Ethernet	P1[1]	ENET_TXD1					
P1[0]/ENET_TXD0	95	1					Ethernet	P1[0]	ENET_TXD0					
VDD(3V3)	96	1					3.3V	VDD(3V3)						
VSS	97	1					GND	VSS						
RTCK	100	1					NC	RTCK						

Pin Name	LQFP100 Pin	Y	R/L
NC	13	-50	L
P0[0]/RD1/TXD3/SDA1	46	50	L
P0[1]/TD1/RXD3/SCL1	47	150	L
P0[10]/TXD2/SDA2/MAT3[0]	48	250	L
P0[11]/RXD2/SCL2/MAT3[1]	49	350	L
P0[15]/TXD1/SCK0/SCK	62	450	L
P0[16]/RXD1/SSEL0/SSEL	63	550	L
P0[17]/CTS1/MISO0/MISO	61	650	L
P0[18]/DCD1/MOSI0/MOSI	60	750	L
P0[19]/DSR1/SDA1	59	850	L
P0[2]/TXD0/AD0[7]	98	950	L
P0[20]/DTR1/SCL1	58	1050	L
P0[21]/RI1/RD1	57	1150	L
P0[22]/RTS1/TD1	56	1250	L
P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]	9	1350	L
P0[24]/AD0[1]/I2SRX_WS/CAP3[1]	8	1450	L
P0[25]/AD0[2]/I2SRX_SDA/TXD3	7	1550	L
P0[26]/AD0[3]/AOUT/RXD3	6	1650	L
P0[27]/SDA0/USB_SDA	25	1750	L
P0[28]/SCL0/USB_SCL	24	1850	L
P0[29]/USB_D+	29	1950	L
P0[3]/RXD0/AD0[6]	99	2050	L
P0[30]/USB_D	30	2150	L
P0[4]/I2SRX_CLK/RD2/CAP2[0]	81	2250	L
P0[5]/I2SRX_WS/TD2/CAP2[1]	80	2350	L
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]	79	2450	L
P0[7]/I2STX_CLK/SCK1/MAT2[1]	78	2550	L
P0[8]/I2STX_WS/MISO1/MAT2[2]	77	2650	L
P0[9]/I2STX_SDA/MOSI1/MAT2[3]	76	2750	L
P1[0]/ENET_TXD0	95	2850	L
P1[1]/ENET_TXD1	94	2950	L
P1[10]/ENET_RXD1	90	3050	L
P1[14]/ENET_RX_ER	89	3150	L
P1[15]/ENET_REF_CLK	88	3250	L
P1[16]/ENET_MDC	87	3350	L
P1[17]/ENET_MDIO	86	3450	L
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]	32	3550	L
P1[19]/MCOA0/USB_PPWR/CAP1[1]	33	3650	L
P1[20]/MCI0/PWM1[2]/SCK0	34	3750	L

P1[21]/MCABORT/PWM1[3]/SSEL0	35	3850 L
P1[22]/MCOB0/USB_PWRD/MAT1[0]	36	3950 L
P1[23]/MCI1/PWM1[4]/MISO0	37	4050 L
P1[24]/MCI2/PWM1[5]/MOSI0	38	4150 L
P1[25]/MCOA1/MAT1[1]	39	4250 L
P1[26]/MCOB1/PWM1[6]/CAP0[0]	40	4350 L
P1[27]/CLKOUT/USB_OVRCR/CAP0[1]	43	4450 L
P1[28]/MCOA2/PCAP1[0]/MAT0[0]	44	4550 L
P1[29]/MCOB2/PCAP1[1]/MAT0[1]	45	4650 L
P1[30]/V_{BUS}/AD0[4]	21	4750 L
P1[31]/SCK1/AD0[5]	20	4850 L
P1[4]/ENET_TX_EN	93	4950 L
P1[8]/ENET_CRS	92	5050 L
P1[9]/ENET_RXD0	91	5150 L
P2[0]/PWM1[1]/TXD1	75	5250 L
P2[1]/PWM1[2]/RXD1	74	5350 L
P2[10]/EINT0/NMI	53	5450 L
P2[11]/EINT1/I2STX_CLK	52	5550 L
P2[12]/EINT2/I2STX_WS	51	5650 L
P2[13]/EINT3/I2STX_SDA	50	5750 L
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]	73	5850 L
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]	70	5950 L
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]	69	6050 L
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]	68	6150 L
P2[6]/PCAP1[0]/RI1/TRACECLK	67	6250 L
P2[7]/RD2/RTS1	66	6350 L
P2[8]/TD2/TXD2	65	6450 L
P2[9]/USB_CONNECT/RXD2	64	6550 L
P3[25]/MAT0[0]/PWM1[2]	27	6650 L
P3[26]/STCLK/MAT0[1]/PWM1[3]	26	6750 L
P4[28]/RX_MCLK/MAT2[0]/TXD3	82	6850 L
P4[29]/TX_MCLK/MAT2[1]/RXD3	85	6950 L
RESET	17	7050 L
RSTOUT	14	7150 L
RTCK	100	7250 L
RTCX1	16	7350 L
RTCX2	18	7450 L
TCK/SWDCLK	5	7550 L
TDI	2	7650 L
TDO/SWO	1	7750 L
TMS/SWDIO	3	7850 L
TRST	4	7950 L
VBAT	19	8050 L

$V_{DD(3V3)}$	28	8150 L
$V_{DD(3V3)}$	54	8250 L
$V_{DD(3V3)}$	71	8350 L
$V_{DD(3V3)}$	96	8450 L
$V_{DD(REG)(3V3)}$	84	8550 L
$V_{DD(REG)(3V3)}$***	42	8650 L
V_{DDA}	10	8750 L
VREFN	15	8850 L
VREFP	12	8950 L
V_{SS}	31	9050 L
V_{SS}	41	9150 L
V_{SS}	55	9250 L
V_{SS}	72	9350 L
V_{SS}	83	9450 L
V_{SS}	97	9550 L
V_{SSA}	11	9650 L
XTAL1	22	9750 L
XTAL2	23	9850 L

X NC 13 1000 -50 L 50 50 1 1 B
X P0[0]/RD1/TXD3/SDA1 46 1000 50 L 50 50 1 1 B
X P0[1]/TD1/RXD3/SCL1 47 1000 150 L 50 50 1 1 B
X P0[10]/TXD2/SDA2/MAT3[0] 48 1000 250 L 50 50 1 1 B
X P0[11]/RXD2/SCL2/MAT3[1] 49 1000 350 L 50 50 1 1 B
X P0[15]/TXD1/SCK0/SCK 62 1000 450 L 50 50 1 1 B
X P0[16]/RXD1/SSEL0/SSEL 63 1000 550 L 50 50 1 1 B
X P0[17]/CTS1/MISO0/MISO 61 1000 650 L 50 50 1 1 B
X P0[18]/DCD1/MOSI0/MOSI 60 1000 750 L 50 50 1 1 B
X P0[19]/DSR1/SDA1 59 1000 850 L 50 50 1 1 B
X P0[2]/TXD0/AD0[7] 98 1000 950 L 50 50 1 1 B
X P0[20]/DTR1/SCL1 58 1000 1050 L 50 50 1 1 B
X P0[21]/RI1/RD1 57 1000 1150 L 50 50 1 1 B
X P0[22]/RTS1/TD1 56 1000 1250 L 50 50 1 1 B
X P0[23]/AD0[0]/I2SRX_CLK/CAP3[0] 9 1000 1350 L 50 50 1 1 B
X P0[24]/AD0[1]/I2SRX_WS/CAP3[1] 8 1000 1450 L 50 50 1 1 B
X P0[25]/AD0[2]/I2SRX_SDA/TXD3 7 1000 1550 L 50 50 1 1 B
X P0[26]/AD0[3]/AOUT/RXD3 6 1000 1650 L 50 50 1 1 B
X P0[27]/SDA0/USB_SDA 25 1000 1750 L 50 50 1 1 B
X P0[28]/SCL0/USB_SCL 24 1000 1850 L 50 50 1 1 B
X P0[29]/USB_D+ 29 1000 1950 L 50 50 1 1 B
X P0[3]/RXD0/AD0[6] 99 1000 2050 L 50 50 1 1 B
X P0[30]/USB_D 30 1000 2150 L 50 50 1 1 B
X P0[4]/I2SRX_CLK/RD2/CAP2[0] 81 1000 2250 L 50 50 1 1 B
X P0[5]/I2SRX_WS/TD2/CAP2[1] 80 1000 2350 L 50 50 1 1 B
X P0[6]/I2SRX_SDA/SSEL1/MAT2[0] 79 1000 2450 L 50 50 1 1 B
X P0[7]/I2STX_CLK/SCK1/MAT2[1] 78 1000 2550 L 50 50 1 1 B
X P0[8]/I2STX_WS/MISO1/MAT2[2] 77 1000 2650 L 50 50 1 1 B
X P0[9]/I2STX_SDA/MOSI1/MAT2[3] 76 1000 2750 L 50 50 1 1 B
X P1[0]/ENET_TXD0 95 1000 2850 L 50 50 1 1 B
X P1[1]/ENET_TXD1 94 1000 2950 L 50 50 1 1 B
X P1[10]/ENET_RXD1 90 1000 3050 L 50 50 1 1 B
X P1[14]/ENET_RX_ER 89 1000 3150 L 50 50 1 1 B
X P1[15]/ENET_REF_CLK 88 1000 3250 L 50 50 1 1 B
X P1[16]/ENET_MDC 87 1000 3350 L 50 50 1 1 B
X P1[17]/ENET_MDIO 86 1000 3450 L 50 50 1 1 B
X P1[18]/USB_UP_LED/PWM1[1]/CAP1[0] 32 1000 3550 L 50 50 1 1 B
X P1[19]/MCOA0/USB_PPWR/CAP1[1] 33 1000 3650 L 50 50 1 1 B
X P1[20]/MCI0/PWM1[2]/SCK0 34 1000 3750 L 50 50 1 1 B

X P1[21]/MCABORT/PWM1[3]/SSEL0 35 1000 3850 L 50 50 1 1 B
X P1[22]/MCOB0/USB_PWRD/MAT1[0] 36 1000 3950 L 50 50 1 1 B
X P1[23]/MCI1/PWM1[4]/MISO0 37 1000 4050 L 50 50 1 1 B
X P1[24]/MCI2/PWM1[5]/MOSI0 38 1000 4150 L 50 50 1 1 B
X P1[25]/MCOA1/MAT1[1] 39 1000 4250 L 50 50 1 1 B
X P1[26]/MCOB1/PWM1[6]/CAP0[0] 40 1000 4350 L 50 50 1 1 B
X P1[27]/CLKOUT/USB_OVRCR/CAP0[1] 43 1000 4450 L 50 50 1 1 B
X P1[28]/MCOA2/PCAP1[0]/MAT0[0] 44 1000 4550 L 50 50 1 1 B
X P1[29]/MCOB2/PCAP1[1]/MAT0[1] 45 1000 4650 L 50 50 1 1 B
X P1[30]/VBUS/AD0[4] 21 1000 4750 L 50 50 1 1 B
X P1[31]/SCK1/AD0[5] 20 1000 4850 L 50 50 1 1 B
X P1[4]/ENET_TX_EN 93 1000 4950 L 50 50 1 1 B
X P1[8]/ENET_CRS 92 1000 5050 L 50 50 1 1 B
X P1[9]/ENET_RXD0 91 1000 5150 L 50 50 1 1 B
X P2[0]/PWM1[1]/TXD1 75 1000 5250 L 50 50 1 1 B
X P2[1]/PWM1[2]/RXD1 74 1000 5350 L 50 50 1 1 B
X P2[10]/EINT0/NMI 53 1000 5450 L 50 50 1 1 B
X P2[11]/EINT1/I2STX_CLK 52 1000 5550 L 50 50 1 1 B
X P2[12]/EINT2/I2STX_WS 51 1000 5650 L 50 50 1 1 B
X P2[13]/EINT3/I2STX_SDA 50 1000 5750 L 50 50 1 1 B
X P2[2]/PWM1[3]/CTS1/TRACEDATA[3] 73 1000 5850 L 50 50 1 1 B
X P2[3]/PWM1[4]/DCD1/TRACEDATA[2] 70 1000 5950 L 50 50 1 1 B
X P2[4]/PWM1[5]/DSR1/TRACEDATA[1] 69 1000 6050 L 50 50 1 1 B
X P2[5]/PWM1[6]/DTR1/TRACEDATA[0] 68 1000 6150 L 50 50 1 1 B
X P2[6]/PCAP1[0]/RI1/TRACECLK 67 1000 6250 L 50 50 1 1 B
X P2[7]/RD2/RTS1 66 1000 6350 L 50 50 1 1 B
X P2[8]/TD2/TXD2 65 1000 6450 L 50 50 1 1 B
X P2[9]/USB_CONNECT/RXD2 64 1000 6550 L 50 50 1 1 B
X P3[25]/MAT0[0]/PWM1[2] 27 1000 6650 L 50 50 1 1 B
X P3[26]/STCLK/MAT0[1]/PWM1[3] 26 1000 6750 L 50 50 1 1 B
X P4[28]/RX_MCLK/MAT2[0]/TXD3 82 1000 6850 L 50 50 1 1 B
X P4[29]/TX_MCLK/MAT2[1]/RXD3 85 1000 6950 L 50 50 1 1 B
X RESET 17 1000 7050 L 50 50 1 1 B
X RSTOUT 14 1000 7150 L 50 50 1 1 B
X RTCK 100 1000 7250 L 50 50 1 1 B
X RTCX1 16 1000 7350 L 50 50 1 1 B
X RTCX2 18 1000 7450 L 50 50 1 1 B
X TCK/SWDCLK 5 1000 7550 L 50 50 1 1 B
X TDI 2 1000 7650 L 50 50 1 1 B
X TDO/SWO 1 1000 7750 L 50 50 1 1 B
X TMS/SWDIO 3 1000 7850 L 50 50 1 1 B
X TRST 4 1000 7950 L 50 50 1 1 B
X VBAT 19 1000 8050 L 50 50 1 1 B

X VDD(3V3) 28 1000 8150 L 50 50 1 1 B
X VDD(3V3) 54 1000 8250 L 50 50 1 1 B
X VDD(3V3) 71 1000 8350 L 50 50 1 1 B
X VDD(3V3) 96 1000 8450 L 50 50 1 1 B
X VDD(REG)(3V3) 84 1000 8550 L 50 50 1 1 B
X VDD(REG)(3V3)*** 42 1000 8650 L 50 50 1 1 B
X VDDA 10 1000 8750 L 50 50 1 1 B
X VREFN 15 1000 8850 L 50 50 1 1 B
X VREFP 12 1000 8950 L 50 50 1 1 B
X VSS 31 1000 9050 L 50 50 1 1 B
X VSS 41 1000 9150 L 50 50 1 1 B
X VSS 55 1000 9250 L 50 50 1 1 B
X VSS 72 1000 9350 L 50 50 1 1 B
X VSS 83 1000 9450 L 50 50 1 1 B
X VSS 97 1000 9550 L 50 50 1 1 B
X VSSA 11 1000 9650 L 50 50 1 1 B
X XTAL1 22 1000 9750 L 50 50 1 1 B
X XTAL2 23 1000 9850 L 50 50 1 1 B

X PAD2 2 1000 850 200 L 50 50 1 1 B